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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I ² C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4s2ab-an

8.1.3.4 Error Code Correction (ECC)

The Flash embeds an ECC module with 8 parity bits for each 64 data bits. The ECC is able to correct one unique error. The errors are detected while a read access is performed into memory array. The ECC (Hamming Algorithm) is a mechanism that encodes data in a manner that makes possible the identification and correction of certain errors in data. The ECC is capable of single bit error correction.

8.1.3.5 Lock Regions

Several lock bits are used to protect write and erase operations on lock regions. A lock region is composed of several consecutive pages, and each lock region has its associated lock bit.

Table 8-2. Lock Bit Number

Product	Number of Lock Bits	Lock Region Size
SAM4SD32	256 (128 + 128)	8 Kbytes
SAM4SD16	128 (64 + 64)	8 Kbytes
SAM4S16/SA16	128	8 Kbytes
SAM4S8	64	8 Kbytes
SAM4S4	32	8 Kbytes
SAM4S2	16	8 Kbytes

If a locked region erase or program command occurs, the command is aborted and the EEFC triggers an interrupt. The lock bits are software programmable through the EEFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.1.3.6 Security Bit

The SAM4SD32/SD16/S16/SA16/S8/S4/S2 feature one security bit based on a specific General Purpose NVM bit (GPNVM bit 0). When the security bit is enabled, any access to the Flash, SRAM, core registers and internal peripherals through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled through the command “Set General Purpose NVM Bit 0” of the EEFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full Flash erase is performed. When the security bit is deactivated, all accesses to the Flash, SRAM, Core registers, Internal Peripherals are permitted.

The ERASE pin integrates a permanent pull-down. Consequently, it can be left unconnected during normal operation. However, it is recommended, in harsh environment, to connect it directly to GND if the erase operation is not used in the application.

To avoid unexpected erase at power-up, a minimum ERASE pin assertion time is required. This time is defined in Table 44-74 “AC Flash Characteristics”.

The erase operation is not performed when the system is in Wait mode with the Flash in deep-power-down mode.

To make sure that the erase operation is performed after power-up, the system must not reconfigure the ERASE pin as GPIO or enter Wait mode with Flash in Deep-power-down mode before the ERASE pin assertion time has elapsed.

The following sequence ensures the erase operation in all cases:

1. Assert the ERASE pin (High)
2. Assert the NRST pin (Low)
3. Power cycle the device

12.6.4.4 LDR and STR, Unprivileged

Load and Store with unprivileged access.

Syntax

```
op{type}T{cond} Rt, [Rn {, #offset}] ; immediate offset
```

where:

op is one of:

LDR Load Register.

STR Store Register.

type is one of:

B unsigned byte, zero extend to 32 bits on loads.

SB signed byte, sign extend to 32 bits (LDR only).

H unsigned halfword, zero extend to 32 bits on loads.

SH signed halfword, sign extend to 32 bits (LDR only).

- omit, for word.

cond is an optional condition code, see “Conditional Execution” .

Rt is the register to load or store.

Rn is the register on which the memory address is based.

offset is an offset from *Rn* and can be 0 to 255.

If *offset* is omitted, the address is the value in *Rn*.

Operation

These load and store instructions perform the same function as the memory access instructions with immediate offset, see “LDR and STR, Immediate Offset” . The difference is that these instructions have only unprivileged access even when used in privileged software.

When used in unprivileged software, these instructions behave in exactly the same way as normal memory access instructions with immediate offset.

Restrictions

In these instructions:

- *Rn* must not be PC
- *Rt* must not be SP and must not be PC.

Condition Flags

These instructions do not change the flags.

Examples

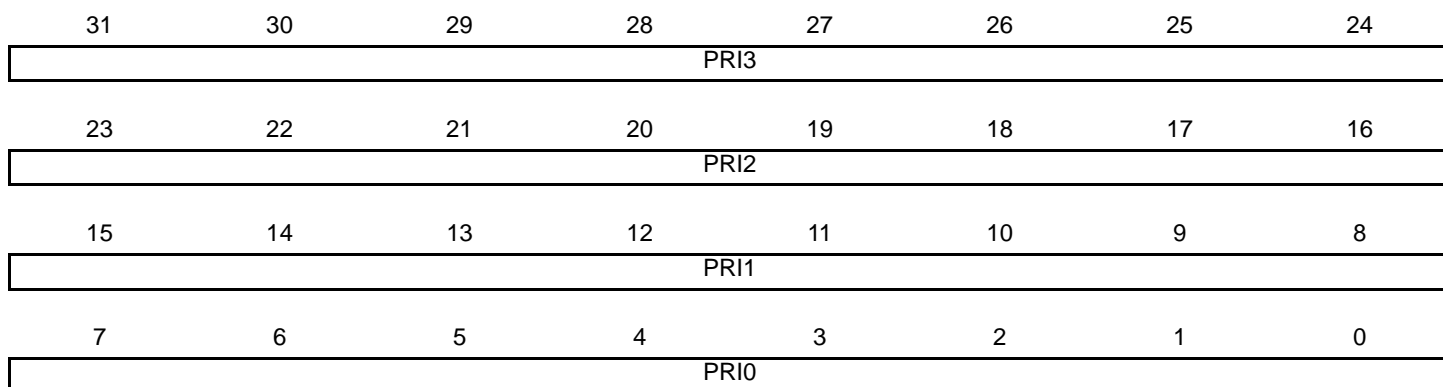
```
STRBTEQ R4, [R7] ; Conditionally store least significant byte in  
; R4 to an address in R7, with unprivileged access  
LDRHT R2, [R2, #8] ; Load halfword value from an address equal to  
; sum of R2 and 8 into R2, with unprivileged access
```

12.8.3.6 Interrupt Priority Registers

Name: NVIC_IPRx [x=0..8]

Access: Read/Write

Reset: 0x00000000



The NVIC_IPR0–NVIC_IPR registers provide a 8-bit priority field for each interrupt. These registers are byte-accessible. Each register holds four priority fields that map up to four elements in the CMSIS interrupt priority array IP[0] to IP[].

- **PRI3: Priority (4m+3)**

Priority, Byte Offset 3, refers to register bits [31:24].

- **PRI2: Priority (4m+2)**

Priority, Byte Offset 2, refers to register bits [23:16].

- **PRI1: Priority (4m+1)**

Priority, Byte Offset 1, refers to register bits [15:8].

- **PRI0: Priority (4m)**

Priority, Byte Offset 0, refers to register bits [7:0].

- Notes:
1. Each priority field holds a priority value, 0–15. The lower the value, the greater the priority of the corresponding interrupt. The processor implements only bits[7:4] of each field; bits[3:0] read as zero and ignore writes.
 2. For more information about the IP[0] to IP[34] interrupt priority array, that provides the software view of the interrupt priorities, see Table 12-29, “CMSIS Functions for NVIC Control” .
 3. The corresponding IPR number n is given by $n = m \text{ DIV } 4$.
 4. The byte offset of the required Priority field in this register is $m \text{ MOD } 4$.

12.9.1.4 Vector Table Offset Register

Name: SCB_VTOR

Access: Read/Write

31	30	29	28	27	26	25	24
TBLOFF							
23	22	21	20	19	18	17	16
TBLOFF							
15	14	13	12	11	10	9	8
TBLOFF							
7	6	5	4	3	2	1	0
TBLOFF	–	–	–	–	–	–	–

The SCB_VTOR indicates the offset of the vector table base address from memory address 0x00000000.

- **TBLOFF: Vector Table Base Offset**

It contains bits [29:7] of the offset of the table base from the bottom of the memory map.

Bit [29] determines whether the vector table is in the code or SRAM memory region:

0: Code.

1: SRAM.

It is sometimes called the TBLBASE bit.

Note: When setting TBLOFF, the offset must be aligned to the number of exception entries in the vector table. Configure the next statement to give the information required for your implementation; the statement reminds the user of how to determine the alignment requirement. The minimum alignment is 32 words, enough for up to 16 interrupts. For more interrupts, adjust the alignment by rounding up to the next power of two. For example, if 21 interrupts are required, the alignment must be on a 64-word boundary because the required table size is 37 words, and the next power of two is 64.

Table alignment requirements mean that bits[6:0] of the table offset are always zero.

13.5.6.3 5.4.3. How to Configure the TPIU

This example only concerns the asynchronous trace mode.

- Set the TRCENA bit to 1 into the Debug Exception and Monitor Register (0xE000EDFC) to enable the use of trace and debug blocks.
- Write 0x2 into the Selected Pin Protocol Register
 - Select the Serial Wire Output – NRZ
- Write 0x100 into the Formatter and Flush Control Register
- Set the suitable clock prescaler value into the Async Clock Prescaler Register to scale the baud rate of the asynchronous output (this can be done automatically by the debugging tool).

13.5.7 IEEE® 1149.1 JTAG Boundary Scan

IEEE 1149.1 JTAG Boundary Scan allows pin-level access independent of the device packaging technology.

IEEE 1149.1 JTAG Boundary Scan is enabled when TST is tied to low, while JTAGSEL is high during power-up, and must be kept in this state during the whole boundary scan operation. The SAMPLE, EXTEST and BYPASS functions are implemented. In SWD/JTAG debug mode, the ARM processor responds with a non-JTAG chip ID that identifies the processor. This is not IEEE 1149.1 JTAG-compliant.

It is not possible to switch directly between JTAG Boundary Scan and SWJ Debug Port operations. A chip reset must be performed after JTAGSEL is changed.

A Boundary-scan Descriptor Language (BSDL) file is provided on Atmel's web site to set up the test.

13.5.7.1 JTAG Boundary-scan Register

The Boundary-scan Register (BSR) contains a number of bits which correspond to active pins and associated control signals.

Each SAM4 input/output pin corresponds to a 3-bit register in the BSR. The OUTPUT bit contains data that can be forced on the pad. The INPUT bit facilitates the observability of data applied to the pad. The CONTROL bit selects the direction of the pad.

For more information, please refer to BSDL files available for the SAM4 Series.

15.5 Real-time Timer (RTT) User Interface

Table 15-1. Register Mapping

Offset	Register	Name	Access	Reset
0x00	Mode Register	RTT_MR	Read/Write	0x0000_8000
0x04	Alarm Register	RTT_AR	Read/Write	0xFFFF_FFFF
0x08	Value Register	RTT_VR	Read-only	0x0000_0000
0x0C	Status Register	RTT_SR	Read-only	0x0000_0000

16.6.6 RTC Calendar Alarm Register

Name: RTC_CALALR

Address: 0x400E1474

Access: Read/Write

31	30	29	28	27	26	25	24
DATEEN	–	DATE					
23	22	21	20	19	18	17	16
MTHEN	–	–	MONTH				
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

This register can only be written if the WPEN bit is cleared in the System Controller Write Protection Mode Register (SYSC_WPMR).

Note: To change one of the DATE, MONTH fields, it is recommended to disable the field before changing the value and then re-enable it after the change has been made. This requires up to three accesses to the RTC_CALALR. The first access clears the enable corresponding to the field to change (DATEEN, MTHEN). If the field is already cleared, this access is not required. The second access performs the change of the value (DATE, MONTH). The third access is required to re-enable the field by writing 1 in DATEEN, MTHEN fields.

- **MONTH: Month Alarm**

This field is the alarm field corresponding to the BCD-coded month counter.

- **MTHEN: Month Alarm Enable**

0: The month-matching alarm is disabled.

1: The month-matching alarm is enabled.

- **DATE: Date Alarm**

This field is the alarm field corresponding to the BCD-coded date counter.

- **DATEEN: Date Alarm Enable**

0: The date-matching alarm is disabled.

1: The date-matching alarm is enabled.

16.6.8 RTC Status Clear Command Register

Name: RTC_SCCR

Address: 0x400E147C

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	TDERRCLR	CALCLR	TIMCLR	SECCLR	ALRCLR	ACKCLR

- **ACKCLR: Acknowledge Clear**

0: No effect.

1: Clears corresponding status flag in the Status Register (RTC_SR).

- **ALRCLR: Alarm Clear**

0: No effect.

1: Clears corresponding status flag in the Status Register (RTC_SR).

- **SECCLR: Second Clear**

0: No effect.

1: Clears corresponding status flag in the Status Register (RTC_SR).

- **TIMCLR: Time Clear**

0: No effect.

1: Clears corresponding status flag in the Status Register (RTC_SR).

- **CALCLR: Calendar Clear**

0: No effect.

1: Clears corresponding status flag in the Status Register (RTC_SR).

- **TDERRCLR: Time and/or Date Free Running Error Clear**

0: No effect.

1: Clears corresponding status flag in the Status Register (RTC_SR).

23.7.9 CRCCU Control Register

Name: CRCCU_CR

Address: 0x40044034

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	RESET

- **RESET: CRC Computation Reset**

0: No effect

1: Sets the CRCCU_SR to 0xFFFFFFFF

25.8.7 Write Protection Status Register

Name: MATRIX_WPSR

Address: 0x400E03E8

Access: Read-only

Reset: See Table 25-4

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
WPVSR							
15	14	13	12	11	10	9	8
WPVSR							
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	WPVS

- **WPVS: Write Protection Violation Status**

0: No write protection violation has occurred since the last read of the MATRIX_WPSR.

1: A write protection violation has occurred since the last read of the MATRIX_WPSR. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSR.

- **WPVSR: Write Protection Violation Source**

When WPVS = 1, WPVSR indicates the register address offset at which a write access has been attempted.

- “SMC Cycle Register”
- “SMC MODE Register”

26.9.6 Coding Timing Parameters

All timing parameters are defined for one chip select and are grouped together in one SMC_REGISTER according to their type.

The SMC_SETUP register groups the definition of all setup parameters:

- NRD_SETUP, NCS_RD_SETUP, NWE_SETUP, NCS_WR_SETUP

The SMC_PULSE register groups the definition of all pulse parameters:

- NRD_PULSE, NCS_RD_PULSE, NWE_PULSE, NCS_WR_PULSE

The SMC_CYCLE register groups the definition of all cycle parameters:

- NRD_CYCLE, NWE_CYCLE

Table 26-4 shows how the timing parameters are coded and their permitted range.

Table 26-4. Coding and Range of Timing Parameters

Coded Value	Number of Bits	Effective Value	Permitted Range	
			Coded Value	Effective Value
setup [5:0]	6	$128 \times \text{setup}[5] + \text{setup}[4:0]$	$0 \leq \leq 31$	$0 \leq \leq 128+31$
pulse [6:0]	7	$256 \times \text{pulse}[6] + \text{pulse}[5:0]$	$0 \leq \leq 63$	$0 \leq \leq 256+63$
cycle [8:0]	9	$256 \times \text{cycle}[8:7] + \text{cycle}[6:0]$	$0 \leq \leq 127$	$0 \leq \leq 256+127$ $0 \leq \leq 512+127$ $0 \leq \leq 768+127$

26.9.7 Reset Values of Timing Parameters

Table 26-5 gives the default value of timing parameters at reset.

Table 26-5. Reset Values of Timing Parameters

Register	Reset Value	Definition
SMC_SETUP	0x01010101	All setup timings are set to 1.
SMC_PULSE	0x01010101	All pulse timings are set to 1.
SMC_CYCLE	0x00030003	The read and write operations last 3 Master Clock cycles and provide one hold cycle.
WRITE_MODE	1	Write is controlled with NWE.
READ_MODE	1	Read is controlled with NRD.

26.9.8 Usage Restriction

The SMC does not check the validity of the user-programmed parameters. If the sum of SETUP and PULSE parameters is larger than the corresponding CYCLE parameter, this leads to unpredictable behavior of the SMC.

For read operations:

Null but positive setup and hold of address and NRD and/or NCS can not be guaranteed at the memory interface because of the propagation delay of these signals through external logic and pads. If positive setup and hold values must be verified, then it is strictly recommended to program non-null values so as to cover possible skews between address, NCS and NRD signals.

29.15 Clock Switching Details

29.15.1 Master Clock Switching Timings

Table 29-1 and Table 29-2 give the worst case timings required for the master clock to switch from one selected clock to another one. This is in the event that the prescaler is de-activated. When the prescaler is activated, an additional time of 64 clock cycles of the newly selected clock has to be added.

Table 29-1. Clock Switching Timings (Worst Case)

To	From	Main Clock	SLCK	PLL Clock
Main Clock		–	$4 \times \text{SLCK} + 2.5 \times \text{Main Clock}$	$3 \times \text{PLL Clock} + 4 \times \text{SLCK} + 1 \times \text{Main Clock}$
SLCK		$0.5 \times \text{Main Clock} + 4.5 \times \text{SLCK}$	–	$3 \times \text{PLL Clock} + 5 \times \text{SLCK}$
PLL Clock		$0.5 \times \text{Main Clock} + 4 \times \text{SLCK} + \text{PLLCOUNT} \times \text{SLCK} + 2.5 \times \text{PLLx Clock}$	$2.5 \times \text{PLL Clock} + 5 \times \text{SLCK} + \text{PLLCOUNT} \times \text{SLCK}$	$2.5 \times \text{PLL Clock} + 4 \times \text{SLCK} + \text{PLLCOUNT} \times \text{SLCK}$

Notes: 1. PLL designates either the PLLA or the PLLB Clock.
2. PLLCOUNT designates either PLLACOUNT or PLLBCOUNT.

Table 29-2. Clock Switching Timings between Two PLLs (Worst Case)

To	From	PLLA Clock	PLLB Clock
PLLA Clock		$2.5 \times \text{PLLA Clock} + 4 \times \text{SLCK} + \text{PLLACOUNT} \times \text{SLCK}$	$3 \times \text{PLLA Clock} + 4 \times \text{SLCK} + 1.5 \times \text{PLLA Clock}$
PLLB Clock		$3 \times \text{PLLB Clock} + 4 \times \text{SLCK} + 1.5 \times \text{PLLB Clock}$	$2.5 \times \text{PLLB Clock} + 4 \times \text{SLCK} + \text{PLLBCOUNT} \times \text{SLCK}$

31.5.15 Register Write Protection

To prevent any single software error from corrupting PIO behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the PIO Write Protection Mode Register (PIO_WPMR).

If a write access to a write-protected register is detected, the WPVS flag in the PIO Write Protection Status Register (PIO_WPSR) is set and the field WPVSR indicates the register in which the write access has been attempted.

The WPVS bit is automatically cleared after reading the PIO_WPSR.

The following registers can be write-protected:

- PIO Enable Register
- PIO Disable Register
- PIO Output Enable Register
- PIO Output Disable Register
- PIO Input Filter Enable Register
- PIO Input Filter Disable Register
- PIO Multi-driver Enable Register
- PIO Multi-driver Disable Register
- PIO Pull-Up Disable Register
- PIO Pull-Up Enable Register
- PIO Peripheral ABCD Select Register 1
- PIO Peripheral ABCD Select Register 2
- PIO Output Write Enable Register
- PIO Output Write Disable Register
- PIO Pad Pull-Down Disable Register
- PIO Pad Pull-Down Enable Register
- PIO Parallel Capture Mode Register

31.6.22 PIO Pull-Up Enable Register

Name: PIO_PUER

Address: 0x400E0E64 (PIOA), 0x400E1064 (PIOB), 0x400E1264 (PIOC)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

- **P0–P31: Pull-Up Enable**

0: No effect.

1: Enables the pull-up resistor on the I/O line.

33.2 Embedded Characteristics

- Master or Slave Serial Peripheral Bus Interface
 - 8-bit to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delay between consecutive transfers and delay before SPI clock per chip select
 - Programmable delay between chip selects
 - Selectable mode fault detection
- Master Mode can drive SPCK up to Peripheral Clock
- Master Mode Bit Rate can be Independent of the Processor/Peripheral Clock
- Slave mode operates on SPCK, asynchronously with core and bus clock
- Four chip selects with external decoder support allow communication with up to 15 peripherals
- Communication with Serial External Devices Supported
 - Serial memories, such as DataFlash and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD controllers, CAN controllers and sensors
 - External coprocessors
- Connection to PDC Channel Capabilities, Optimizing Data Transfers
 - One channel for the receiver
 - One channel for the transmitter
- Register Write Protection

- **CTSIC: Clear to Send Input Change Flag (cleared on read)**

0: No input change has been detected on the CTS pin since the last read of US_CSR.

1: At least one input change has been detected on the CTS pin since the last read of US_CSR.

- **RI: Image of RI Input**

0: RI input is driven low.

1: RI input is driven high.

- **DSR: Image of DSR Input**

0: DSR input is driven low.

1: DSR input is driven high.

- **DCD: Image of DCD Input**

0: DCD input is driven low.

1: DCD input is driven high.

- **CTS: Image of CTS Input**

0: CTS input is driven low.

1: CTS input is driven high.

- **MANERR: Manchester Error (cleared by writing a one to the bit US_CR.RSTSTA)**

0: No Manchester error has been detected since the last RSTSTA.

1: At least one Manchester error has been detected since the last RSTSTA.

38.14.12 HSMCI Status Register

Name: HSMCI_SR

Address: 0x40000040

Access: Read-only

31	30	29	28	27	26	25	24
UNRE	OVRE	ACKRCVE	ACKRCV	XFRDONE	FIFOEMPTY	–	–
23	22	21	20	19	18	17	16
CSTOE	DTOE	DCRCE	RTOE	RENDE	RCRCE	RDIRE	RINDE
15	14	13	12	11	10	9	8
TXBUFE	RXBUFF	CSRCV	SDIOWAIT	–	–	–	SDIOIRQA
7	6	5	4	3	2	1	0
ENDTX	ENDRX	NOTBUSY	DTIP	BLKE	TXRDY	RXRDY	CMDRDY

- **CMDRDY: Command Ready (cleared by writing in HSMCI_CMDR)**

0: A command is in progress.

1: The last command has been sent.

- **RXRDY: Receiver Ready (cleared by reading HSMCI_RDR)**

0: Data has not yet been received since the last read of HSMCI_RDR.

1: Data has been received since the last read of HSMCI_RDR.

- **TXRDY: Transmit Ready (cleared by writing in HSMCI_TDR)**

0: The last data written in HSMCI_TDR has not yet been transferred in the Shift Register.

1: The last data written in HSMCI_TDR has been transferred in the Shift Register.

- **BLKE: Data Block Ended (cleared on read)**

This flag must be used only for Write Operations.

0: A data block transfer is not yet finished.

1: A data block transfer has ended, including the CRC16 Status transmission. The flag is set for each transmitted CRC Status.

Refer to the MMC or SD Specification for more details concerning the CRC Status.

- **DTIP: Data Transfer in Progress (cleared at the end of CRC16 calculation)**

0: No data transfer in progress.

1: The current data transfer is still in progress, including CRC16 calculation.

- **NOTBUSY: HSMCI Not Busy**

A block write operation uses a simple busy signalling of the write operation duration on the data (DAT0) line: during a data transfer block, if the card does not have a free data receive buffer, the card indicates this condition by pulling down the data line (DAT0) to LOW. The card stops pulling down the data line as soon as at least one receive buffer for the defined data transfer block length becomes free.

Refer to the MMC or SD Specification for more details concerning the busy behavior.

39.7.29 PWM Stepper Motor Mode Register

Name: PWM_SMMR

Address: 0x400200B0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	DOWN1	DOWN0
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	GCEN1	GCEN0

- **GCENx: Gray Count ENable**

0: Disable gray count generation on PWML[2*x], PWMH[2*x], PWML[2*x +1], PWMH[2*x +1]

1: Enable gray count generation on PWML[2*x], PWMH[2*x], PWML[2*x +1], PWMH[2*x +1].

- **DOWNx: DOWN Count**

0: Up counter.

1: Down counter.

- **WAKEUP: USB Bus Wakeup Interrupt**

0: USB Bus Wakeup Interrupt is disabled

1: USB Bus Wakeup Interrupt is enabled

Note: When the USB block is in suspend mode, the application may power down the USB logic. In this case, any USB HOST resume request that is made must be taken into account and, thus, the reset value of the RXRSM bit of the register UDP_IMR is enabled.

45.3 100-ball VFBGA Mechanical Characteristics

Figure 45-3. 100-ball VFBGA Package Drawing

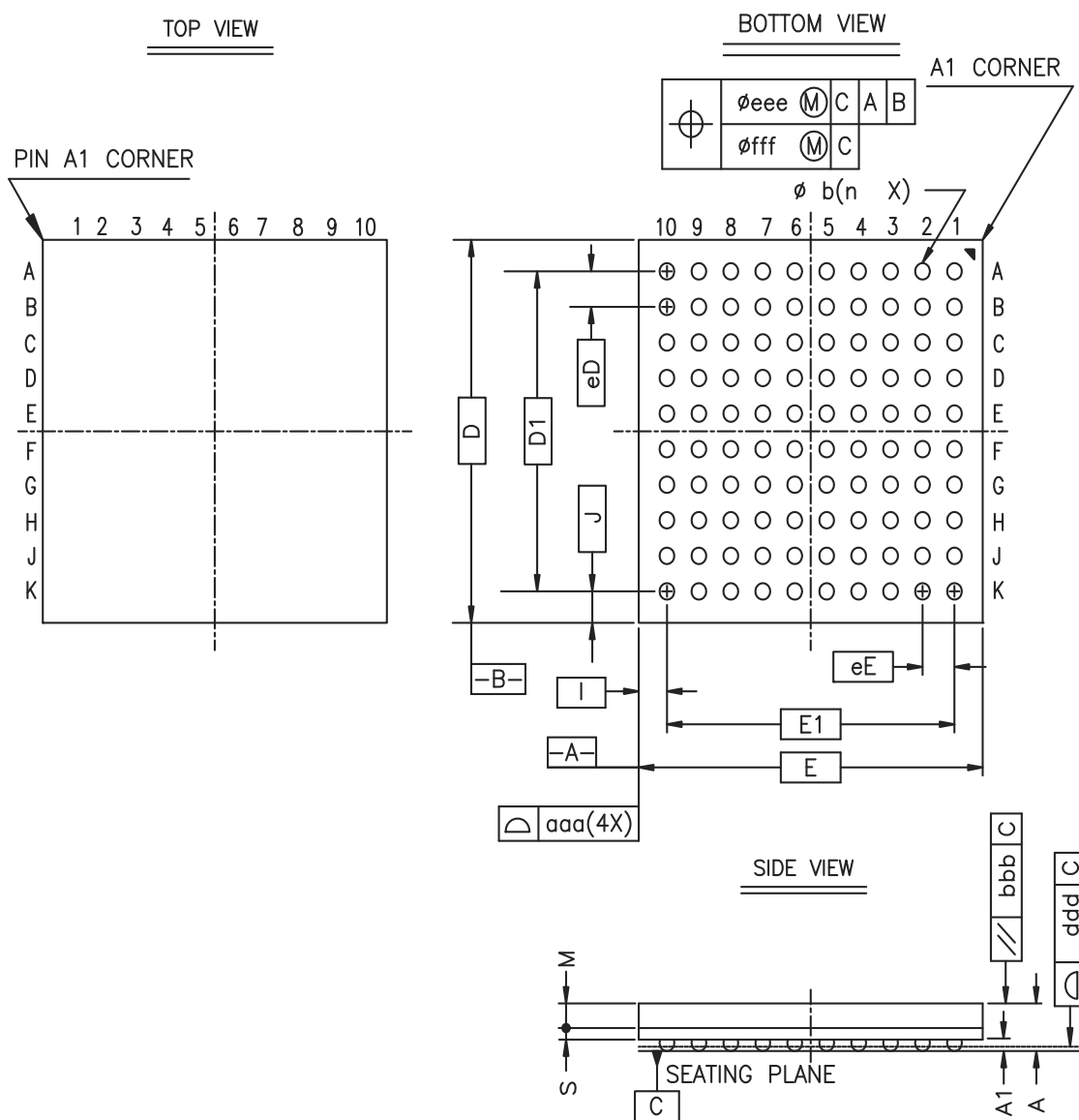


Table 45-8. VFBGA Package Dimensions

		Symbol	Common Dimensions (mm)
Package:			VFBGA
Body Size:	X	E	7.000 ± 0.100
	Y	D	7.000 ± 0.100
Ball Pitch:	X	eE	0.650
	Y	eD	0.650
Total Thickness:		A	1.000 max
Mold Thickness:		M	0.450 ref.
Substrate Thickness:		S	0.210 ref.