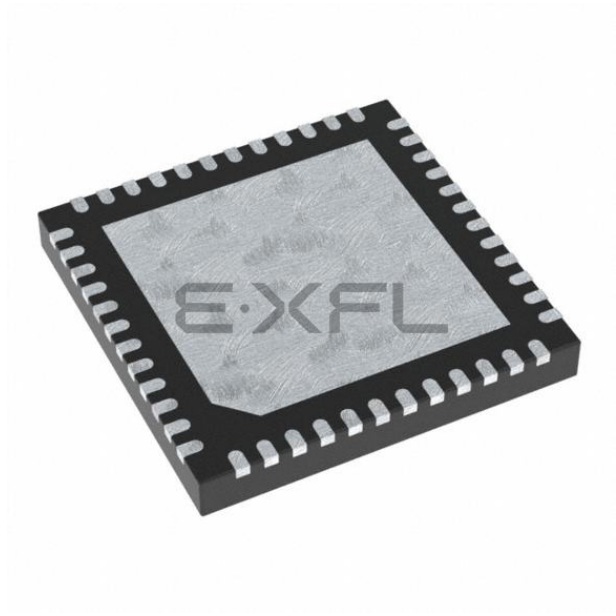

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-VFQFN Exposed Pad |
| Supplier Device Package | 48-QFN (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsam4s2ab-mn |

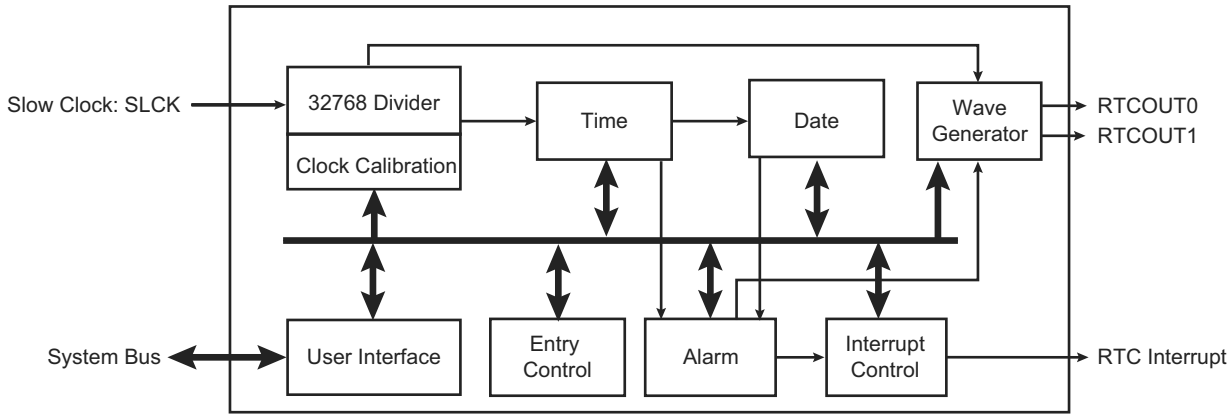
- I/O
  - Up to 79 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and on-die series resistor termination
  - Three 32-bit Parallel Input/Output Controllers, Peripheral DMA-assisted Parallel Capture mode
- Packages
  - 100-lead packages
    - LQFP – 14 x 14 mm, pitch 0.5 mm
    - TFBGA – 9 x 9 mm, pitch 0.8 mm
    - VFBGA – 7 x 7 mm, pitch 0.65 mm
  - 64-lead packages
    - LQFP – 10 x 10 mm, pitch 0.5 mm
    - QFN – 9 x 9 mm, pitch 0.5 mm
    - WLCSP – 4.42 x 4.72 mm, pitch 0.4 mm (SAM4SD32/SAM4SD16)
    - WLCSP – 4.42 x 3.42 mm, pitch 0.4 mm (SAM4S16/S8)
    - WLCSP – 3.32 x 3.32 mm, pitch 0.4 mm (SAM4S4/S2)
  - 48-lead packages
    - LQFP – 7 x 7 mm, pitch 0.5 mm
    - QFN – 7 x 7 mm, pitch 0.5 mm

**Table 12-13. Cortex-M4 Instructions (Continued)**

| Mnemonic | Operands | Description | Flags |
|---|---|---|---|
| LDMDB, LDMEA | Rn{!}, reglist | Load Multiple registers, decrement before | – |
| LDMFD, LDMIA | Rn{!}, reglist | Load Multiple registers, increment after | – |
| LDR | Rt, [Rn, #offset] | Load Register with word | – |
| LDRB, LDRBT | Rt, [Rn, #offset] | Load Register with byte | – |
| LDRD | Rt, Rt2, [Rn, #offset] | Load Register with two bytes | – |
| LDREX | Rt, [Rn, #offset] | Load Register Exclusive | – |
| LDREXB | Rt, [Rn] | Load Register Exclusive with byte | – |
| LDREXH | Rt, [Rn] | Load Register Exclusive with halfword | – |
| LDRH, LDRHT | Rt, [Rn, #offset] | Load Register with halfword | – |
| LDRSB, DRSBT | Rt, [Rn, #offset] | Load Register with signed byte | – |
| LDRSH, LDRSHT | Rt, [Rn, #offset] | Load Register with signed halfword | – |
| LDRT | Rt, [Rn, #offset] | Load Register with word | – |
| LSL, LSLS | Rd, Rm, <Rs\|#n> | Logical Shift Left | N,Z,C |
| LSR, LSRS | Rd, Rm, <Rs\|#n> | Logical Shift Right | N,Z,C |
| MLA | Rd, Rn, Rm, Ra | Multiply with Accumulate, 32-bit result | – |
| MLS | Rd, Rn, Rm, Ra | Multiply and Subtract, 32-bit result | – |
| MOV, MOVS | Rd, Op2 | Move | N,Z,C |
| MOVT | Rd, #imm16 | Move Top | – |
| MOVW, MOV | Rd, #imm16 | Move 16-bit constant | N,Z,C |
| MRS | Rd, spec_reg | Move from special register to general register | – |
| MSR | spec_reg, Rm | Move from general register to special register | N,Z,C,V |
| MUL, MULS | {Rd,} Rn, Rm | Multiply, 32-bit result | N,Z |
| MVN, MVNS | Rd, Op2 | Move NOT | N,Z,C |
| NOP | – | No Operation | – |
| ORN, ORNS | {Rd,} Rn, Op2 | Logical OR NOT | N,Z,C |
| ORR, ORRS | {Rd,} Rn, Op2 | Logical OR | N,Z,C |
| PKHTB, PKHBT | {Rd,} Rn, Rm, Op2 | Pack Halfword | – |
| POP | reglist | Pop registers from stack | – |
| PUSH | reglist | Push registers onto stack | – |
| QADD | {Rd,} Rn, Rm | Saturating double and Add | Q |
| QADD16 | {Rd,} Rn, Rm | Saturating Add 16 | – |
| QADD8 | {Rd,} Rn, Rm | Saturating Add 8 | – |
| QASX | {Rd,} Rn, Rm | Saturating Add and Subtract with Exchange | – |
| QDADD | {Rd,} Rn, Rm | Saturating Add | Q |
| QDSUB | {Rd,} Rn, Rm | Saturating double and Subtract | Q |
| QSAX | {Rd,} Rn, Rm | Saturating Subtract and Add with Exchange | – |
| QSUB | {Rd,} Rn, Rm | Saturating Subtract | Q |

## 16.3 Block Diagram

**Figure 16-1. RTC Block Diagram**




## 16.4 Product Dependencies

### 16.4.1 Power Management

The Real-time Clock is continuously clocked at 32.768 kHz. The Power Management Controller has no effect on RTC behavior.

### 16.4.2 Interrupt

RTC interrupt line is connected on one of the internal sources of the interrupt controller. RTC interrupt requires the interrupt controller to be programmed first.

**Table 16-1. Peripheral IDs**

| Instance | ID |
|---|---|
| RTC | 2 |

## 16.5 Functional Description

The RTC provides a full binary-coded decimal (BCD) clock that includes century (19/20), year (with leap years), month, date, day, hours, minutes and seconds reported in RTC Time Register (RTC_TIMR) and RTC Calendar Register (RTC_CALR).

The valid year range is up to 2099 in Gregorian mode (or 1300 to 1499 in Persian mode).

The RTC can operate in 24-hour mode or in 12-hour mode with an AM/PM indicator.

Corrections for leap years are included (all years divisible by 4 being leap years except 1900). This is correct up to the year 2099.

The RTC can generate configurable waveforms on RTCOUT0/1 outputs.

### 16.5.1 Reference Clock

The reference clock is the Slow Clock (SLCK). It can be driven internally or by an external 32.768 kHz crystal.

During low power modes of the processor, the oscillator runs and power consumption is critical. The crystal selection has to take into account the current consumption for power saving and the frequency drift due to temperature effect on the circuit for time accuracy.

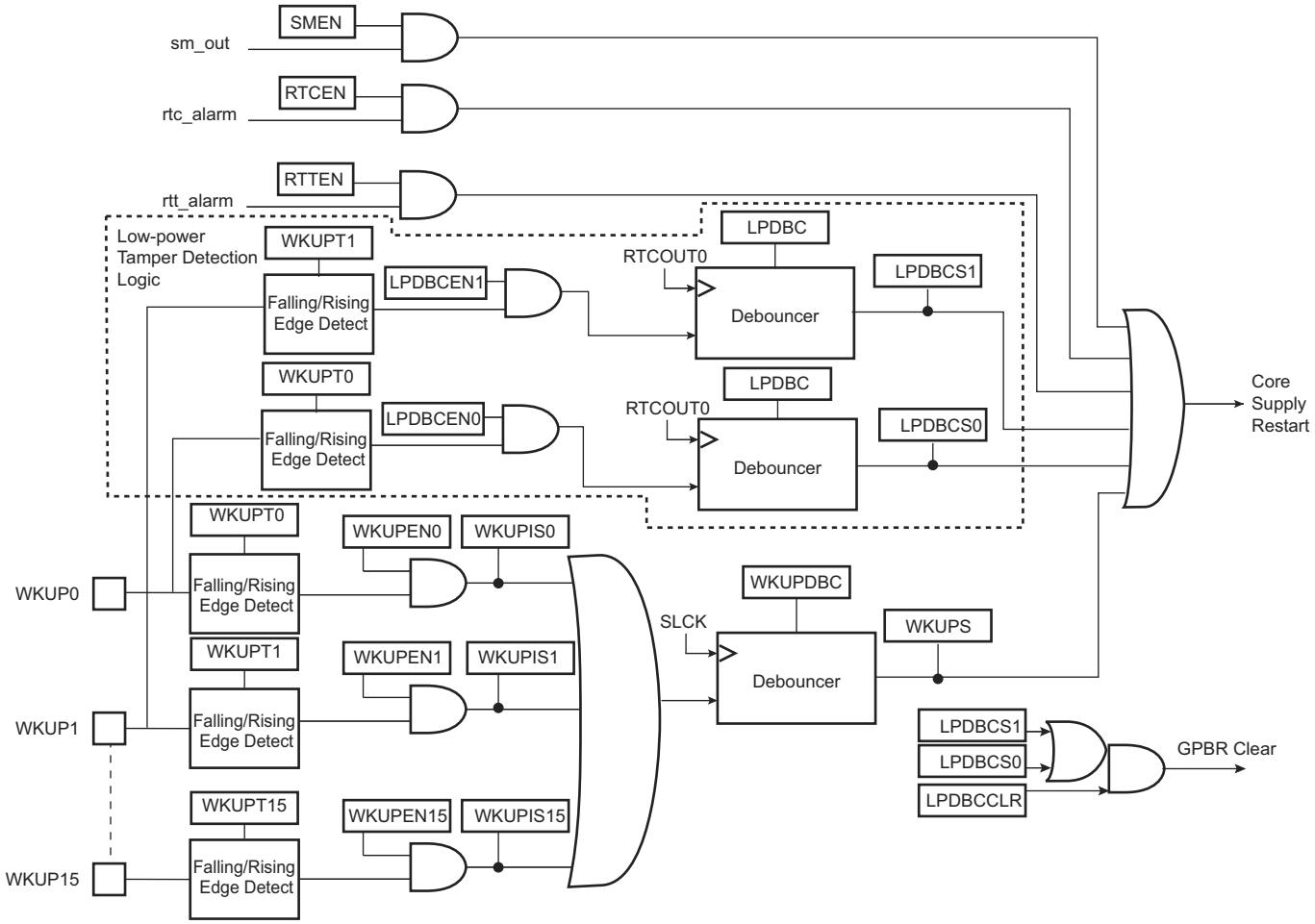
If BODRSTEN is set and the voltage regulation is lost (output voltage of the regulator too low), the vddcore_nreset signal is asserted for a minimum of one slow clock cycle and then released if bodcore_in has been reactivated. The BODRSTS bit in SUPC_SR indicates the source of the last reset.

Until bodcore_in is deactivated, the vddcore_nreset signal remains active.

### 18.4.7 Wake-up Sources

The wake-up events allow the device to exit Backup mode. When a wake-up event is detected, the SUPC performs a sequence that automatically reenables the core power supply.

**Figure 18-4. Wake-up Sources**




#### 18.4.7.1 Wake-up Inputs

The wake-up inputs, WKUPx, can be programmed to perform a wake-up of the core power supply. Each input can be enabled by writing a 1 to the corresponding bit, WKUPENx, in the Wake-up Inputs register (SUPC_WUIR). The wake-up level can be selected with the corresponding polarity bit, WKUPTx, also located in SUPC_WUIR.

The resulting signals are wired-ORed to trigger a debounce counter, which is programmed with the WKUPDBC field in SUPC_WUMR. The WKUPDBC field selects a debouncing period of 3, 32, 512, 4,096 or 32,768 slow clock cycles. The duration of these periods corresponds, respectively, to about 100 µs, about 1 ms, about 16 ms, about 128 ms and about 1 second (for a typical slow clock frequency of 32 kHz). Programming WKUPDBC to 0x0 selects an immediate wake-up, i.e., an enabled WKUP pin must be active according to its polarity during a minimum of one slow clock period to wake up the core power supply.

### 18.5.4 Supply Controller Supply Monitor Mode Register

**Name:** SUPC_SMMR

**Address:** 0x400E1414

**Access:** Read/Write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| – | – | SMIEN | SMRSTEN | – | SMSMPL | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | SMTH | | | |

This register is located in the VDDIO domain.

This register can only be written if the WPEN bit is cleared in the System Controller Write Protection Mode Register (SYSC_MR).

- **SMTH: Supply Monitor Threshold**

Selects the threshold voltage of the supply monitor. Refer to the Electrical Characteristics for voltage values.

- **SMSMPL: Supply Monitor Sampling Period**

| Value | Name | Description |
|---|---|---|
| 0x0 | SMD | Supply Monitor disabled |
| 0x1 | CSM | Continuous Supply Monitor |
| 0x2 | 32SLCK | Supply Monitor enabled one SLCK period every 32 SLCK periods |
| 0x3 | 256SLCK | Supply Monitor enabled one SLCK period every 256 SLCK periods |
| 0x4 | 2048SLCK | Supply Monitor enabled one SLCK period every 2,048 SLCK periods |

- **SMRSTEN: Supply Monitor Reset Enable**

0 (NOT_ENABLE): The core reset signal vddcore_nreset is not affected when a supply monitor detection occurs.

1 (ENABLE): The core reset signal, vddcore_nreset is asserted when a supply monitor detection occurs.

- **SMIEN: Supply Monitor Interrupt Enable**

0 (NOT_ENABLE): The SUPC interrupt signal is not affected when a supply monitor detection occurs.

1 (ENABLE): The SUPC interrupt signal is asserted when a supply monitor detection occurs.

# 19. General Purpose Backup Registers (GPBR)

## 19.1 Description

The System Controller embeds 256 bits of General Purpose Backup registers organized as Eight 32-bit registers.

It is possible to generate an immediate clear of the content of General Purpose Backup registers 0 to 3 (first half) if a Low-power Debounce event is detected on one of the wakeup pins, WKUP0 or WKUP1. The content of the other General Purpose Backup registers (second half) remains unchanged.

The Supply Controller module must be programmed accordingly. In the register SUPC_WUMR in the Supply Controller module, LPDBCCLR, LPDBCEN0 and/or LPDBCEN1 bit must be configured to 1 and LPDBC must be other than 0.

If a Tamper event has been detected, it is not possible to write to the General Purpose Backup registers while the LPDBCS0 or LPDBCS1 flags are not cleared in the Supply Controller Status Register (SUPC_SR).

## 19.2 Embedded Characteristics

- 256 bits of General Purpose Backup Registers

### 20.5.3 EEFC Flash Status Register

**Name:** EEFC_FSR

**Address:** 0x400E0A08 (0), 0x400E0C08 (1)

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | – | – | – |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | – | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | FLERR | FLOCKE | FCMDE | FRDY |

- **FRDY: Flash Ready Status (cleared when Flash is busy)**

0: The EEFC is busy.

1: The EEFC is ready to start a new command.

When set, this flag triggers an interrupt if the FRDY flag is set in EEFC_FMR.

This flag is automatically cleared when the EEFC is busy.

- **FCMDE: Flash Command Error Status (cleared on read or by writing EEFC_FCR)**

0: No invalid commands and no bad keywords were written in EEFC_FMR.

1: An invalid command and/or a bad keyword was/were written in EEFC_FMR.

- **FLOCKE: Flash Lock Error Status (cleared on read)**

0: No programming/erase of at least one locked region has happened since the last read of EEFC_FSR.

1: Programming/erase of at least one locked region has happened since the last read of EEFC_FSR.

This flag is automatically cleared when EEFC_FSR is read or EEFC_FCR is written.

- **FLERR: Flash Error Status (cleared when a programming operation starts)**

0: No Flash memory error occurred at the end of programming (EraseVerify or WriteVerify test has passed).

1: A Flash memory error occurred at the end of programming (EraseVerify or WriteVerify test has failed).

### 29.17.15PMC Interrupt Disable Register

**Name:** PMC_IDR

**Address:** 0x400E0464

**Access:** Write-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | CFDEV | MOSCRCS | MOSCSELS |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | PCKRDY2 | PCKRDY1 | PCKRDY0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | MCKRDY | LOCKB | LOCKA | MOSCXTS |

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Disables the corresponding interrupt.

- **MOSCXTS: Main Crystal Oscillator Status Interrupt Disable**
- **LOCKA: PLLA Lock Interrupt Disable**
- **LOCKB: PLLB Lock Interrupt Disable**
- **MCKRDY: Master Clock Ready Interrupt Disable**
- **PCKRDYx: Programmable Clock Ready x Interrupt Disable**
- **MOSCSELS: Main Oscillator Selection Status Interrupt Disable**
- **MOSCRCS: Main On-Chip RC Status Interrupt Disable**
- **CFDEV: Clock Failure Detector Event Interrupt Disable**

### 31.6.10 PIO Set Output Data Register

**Name:** PIO_SODR

**Address:** 0x400E0E30 (PIOA), 0x400E1030 (PIOB), 0x400E1230 (PIOC)

**Access:** Write-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| P31 | P30 | P29 | P28 | P27 | P26 | P25 | P24 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

- **P0–P31: Set Output Data**

0: No effect.

1: Sets the data to be driven on the I/O line.

### 31.6.43 PIO Rising Edge/High-Level Select Register

**Name:** PIO_REHLSR

**Address:** 0x400E0ED4 (PIOA), 0x400E10D4 (PIOB), 0x400E12D4 (PIOC)

**Access:** Write-only

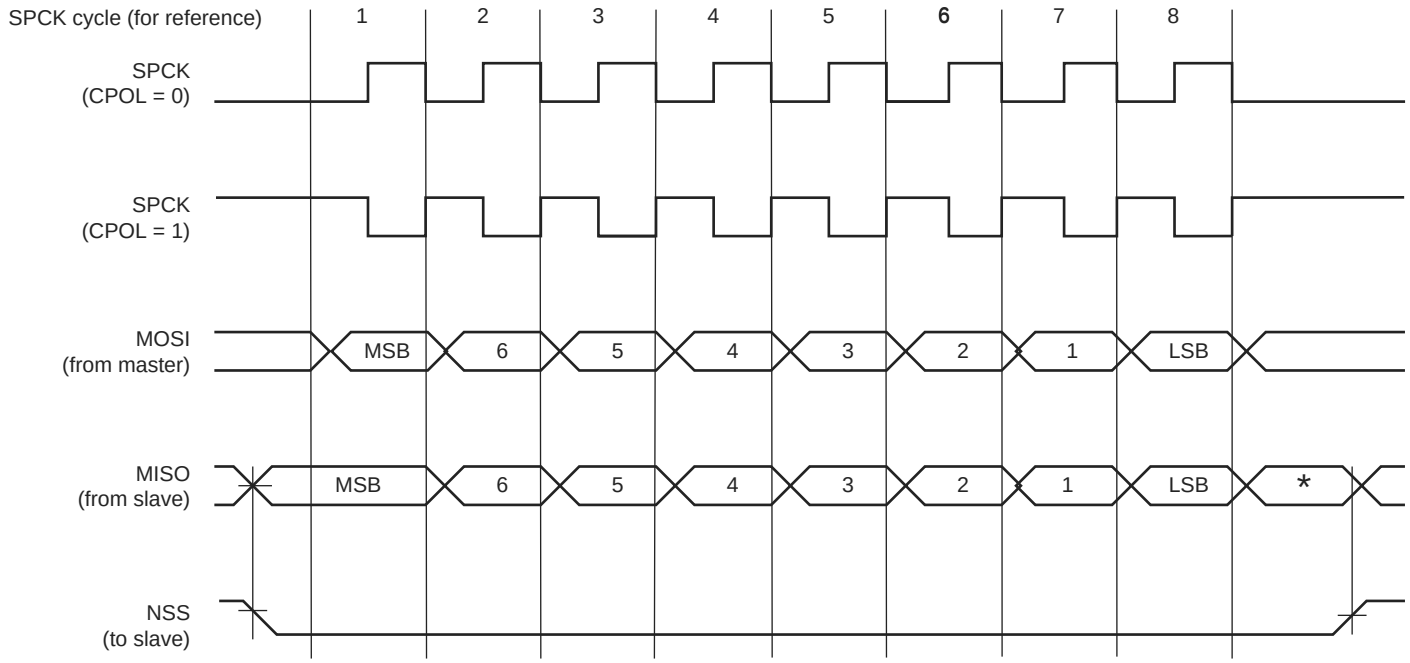
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| P31 | P30 | P29 | P28 | P27 | P26 | P25 | P24 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

- **P0–P31: Rising Edge/High-Level Interrupt Selection**

0: No effect.

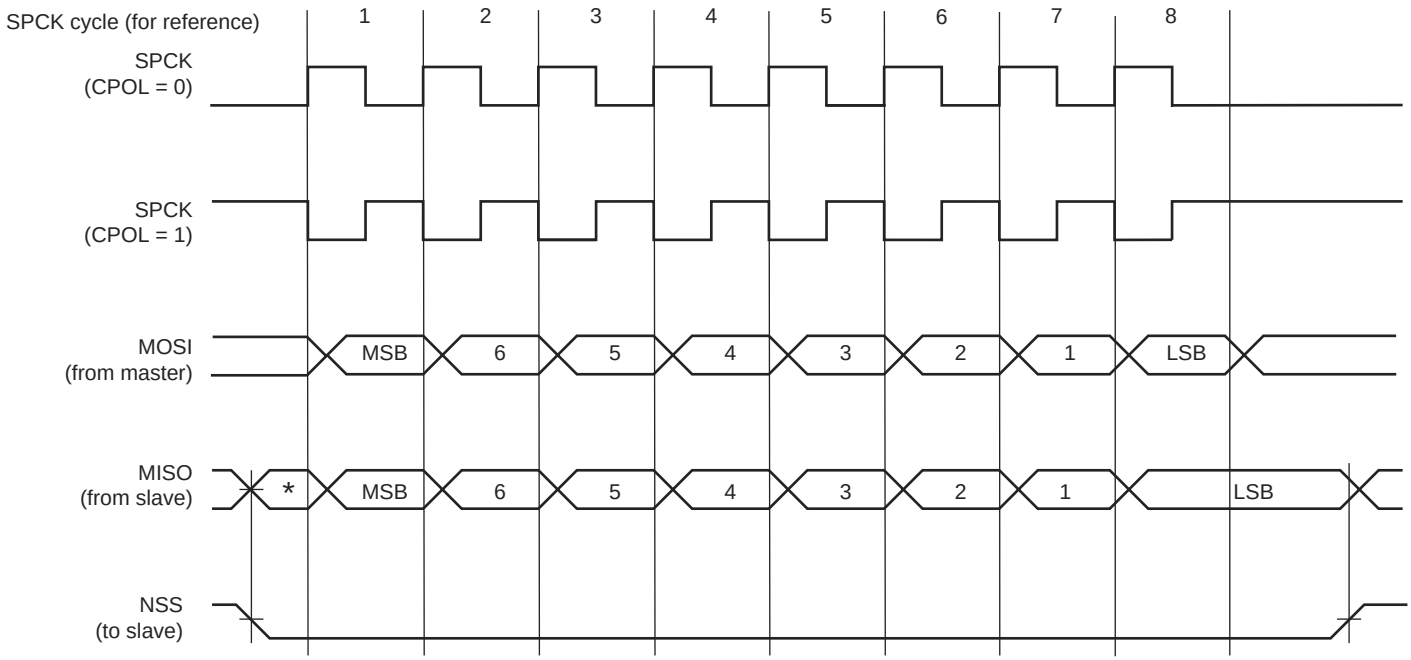
1: The interrupt source is set to a rising edge detection or high-level detection event, depending on PIO_ELSR.

**Figure 33-3. SPI Transfer Format (NCPHA = 1, 8 bits per transfer)**



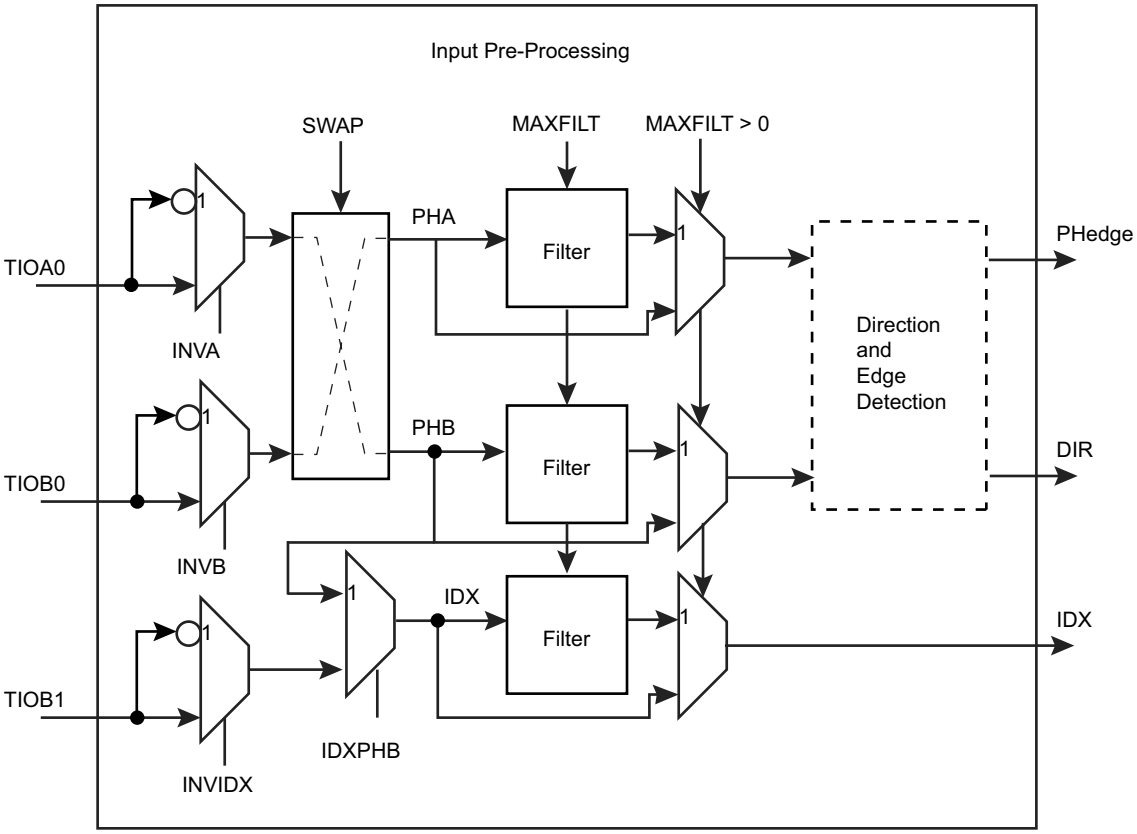

* Not defined.

**Figure 33-4. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)**




* Not defined.

**Figure 37-16. Input Stage**




Input filtering can efficiently remove spurious pulses that might be generated by the presence of particulate contamination on the optical or magnetic disk of the rotary sensor.

Spurious pulses can also occur in environments with high levels of electro-magnetic interference. Or, simply if vibration occurs even when rotation is fully stopped and the shaft of the motor is in such a position that the beginning of one of the reflective or magnetic bars on the rotary sensor disk is aligned with the light or magnetic (Hall) receiver cell of the rotary sensor. Any vibration can make the PHA, PHB signals toggle for a short duration.

### 38.14.13HSMCI Interrupt Enable Register

**Name:** HSMCI_IER

**Address:** 0x40000044

**Access:** Write-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| UNRE | OVRE | ACKRCVE | ACKRCV | XFRDONE | FIFOEMPTY | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CSTOE | DTOE | DCRCE | RTOE | RENDE | RCRCE | RDIRE | RINDE |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TXBUFE | RXBUFF | CSRCV | SDIOWAIT | – | – | – | SDIOIRQA |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ENDTX | ENDRX | NOTBUSY | DTIP | BLKE | TXRDY | RXRDY | CMDRDY |

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

- **CMDRDY: Command Ready Interrupt Enable**
- **RXRDY: Receiver Ready Interrupt Enable**
- **TXRDY: Transmit Ready Interrupt Enable**
- **BLKE: Data Block Ended Interrupt Enable**
- **DTIP: Data Transfer in Progress Interrupt Enable**
- **NOTBUSY: Data Not Busy Interrupt Enable**
- **ENDRX: End of Receive Buffer Interrupt Enable**
- **ENDTX: End of Transmit Buffer Interrupt Enable**
- **SDIOIRQA: SDIO Interrupt for Slot A Interrupt Enable**
- **SDIOWAIT: SDIO Read Wait Operation Status Interrupt Enable**
- **CSRCV: Completion Signal Received Interrupt Enable**
- **RXBUFF: Receive Buffer Full Interrupt Enable**
- **TXBUFE: Transmit Buffer Empty Interrupt Enable**
- **RINDE: Response Index Error Interrupt Enable**
- **RDIRE: Response Direction Error Interrupt Enable**
- **RCRCE: Response CRC Error Interrupt Enable**
- **RENDE: Response End Bit Error Interrupt Enable**

After a reset of the PWM controller, DIVA (DIVB) and PREA (PREB) are set to ‘0’. This implies that after reset clkA (clkB) are turned off.

At reset, all clocks provided by the modulo n counter are turned off except the peripheral clock. This situation is also true when the PWM peripheral clock is turned off through the Power Management Controller.

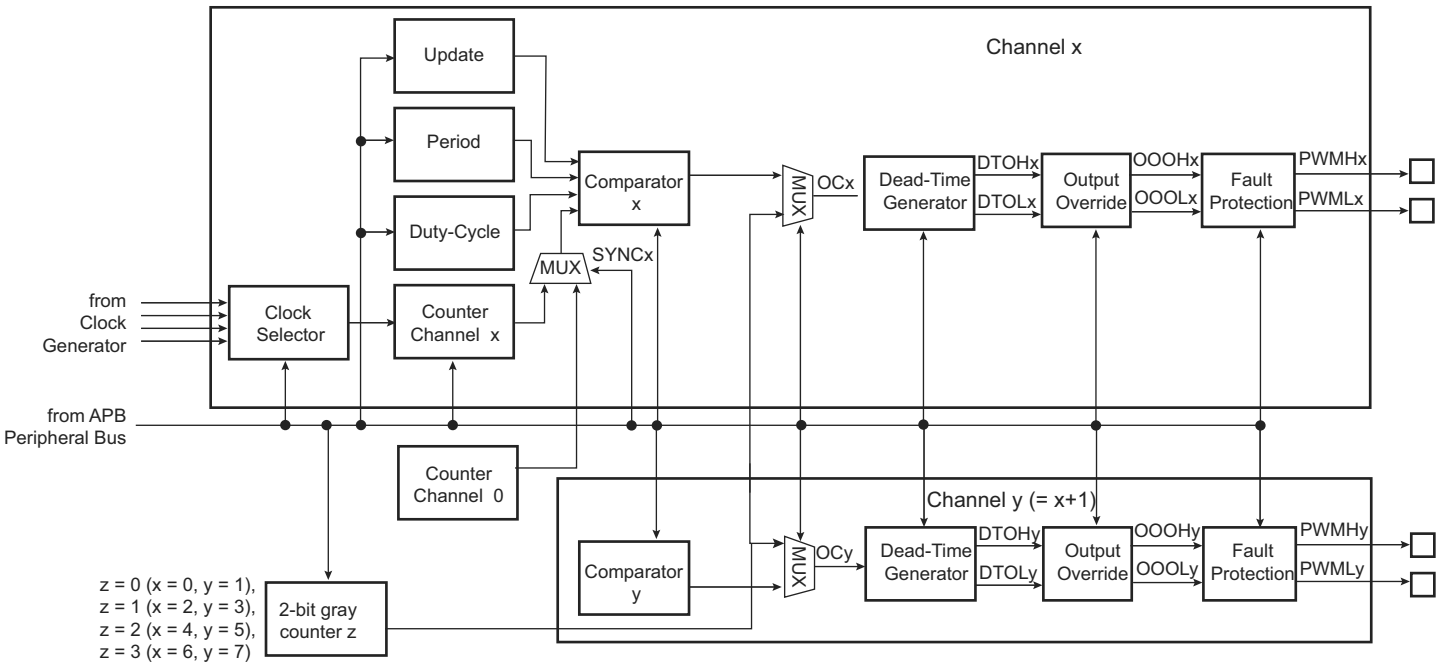
**CAUTION**:

Before using the PWM controller, the programmer must first enable the peripheral clock in the Power Management Controller (PMC).

### 39.6.2 PWM Channel

#### 39.6.2.1 Channel Block Diagram

**Figure 39-3. Functional View of the Channel Block Diagram**




Each of the 4 channels is composed of six blocks:

- A clock selector which selects one of the clocks provided by the clock generator (described in Section 39.6.1 “PWM Clock Generator”).
- A counter clocked by the output of the clock selector. This counter is incremented or decremented according to the channel configuration and comparators matches. The size of the counter is 16 bits.
- A comparator used to compute the OCx output waveform according to the counter value and the configuration. The counter value can be the one of the channel counter or the one of the channel 0 counter according to SYNCx bit in the PWM Sync Channels Mode Register (PWM_SCM).
- A 2-bit configurable gray counter enables the stepper motor driver. One gray counter drives 2 channels.
- A dead-time generator providing two complementary outputs (DTOHx/DTOLx) which allows to drive external power control switches safely.
- An output override block that can force the two complementary outputs to a programmed value (OOOHx/OOOLx).
- An asynchronous fault protection mechanism that has the highest priority to override the two complementary outputs (PWMHx/PWMLx) in case of fault detection (outputs forced to ‘0’, ‘1’).

### 39.7.43 PWM Channel Dead Time Update Register

**Name:** PWM_DTUPDx [x=0..3]

**Address:** 0x4002021C [0], 0x4002023C [1], 0x4002025C [2], 0x4002027C [3]

**Access:** Write-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| DTLUPD | | | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| DTLUPD | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DTHUPD | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTHUPD | | | | | | | |

This register can only be written if bits WPSWS4 and WPHWS4 are cleared in the PWM Write Protection Status Register.

This register acts as a double buffer for the DTH and DTL values. This prevents an unexpected waveform when modifying the dead-time values.

Only the first 12 bits (dead-time counter size) of fields DTHUPD and DTLUPD are significant.

- **DTHUPD: Dead-Time Value Update for PWMHx Output**

Defines the dead-time value for PWMHx output. This value must be defined between 0 and the value (CPRD – CDTY) (PWM_CPRDx and PWM_CDTYx). This value is applied only at the beginning of the next channel x PWM period.

- **DTLUPD: Dead-Time Value Update for PWMLx Output**

Defines the dead-time value for PWMLx output. This value must be defined between 0 and CDTY (PWM_CDTYx). This value is applied only at the beginning of the next channel x PWM period.

This flag is used to generate a Data IN transaction (device to host). Device firmware checks that it can write a data payload in the FIFO, checking that TXPKTRDY is cleared. Transfer to the FIFO is done by writing in the UDP_FDRx. Once the data payload has been transferred to the FIFO, the firmware notifies the USB device setting TXPKTRDY to one. USB bus transactions can start. TXCOMP is set once the data payload has been received by the host.

After setting or clearing this bit, a wait time of 3 UDPCK clock cycles and 3 peripheral clock cycles is required before accessing DPR.

- **FORCESTALL: Force Stall (used by Control, Bulk and Isochronous Endpoints)**

Read:

0: Normal state

1: Stall state

Write:

0: Return to normal state

1: Send STALL to the host

Refer to chapters 8.4.5 and 9.4.5 of the *Universal Serial Bus Specification, Rev. 2.0* for more information on the STALL handshake.

Control endpoints: During the data stage and status stage, this bit indicates that the microcontroller cannot complete the request.

Bulk and interrupt endpoints: This bit notifies the host that the endpoint is halted.

The host acknowledges the STALL, device firmware is notified by the STALLSENT flag.

- **RX_DATA_BK1: Receive Data Bank 1 (only used by endpoints with ping-pong attributes)**

This flag generates an interrupt while it is set to one.

Write (cleared by the firmware):

0: Notifies USB device that data have been read in the FIFO's Bank 1.

1: To leave the read value unchanged.

Read (Set by the USB peripheral):

0: No data packet has been received in the FIFO's Bank 1.

1: A data packet has been received, it has been stored in FIFO's Bank 1.

When the device firmware has polled this bit or has been interrupted by this signal, it must transfer data from the FIFO to microcontroller memory. The number of bytes received is available in RXBYTECNT field. Bank 1 FIFO values are read through UDP_FDRx. Once a transfer is done, the device firmware must release Bank 1 to the USB device by clearing RX_DATA_BK1.

After setting or clearing this bit, a wait time of 3 UDPCK clock cycles and 3 peripheral clock cycles is required before accessing DPR.

- **DIR: Transfer Direction (only available for control endpoints) (Read/Write)**

0: Allows Data OUT transactions in the control data stage.

1: Enables Data IN transactions in the control data stage.

Refer to Chapter 8.5.3 of the *Universal Serial Bus Specification, Rev. 2.0* for more information on the control data stage.

This bit must be set before UDP_CSRx/RXSETUP is cleared at the end of the setup stage. According to the request sent in the setup data packet, the data stage is either a device to host (DIR = 1) or host to device (DIR = 0) data transfer. It is not necessary to check this bit to reverse direction for the status stage.

The sequence can be customized by programming the Sequence Channel Registers ADC_SEQR1 and ADC_SEQR2 and setting the USEQ bit of the Mode Register (ADC_MR). The user can choose a specific order of channels and can program up to 16 conversions by sequence. The user is free to create a personal sequence by writing channel numbers in ADC_SEQR1 and ADC_SEQR2. Not only can channel numbers be written in any sequence, channel numbers can be repeated several times. When the bit USEQ in ADC_MR is set, the fields USCHx in ADC_SEQR1 and ADC_SEQR2 are used to define the sequence. Only enabled USCHx fields will be part of the sequence. Each USCHx field has a corresponding enable, CHx, in ADC_CHER (USCHx field with the lowest x index is associated with bit CHx of the lowest index).

If all ADC channels (i.e., 16) are used on an application board, there is no restriction of usage of the user sequence. However, if some ADC channels are not enabled for conversion but rather used as pure digital inputs, the respective indexes of these channels cannot be used in the user sequence fields (see ADC_SEQRx). For example, if channel 4 is disabled (ADC_CSR[4] = 0), ADC_SEQRx fields USCH1 up to USCH16 must not contain the value 4. Thus the length of the user sequence may be limited by this behavior.

As an example, if only four channels over 16 (CH0 up to CH3) are selected for ADC conversions, the user sequence length cannot exceed four channels. Each trigger event may launch up to four successive conversions of any combination of channels 0 up to 3 but no more (i.e., in this case the sequence CH0, CH0, CH1, CH1, CH1 is impossible).

A sequence that repeats the same channel several times requires more enabled channels than channels actually used for conversion. For example, the sequence CH0, CH0, CH1, CH1 requires four enabled channels (four free channels on application boards) whereas only CH0, CH1 are really converted.

Note: The reference voltage pins always remain connected in Normal mode as in Sleep mode.

### 42.6.8 Comparison Window

The ADC Controller features automatic comparison functions. It compares converted values to a low threshold, a high threshold or both, depending on the value of the CMPMODE bit in ADC_EMR. The comparison can be done on all channels or only on the channel specified in the CMPSEL field of ADC_EMR. To compare all channels, the CMPALL bit of ADC_EMR must be set.

The flag can be read on the COMPE bit of the Interrupt Status register (ADC_ISR) and can trigger an interrupt.

The high threshold and the low threshold can be read/write in the Compare Window register (ADC_CWR).

### 42.6.9 Differential Inputs

The ADC can be used either as a single-ended ADC (DIFF bit = 0 in ADC_COR) or as a fully differential ADC (DIFF bit = 1 in ADC_COR) as shown in Figure 42-7. By default, after a reset, the ADC is in Single-ended mode.

If ANACH is set in ADC_MR, the ADC can apply a different mode on each channel. Otherwise the parameters of CH0 are applied to all channels.

The same inputs are used in Single-ended or Differential mode.

In Single-ended mode, inputs are managed by a 16:1-channel analog multiplexer. In Fully Differential mode, inputs are managed by an 8:1-channel analog multiplexer. See Table 42-4.

**Table 42-4. Input Pins and Channel Numbers**

| Input Pin | Channel Number | |
|---|---|---|
| | Single-ended Mode | Differential Mode |
| AD0 | CH0 | CH0 |
| AD1 | CH1 | |
| AD2 | CH2 | CH1 |
| AD3 | CH3 | |

- **FREERUN: Free Run Mode**

| Value | Name | Description |
|---|---|---|
| 0 | OFF | Normal Mode |
| 1 | ON | Free Run Mode: Never wait for any trigger. |

- **PRESCAL: Prescaler Rate Selection**

PRESCAL = ($f_{peripheral\ clock}$ / ($2 \times f_{ADCCLK}$)) – 1.

- **STARTUP: Startup Time**

| Value | Name | Description |
|---|---|---|
| 0 | SUT0 | 0 periods of ADCCLK |
| 1 | SUT8 | 8 periods of ADCCLK |
| 2 | SUT16 | 16 periods of ADCCLK |
| 3 | SUT24 | 24 periods of ADCCLK |
| 4 | SUT64 | 64 periods of ADCCLK |
| 5 | SUT80 | 80 periods of ADCCLK |
| 6 | SUT96 | 96 periods of ADCCLK |
| 7 | SUT112 | 112 periods of ADCCLK |
| 8 | SUT512 | 512 periods of ADCCLK |
| 9 | SUT576 | 576 periods of ADCCLK |
| 10 | SUT640 | 640 periods of ADCCLK |
| 11 | SUT704 | 704 periods of ADCCLK |
| 12 | SUT768 | 768 periods of ADCCLK |
| 13 | SUT832 | 832 periods of ADCCLK |
| 14 | SUT896 | 896 periods of ADCCLK |
| 15 | SUT960 | 960 periods of ADCCLK |

- **SETTLING: Analog Settling Time**

| Value | Name | Description |
|---|---|---|
| 0 | AST3 | 3 periods of ADCCLK |
| 1 | AST5 | 5 periods of ADCCLK |
| 2 | AST9 | 9 periods of ADCCLK |
| 3 | AST17 | 17 periods of ADCCLK |

- **ANACH: Analog Change**

| Value | Name | Description |
|---|---|---|
| 0 | NONE | No analog change on channel switching: DIFF0, GAIN0 and OFF0 are used for all channels. |
| 1 | ALLOWED | Allows different analog settings for each channel. See ADC_CGR and ADC_COR registers. |

- **TRACKTIM: Tracking Time**

Tracking Time = (TRACKTIM + 1) × ADCCLK periods

### 42.7.21 ADC Write Protection Status Register

**Name:** ADC_WPSR

**Address:** 0x400380E8

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WPVSRC | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| WPVSRC | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | – | – | – | WPVS |

- **WPVS: Write Protection Violation Status**

0: No write protection violation has occurred since the last read of the ADC_WPSR.

1: A write protection violation has occurred since the last read of the ADC_WPSR. If this violation is an unauthorized attempt to write a protected register, the associated violation is reported into field WPVSRC.

- **WPVSRC: Write Protection Violation Source**

When WPVS = 1, WPVSRC indicates the register address offset at which a write access has been attempted.

**Table 44-4. 1.2V Voltage Regulator Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDIN}$ | DC Input Voltage | (4) | 1.6 | 3.3 | 3.6 | V |
| $V_{DDOUT}$ | DC Output Voltage | Normal Mode | – | 1.2 | – | V |
| | | Standby Mode | – | 0 | – | |
| $V_{O(accuracy)}$ | Output Voltage Accuracy | $I_{LOAD}$ = 0.8mA to 80mA (after trimming) | -3 | | 3 | % |
| $I_{LOAD}$ | Maximum DC Output Current | $V_{DDIN}$ > 1.8V | – | – | 80 | mA |
| | | $V_{DDIN} \leq$ 1.8V | – | – | 40 | |
| $I_{LOAD-START}$ | Maximum Peak Current during Startup | (3) | – | – | 400 | |
| $V_{DROPOUT}$ | Dropout Voltage | $V_{DDIN}$ = 1.6V, $I_{LOAD}$ = Max | – | 400 | – | mV |
| $V_{LINE}$ | Line Regulation | $V_{DDIN}$ from 2.7V to 3.6V; $I_{LOAD}$ MAX | – | 10 | 30 | mV |
| $V_{LINE-TR}$ | Transient Line Regulation | $V_{DDIN}$ from 2.7V to 3.6V; $t_r = t_f$ = 5µs; $I_{LOAD}$ Max | – | 50 | 150 | |
| $V_{LOAD}$ | Load Regulation | $V_{DDIN} \geq$ 1.8V; $I_{LOAD}$ = 10% to 90% MAX | – | 20 | 40 | mV |
| $V_{LOAD-TR}$ | Transient Load Regulation | $V_{DDIN} \geq$ 1.8V; $I_{LOAD}$ = 10% to 90% MAX; $t_r = t_f$ = 5 µs | – | 50 | 150 | mV |
| $I_Q$ | Quiescent Current | Normal Mode, $I_{LOAD}$ = 0 mA | – | 5 | – | µA |
| | | Normal Mode, $I_{LOAD}$ = 80 mA | – | 500 | – | |
| | | Standby Mode | – | 500 | 1 | |
| $CD_{IN}$ | Input Decoupling Capacitor | (1) | – | 4.7 | – | µF |
| $CD_{OUT}$ | Output Decoupling Capacitor | (2) | 1.85 | 2.2 | 5.9 | µF |
| | | ESR | 0.1 | | 10 | Ω |
| $t_{on}$ | Turn-on Time | $CD_{OUT}$ = 2.2µF, $V_{DDOUT}$ reaches 1.2V (± 3%) | – | 300 | – | µs |
| $t_{off}$ | Turn-off Time | $CD_{OUT}$ = 2.2µF | – | – | 40 | ms |

Notes:
1. A 4.7µF or higher ceramic capacitor must be connected between VDDIN and the closest GND pin of the device. This large decoupling capacitor is mandatory to reduce startup current, improving transient response and noise rejection.
2. To ensure stability, an external 2.2 µF output capacitor, $CD_{OUT}$ must be connected between the VDDOUT and the closest GND pin of the device. The ESR (Equivalent Series Resistance) of the capacitor must be in the range 0.1 to 10 Ω. Solid tantalum, and multilayer ceramic capacitors are all suitable as output capacitor. A 100 nF bypass capacitor between VDDOUT and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Defined as the current needed to charge external bypass/decoupling capacitor network.
4. See Section 5.2.2 “VDDIO Versus VDDIN”