**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, POR, PWM, WDT |
| Number of I/O | 47 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 64K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.62V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsam4s2bb-an |

Before programming SCB_VTOR to relocate the vector table, ensure that the vector table entries of the new vector table are set up for fault handlers, NMI and all enabled exception like interrupts. For more information, see the “Vector Table Offset Register” .

#### 12.8.2.1 NVIC Programming Hints

The software uses the CPSIE I and CPSID I instructions to enable and disable the interrupts. The CMSIS provides the following intrinsic functions for these instructions:

void __disable_irq(void) // Disable Interrupts

void __enable_irq(void) // Enable Interrupts

In addition, the CMSIS provides a number of functions for NVIC control, including:

**Table 12-29. CMSIS Functions for NVIC Control**

| CMSIS Interrupt Control Function | Description |
|---|---|
| void NVIC_SetPriorityGrouping(uint32_t priority_grouping) | Set the priority grouping |
| void NVIC_EnableIRQ(IRQn_t IRQn) | Enable IRQn |
| void NVIC_DisableIRQ(IRQn_t IRQn) | Disable IRQn |
| uint32_t NVIC_GetPendingIRQ (IRQn_t IRQn) | Return true (IRQ-Number) if IRQn is pending |
| void NVIC_SetPendingIRQ (IRQn_t IRQn) | Set IRQn pending |
| void NVIC_ClearPendingIRQ (IRQn_t IRQn) | Clear IRQn pending status |
| uint32_t NVIC_GetActive (IRQn_t IRQn) | Return the IRQ number of the active interrupt |
| void NVIC_SetPriority (IRQn_t IRQn, uint32_t priority) | Set priority for IRQn |
| uint32_t NVIC_GetPriority (IRQn_t IRQn) | Read priority of IRQn |
| void NVIC_SystemReset (void) | Reset the system |

The input parameter IRQn is the IRQ number. For more information about these functions, see the CMSIS documentation.

To improve software efficiency, the CMSIS simplifies the NVIC register presentation. In the CMSIS:

- The Set-enable, Clear-enable, Set-pending, Clear-pending and Active Bit registers map to arrays of 32-bit integers, so that:
  - The array ISER[0] to ISER[1] corresponds to the registers ISER0–ISER1
  - The array ICER[0] to ICER[1] corresponds to the registers ICER0–ICER1
  - The array ISPR[0] to ISPR[1] corresponds to the registers ISPR0–ISPR1
  - The array ICPR[0] to ICPR[1] corresponds to the registers ICPR0–ICPR1
  - The array IABR[0] to IABR[1] corresponds to the registers IABR0–IABR1
- The Interrupt Priority Registers (IPR0–IPR ) provide an 8-bit priority field for each interrupt and each register holds four priority fields.

The CMSIS provides thread-safe code that gives atomic access to the Interrupt Priority Registers. Table 12-30 shows how the interrupts, or IRQ numbers, map onto the interrupt registers and corresponding CMSIS variables that have one bit per interrupt.

**Table 12-30. Mapping of Interrupts**

| | CMSIS Array Elements(1) | | | | |
|---|---|---|---|---|---|
| Interrupts | Set-enable | Clear-enable | Set-pending | Clear-pending | Active Bit |
| 0–31 | ISER[0] | ICER[0] | ISPR[0] | ICPR[0] | IABR[0] |
| 32–35 | ISER[1] | ICER[1] | ISPR[1] | ICPR[1] | IABR[1] |

#### 12.9.1.11 System Handler Priority Register 3

**Name:** SCB_SHPR3

**Access:** Read/Write

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| PRI_15 | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRI_14 | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | – | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | – | – | – | – |

- **PRI_15: Priority**

Priority of system handler 15, SysTick exception.

- **PRI_14: Priority**

Priority of system handler 14, PendSV.

# 16. Real-time Clock (RTC)

## 16.1 Description

The Real-time Clock (RTC) peripheral is designed for very low power consumption. For optimal functionality, the RTC requires an accurate external 32.768 kHz clock, which can be provided by a crystal oscillator.

It combines a complete time-of-day clock with alarm and a Gregorian or Persian calendar, complemented by a programmable periodic interrupt. The alarm and calendar registers are accessed by a 32-bit data bus.

The time and calendar values are coded in binary-coded decimal (BCD) format. The time format can be 24-hour mode or 12-hour mode with an AM/PM indicator.

Updating time and calendar fields and configuring the alarm fields are performed by a parallel capture on the 32-bit data bus. An entry control is performed to avoid loading registers with incompatible BCD format data or with an incompatible date according to the current month/year/century.

A clock divider calibration circuitry can be used to compensate for crystal oscillator frequency inaccuracy.

An RTC output can be programmed to generate several waveforms, including a prescaled clock derived from 32.768 kHz.

## 16.2 Embedded Characteristics

- Ultra Low Power Consumption
- Full Asynchronous Design
- Gregorian Calendar up to 2099 or Persian Calendar
- Programmable Periodic Interrupt
- Safety/security features:
  - Valid Time and Date Programmation Check
  - On-The-Fly Time and Date Validity Check
- Crystal Oscillator Clock Calibration
- Waveform Generation
- Register Write Protection

# 18. Supply Controller (SUPC)

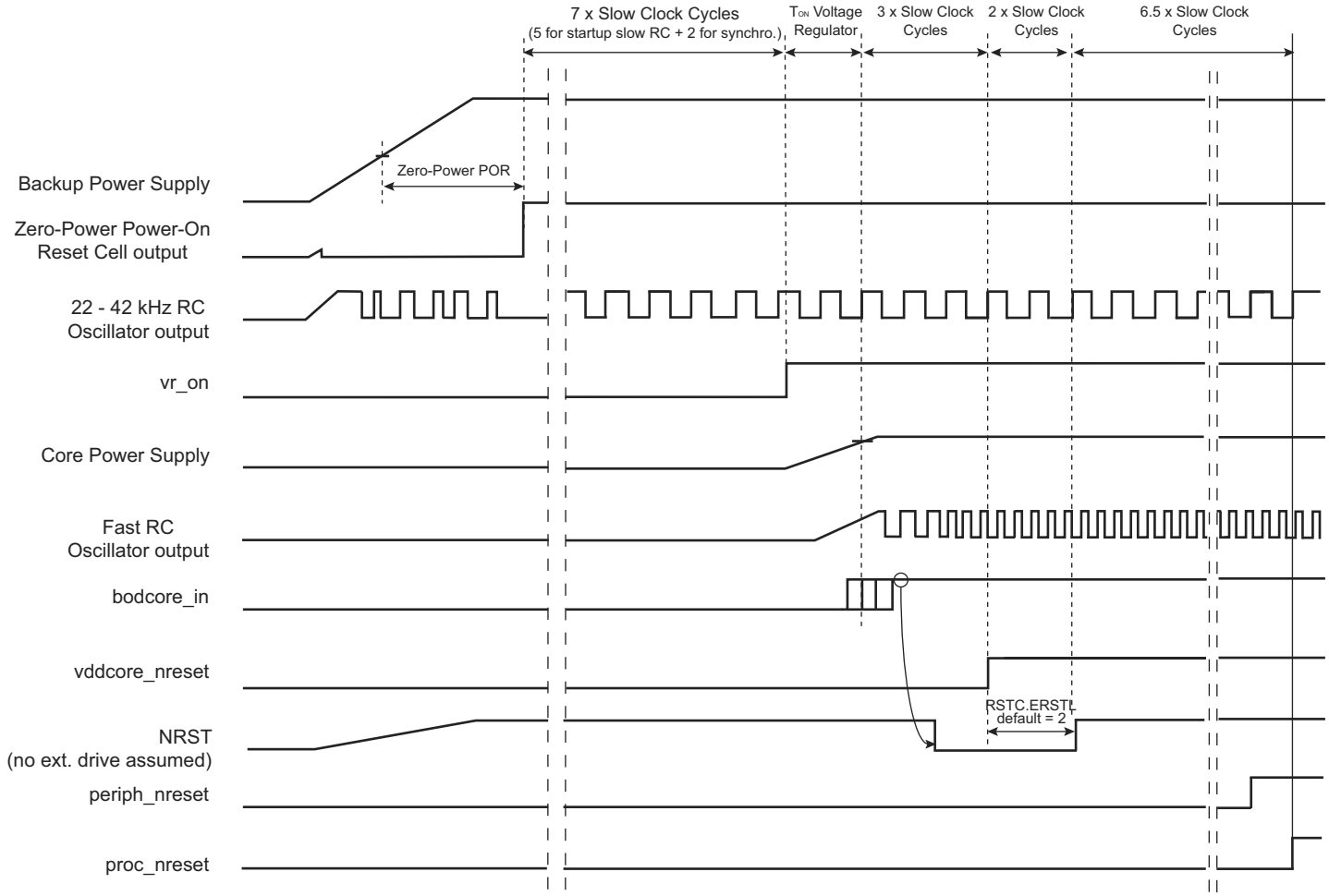
## 18.1 Description

The Supply Controller (SUPC) controls the supply voltages of the system and manages the Backup mode. In this mode, current consumption is reduced to a few microamps for backup power retention. Exit from this mode is possible on multiple wake-up sources. The SUPC also generates the slow clock by selecting either the low-power RC oscillator or the low-power crystal oscillator.

## 18.2 Embedded Characteristics

- Manages the Core Power Supply VDDCORE and Backup Mode by Controlling the Embedded Voltage Regulator
- A Supply Monitor Detection on VDDIO or a Brownout Detection on VDDCORE Triggers a Core Reset
- Generates the Slow Clock SLCK by Selecting Either the 22-42 kHz Low-Power RC Oscillator or the 32 kHz Low-Power Crystal Oscillator
- Low-power Tamper Detection on Two Inputs
- Anti-tampering by Immediate Clear of the General-purpose Backup Registers
- Supports Multiple Wake-up Sources for Exit from Backup Mode
  - 16 Wake-up Inputs with Programmable Debouncing
  - Real-Time Clock Alarm
  - Real-Time Timer Alarm
  - Supply Monitor Detection on VDDIO, with Programmable Scan Period and Voltage Threshold

**Figure 18-3. Raising the VDDIO Power Supply**




Note: After “proc_nreset” rising, the core starts fetching instructions from Flash at 4 MHz.

### 18.4.6 Core Reset

The Supply Controller manages the vddcore_nreset signal to the Reset Controller, as described in Section 18.4.5 ”Backup Power Supply Reset”. The vddcore_nreset signal is normally asserted before shutting down the core power supply and released as soon as the core power supply is correctly regulated.

There are two additional sources which can be programmed to activate vddcore_nreset:

- a supply monitor detection
- a brownout detection

#### 18.4.6.1 Supply Monitor Reset

The supply monitor is capable of generating a reset of the system. This is enabled by setting the SMRSTEN bit in SUPC_SMMR.

If SMRSTEN is set and if a supply monitor detection occurs, the vddcore_nreset signal is immediately activated for a minimum of one slow clock cycle.

#### 18.4.6.2 Brownout Detector Reset

The brownout detector provides the bodcore_in signal to the SUPC. This signal indicates that the voltage regulation is operating as programmed. If this signal is lost for longer than 1 slow clock period while the voltage regulator is enabled, the SUPC asserts vddcore_nreset if BODRSTEN is written to 1 in SUPC_MR.

# 23. Cyclic Redundancy Check Calculation Unit (CRCCU)

## 23.1 Description

The Cyclic Redundancy Check Calculation Unit (CRCCU) has its own DMA which functions as a Master with the Bus Matrix. Three different polynomials are available: CCITT802.3, CASTAGNOLI and CCITT16.

The CRCCU is designed to perform data integrity checks of off-/on-chip memories as a background task without CPU intervention.

## 23.2 Embedded Characteristics

- Data Integrity Check of Off-/On-Chip Memories
- Background Task Without CPU Intervention
- Performs Cyclic Redundancy Check (CRC) Operation on Programmable Memory Area
- Programmable Bus Burden

Note: The CRCCU is designed to verify data integrity of off-/on-chip memories, thus the CRC must be generated and verified by the CRCCU. The CRCCU performs the CRC from LSB to MSB. If the CRC has been performed with the same polynomial by another device, a bit-reverse must be done on each byte before using the CRCCU.

## 23.6 Transfer Control Registers Memory Mapping

**Table 23-2. Transfer Control Register Memory Mapping**

| Offset | Register | Name | Access | Reset |
|---|---|---|---|---|
| CRCCU_DSCR + 0x0 | CRCCU Transfer Address Register | TR_ADDR | Read/Write | 0x00000000 |
| CRCCU_DSCR + 0x4 | CRCCU Transfer Control Register | TR_CTRL | Read/Write | 0x00000000 |
| CRCCU_DSCR + 0xC–0x10 | Reserved | – | – | – |
| CRCCU_DSCR+0x10 | CRCCU Transfer Reference Register | TR_CRC | Read/Write | 0x00000000 |

Note: These registers are memory mapped.

### 31.6.23 PIO Pull-Up Status Register

**Name:** PIO_PUSR

**Address:** 0x400E0E68 (PIOA), 0x400E1068 (PIOB), 0x400E1268 (PIOC)

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| P31 | P30 | P29 | P28 | P27 | P26 | P25 | P24 |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| P23 | P22 | P21 | P20 | P19 | P18 | P17 | P16 |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

- **P0–P31: Pull-Up Status**

0: Pull-up resistor is enabled on the I/O line.

1: Pull-up resistor is disabled on the I/O line.

- **CKG: Receive Clock Gating Selection**

| Value | Name | Description |
|---|---|---|
| 0 | CONTINUOUS | None |
| 1 | EN_RF_LOW | Receive Clock enabled only if RF Low |
| 2 | EN_RF_HIGH | Receive Clock enabled only if RF High |

- **START: Receive Start Selection**

| Value | Name | Description |
|---|---|---|
| 0 | CONTINUOUS | Continuous, as soon as the receiver is enabled, and immediately after the end of transfer of the previous data. |
| 1 | TRANSMIT | Transmit start |
| 2 | RF_LOW | Detection of a low level on RF signal |
| 3 | RF_HIGH | Detection of a high level on RF signal |
| 4 | RF_FALLING | Detection of a falling edge on RF signal |
| 5 | RF_RISING | Detection of a rising edge on RF signal |
| 6 | RF_LEVEL | Detection of any level change on RF signal |
| 7 | RF_EDGE | Detection of any edge on RF signal |
| 8 | CMP_0 | Compare 0 |

- **STOP: Receive Stop Selection**

0: After completion of a data transfer when starting with a Compare 0, the receiver stops the data transfer and waits for a new compare 0.

1: After starting a receive with a Compare 0, the receiver operates in a continuous mode until a Compare 1 is detected.

- **STTDLY: Receive Start Delay**

If STTDLY is not 0, a delay of STTDLY clock cycles is inserted between the start event and the actual start of reception. When the Receiver is programmed to start synchronously with the Transmitter, the delay is also applied.

Note: It is very important that STTDLY be set carefully. If STTDLY must be set, it should be done in relation to TAG (Receive Sync Data) reception.

- **PERIOD: Receive Period Divider Selection**

This field selects the divider to apply to the selected Receive Clock in order to generate a new Frame Sync Signal. If 0, no PERIOD signal is generated. If not 0, a PERIOD signal is generated each 2 x (PERIOD + 1) Receive Clock.

### 32.9.8 SSC Transmit Holding Register

**Name:** SSC_THR

**Address:** 0x40004024

**Access:** Write-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| TDAT | | | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| TDAT | | | | | | | |

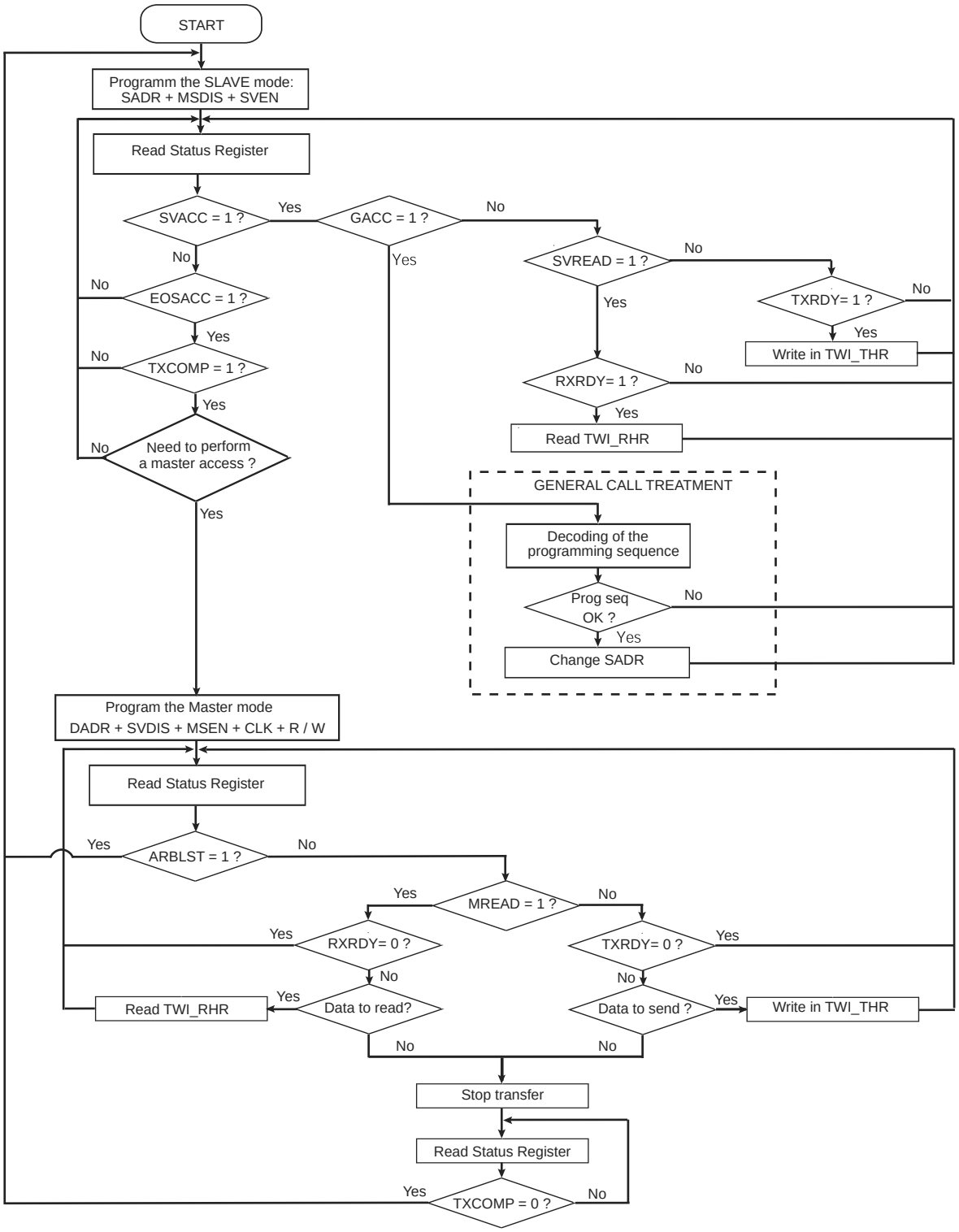
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TDAT | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TDAT | | | | | | | |

- **TDAT: Transmit Data**

Right aligned regardless of the number of data bits defined by DATLEN in SSC_TFMR.

**Figure 34-22. Multi-master Flowchart**




## 34.7.5 Slave Mode

### 34.7.5.1 Definition

Slave mode is defined as a mode where the device receives the clock and the address from another device called the master.

### 35.6.5 UART Interrupt Mask Register

**Name:** UART_IMR

**Address:** 0x400E0610 (0), 0x400E0810 (1)

**Access:** Read-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | – | – | – |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | RXBUFF | TXBUFE | – | TXEMPTY | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PARE | FRAME | OVRE | ENDTX | ENDRX | – | TXRDY | RXRDY |

The following configuration values are valid for all listed bit names of this register:

0: The corresponding interrupt is disabled.

1: The corresponding interrupt is enabled.

- **RXRDY: Mask RXRDY Interrupt**
- **TXRDY: Disable TXRDY Interrupt**
- **ENDRX: Mask End of Receive Transfer Interrupt**
- **ENDTX: Mask End of Transmit Interrupt**
- **OVRE: Mask Overrun Error Interrupt**
- **FRAME: Mask Framing Error Interrupt**
- **PARE: Mask Parity Error Interrupt**
- **TXEMPTY: Mask TXEMPTY Interrupt**
- **TXBUFE: Mask TXBUFE Interrupt**
- **RXBUFF: Mask RXBUFF Interrupt**

### 37.7.16 TC QDEC Interrupt Disable Register

**Name:** TC_QIDR

**Address:** 0x400100CC (0), 0x400140CC (1)

**Access:** Write-only

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | – | – | – |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | – | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | – | QERR | DIRCHG | IDX |

- **IDX: Index**

0: No effect.

1: Disables the interrupt when a rising edge occurs on IDX input.

- **DIRCHG: Direction Change**

0: No effect.

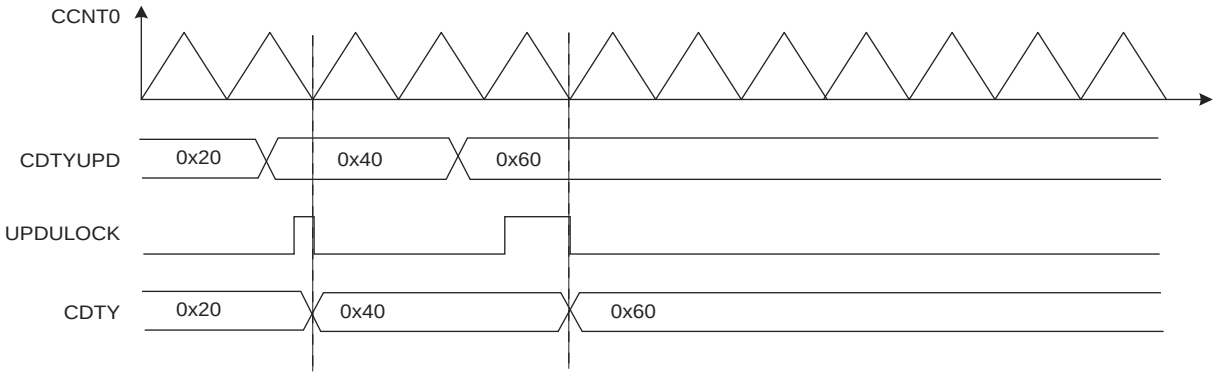
1: Disables the interrupt when a change on rotation direction is detected.

- **QERR: Quadrature Error**

0: No effect.

1: Disables the interrupt when a quadrature error occurs on PHA, PHB.

**Figure 39-10. Method 1 (UPDM = 0)**




**Method 2: Manual write of duty-cycle values and automatic trigger of the update**

In this mode, the update of the period value, the duty-cycle values, the dead-time values and the update period value must be done by writing in their respective update registers with the processor (respectively PWM_CPRDUPDx, PWM_CDTYUPDx, PWM_DTUPDx and PWM_SCUPUPD).

To trigger the update of the period value and the dead-time values, the user must use the bit UPDULOCK in the PWM_SCUC register, which updates synchronously (at the same PWM period) the synchronous channels:

- If the bit UPDULOCK is set to '1', the update is done at the next PWM period of the synchronous channels.
- If the UPDULOCK bit is not set to '1', the update is locked and cannot be performed.

After writing the UPDULOCK bit to '1', it is held at this value until the update occurs, then it is read 0.

The update of the duty-cycle values and the update period is triggered automatically after an update period.

To configure the automatic update, the user must define a value for the update period by the UPR field in the PWM_SCUP register. The PWM controller waits UPR+1 period of synchronous channels before updating automatically the duty values and the update period value.

The status of the duty-cycle value write is reported in the PWM Interrupt Status Register 2 (PWM_ISR2) by the following flags:

- WRDY: this flag is set to '1' when the PWM Controller is ready to receive new duty-cycle values and a new update period value. It is reset to '0' when the PWM_ISR2 register is read.

Depending on the interrupt mask in the PWM Interrupt Mask Register 2 (PWM_IMR2), an interrupt can be generated by these flags.

Sequence for Method 2:

1. Select the manual write of duty-cycle values and the automatic update by setting the field UPDM to '1' in the PWM_SCM register
2. Define the synchronous channels by the bits SYNCx in the PWM_SCM register.
3. Define the update period by the field UPR in the PWM_SCUP register.
4. Enable the synchronous channels by writing CHID0 in the PWM_ENA register.
5. If an update of the period value and/or of the dead-time values is required, write registers that need to be updated (PWM_CPRDUPDx, PWM_DTUPDx), else go to Step 8.
6. Set UPDULOCK to '1' in PWM_SCUC.
7. The update of these registers will occur at the beginning of the next PWM period. At this moment the bit UPDULOCK is reset, go to Step 5. for new values.
8. If an update of the duty-cycle values and/or the update period is required, check first that write of new update values is possible by polling the flag WRDY (or by waiting for the corresponding interrupt) in the PWM_ISR2.
9. Write registers that need to be updated (PWM_CDTYUPDx, PWM_SCUPUPD).

2. During the Status OUT stage, the host emits a zero length packet to the device (Data OUT transaction with no data).

### 40.6.2 Handling Transactions with USB 2.0 Device Peripheral

#### 40.6.2.1 Setup Transaction

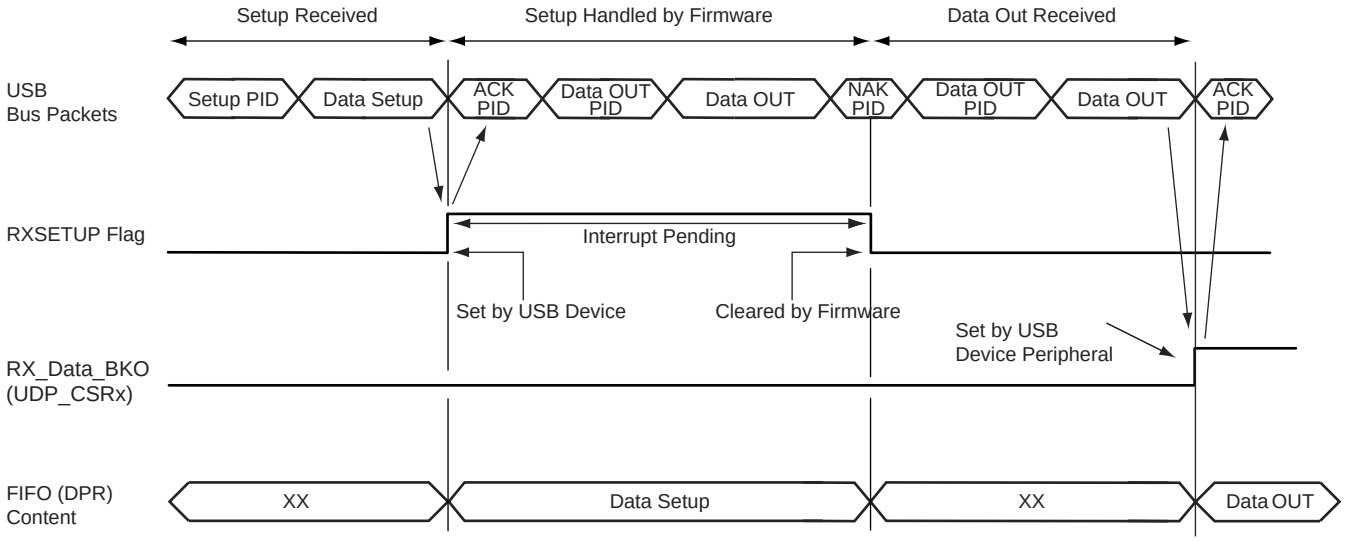
Setup is a special type of host-to-device transaction used during control transfers. Control transfers must be performed using endpoints with no ping-pong attributes. A setup transaction needs to be handled as soon as possible by the firmware. It is used to transmit requests from the host to the device. These requests are then handled by the USB device and may require more arguments. The arguments are sent to the device by a Data OUT transaction which follows the setup transaction. These requests may also return data. The data is carried out to the host by the next Data IN transaction which follows the setup transaction. A status transaction ends the control transfer.

When a setup transfer is received by the USB endpoint:

- The USB device automatically acknowledges the setup packet
- RXSETUP is set in the UDP_CSRx
- An endpoint interrupt is generated while the RXSETUP is not cleared. This interrupt is carried out to the microcontroller if interrupts are enabled for this endpoint.

Thus, firmware must detect the RXSETUP polling the UDP_CSRx or catching an interrupt, read the setup packet in the FIFO, then clear the RXSETUP. RXSETUP cannot be cleared before the setup packet has been read in the FIFO. Otherwise, the USB device would accept the next Data OUT transfer and overwrite the setup packet in the FIFO.

**Figure 40-5. Setup Transaction Followed by a Data OUT Transaction**



- **WAKEUP: USB Bus Wakeup Interrupt**

0: USB Bus Wakeup Interrupt is disabled

1: USB Bus Wakeup Interrupt is enabled

Note: When the USB block is in suspend mode, the application may power down the USB logic. In this case, any USB HOST resume request that is made must be taken into account and, thus, the reset value of the RXRSM bit of the register UDP_IMR is enabled.

### 41.7.5 ACC Interrupt Mask Register

**Name:** ACC_IMR

**Address:** 0x4004002C

**Access:** Read-only

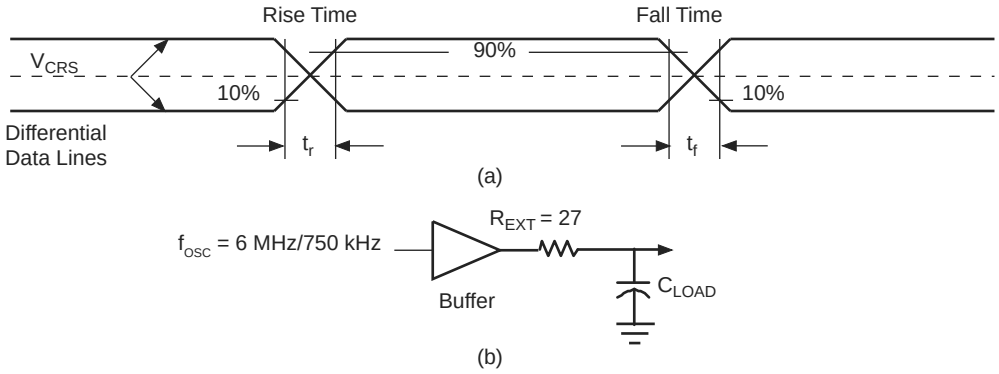
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | – | – | – |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| – | – | – | – | – | – | – | – |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| – | – | – | – | – | – | – | – |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| – | – | – | – | – | – | – | CE |

- **CE: Comparison Edge**

0: The interrupt is disabled.

1: The interrupt is enabled.

**Figure 44-17. USB Data Signal Rise and Fall Times**



**10-bit ADC Mode**

In 10-bit mode, the ADC produces 12-bit output but the output data in the register ADC_CDRx is shifted two bits to the right, removing the two LSBs of the 12-bit ADC.

The gain and offset have the same values as for 12-bit mode, with digital full-scale output code range reduced to 1024 (vs 4096).

The INL and DNL have the same values as for 12-bit mode.

The dynamic performances are the 12-bit mode values, reduced by 12 dB.

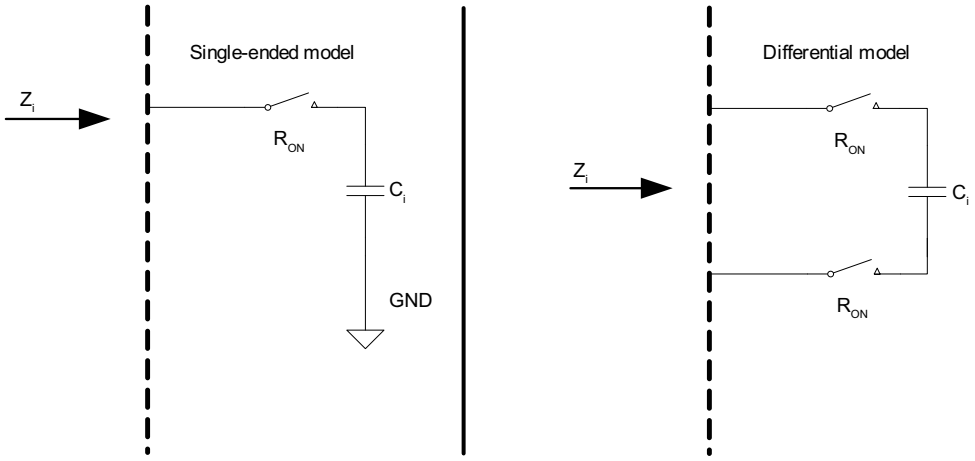
**Low Voltage Supply**

The ADC performs in 10-bit mode or in 12-bit mode. Working at low voltage ($V_{DDIN}$ or/and $V_{ADVREF}$) between 2 and 2.4V is subject to the following restrictions:

- The field IBCTL must be 00 to reduce the biasing of the ADC under low voltage. See Section 44.8.1.1 “ADC Bias Current”.
- In 10-bit mode, the ADC clock should not exceed 5 MHz (max signal bandwidth is 250 kHz).
- In 12-bit mode, the ADC clock should not exceed 2 MHz (max signal bandwidth is 100 kHz).

### 44.8.5.3 ADC Channel Input Impedance

**Figure 44-20. Input Channel Model**




where:

- $Z_i$ is input impedance in single-ended or differential mode
- $C_i$ = 1 to 8 pF ±20% depending on the gain value and mode (SE or DIFF); temperature dependency is negligible
- $R_{ON}$ is typical 2 kΩ and 8 kΩ max (worst case process and high temperature)
- $R_{ON}$ is negligible regarding the value of $Z_i$

The following formula is used to calculate input impedance:

$$Z_i = \frac{1}{f_S \times C_i}$$

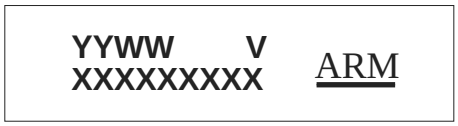
where:

- $f_S$ is the sampling frequency of the ADC channel
- Typ values are used to compute ADC input impedance $Z_i$

# 46. Marking

All devices are marked with the Atmel logo and the ordering code.

Additional marking is as follows:




where

- “YY”: manufactory year
- “WW”: manufactory week
- “V”: revision
- “XXXXXXXXX”: lot number