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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4s2ca-cu

Features

- Core
  - ARM Cortex-M4 with 2 Kbytes of cache running at up to 120 MHz
  - Memory Protection Unit (MPU)
  - DSP Instruction Set
  - Thumb®-2 instruction set
- Pin-to-pin compatible with SAM3N, SAM3S, SAM4N and SAM7S legacy products (64-pin version)
- Memories
  - Up to 2048 Kbytes embedded Flash with optional dual-bank and cache memory, ECC, Security Bit and Lock Bits
  - Up to 160 Kbytes embedded SRAM
  - 16 Kbytes ROM with embedded boot loader routines (UART, USB) and IAP routines
  - 8-bit Static Memory Controller (SMC): SRAM, PSRAM, NOR and NAND Flash support
- System
  - Embedded voltage regulator for single supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main power with failure detection and optional low-power 32.768 kHz for RTC or device clock
  - RTC with Gregorian and Persian calendar mode, waveform generation in low-power modes
  - RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency inaccuracy
  - High-precision 8/12 MHz factory-trimmed internal RC oscillator with 4 MHz default frequency for device startup, in-application trimming access for frequency adjustment
  - Slow clock internal RC oscillator as permanent low-power mode device clock
  - Two PLLs up to 240 MHz for device clock and for USB
  - Temperature sensor
  - Low-power tamper detection on two inputs, anti-tampering by immediate clear of general-purpose backup registers (GPBR)
  - Up to 22 Peripheral DMA (PDC) channels
- Low-power Modes
  - Sleep, Wait and Backup modes; consumption down to 1 µA in Backup mode
- Peripherals
  - USB 2.0 Device: 12 Mbps, 2668 byte FIFO, up to 8 bidirectional Endpoints, on-chip transceiver
  - Up to two USARTs with ISO7816, IrDA®, RS-485, SPI, Manchester and Modem Mode
  - Two 2-wire UARTs
  - Up to two 2-Wire Interface modules (I2C-compatible), one SPI, one Serial Synchronous Controller (I2S), one high-speed Multimedia Card Interface (SDIO/SD Card/MMC)
  - Two 3-channel 16-bit Timer Counters with capture, waveform, compare and PWM mode, Quadrature decoder logic and 2-bit Gray up/down counter for stepper motor
  - 4-channel 16-bit PWM with complementary output, fault input, 12-bit dead time generator counter for motor control
  - 32-bit Real-time Timer and RTC with calendar, alarm and 32 kHz trimming features
  - 256-bit General Purpose Backup Registers (GPBR)
  - Up to 16-channel, 1Msps ADC with differential input mode and programmable gain stage and auto calibration
  - One 2-channel 12-bit 1Msps DAC
  - One Analog Comparator with flexible input selection, selectable input hysteresis
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU) for data integrity check of off-/on-chip memories
  - Register Write Protection

4.1.5 100-ball TFBGA Pinout

Table 4-2. SAM4SD32/SD16/SA16/S16/S8/S4/S2 100-ball TFBGA Pinout

A1	PB1/AD5	C6	TCK/SWCLK/PB7	F1	PA18/PGMD6/AD1	H6	PC4
A2	PC29/AD13	C7	PC16	F2	PC26	H7	PA11/PGMM3
A3	VDDIO	C8	PA1/PGMEN1	F3	VDDOUT	H8	PC1
A4	PB9/PGMCK/XIN	C9	PC17	F4	GND	H9	PA6/PGMNOE
A5	PB8/XOUT	C10	PA0/PGMEN0	F5	VDDIO	H10	TDI/PB4
A6	PB13/DAC0	D1	PB3/AD7	F6	PA27/PGMD15	J1	PC15/AD11
A7	DDP/PB11	D2	PB0/AD4	F7	PC8	J2	PC0
A8	DDM/PB10	D3	PC24	F8	PA28	J3	PA16/PGMD4
A9	TMS/SWDIO/PB6	D4	PC22	F9	TST	J4	PC6
A10	JTAGSEL	D5	GND	F10	PC9	J5	PA24/PGMD12
B1	PC30/AD14	D6	GND	G1	PA21/PGMD9/AD8	J6	PA25/PGMD13
B2	ADVREF	D7	VDDCORE	G2	PC27	J7	PA10/PGMM2
B3	GNDANA	D8	PA2/PGMEN2	G3	PA15/PGMD3	J8	GND
B4	PB14/DAC1	D9	PC11	G4	VDDCORE	J9	VDDCORE
B5	PC21	D10	PC14	G5	VDDCORE	J10	VDDIO
B6	PC20	E1	PA17/PGMD5/AD0	G6	PA26/PGMD14	K1	PA22/PGMD10/AD9
B7	PA31	E2	PC31	G7	PA12/PGMD0	K2	PC13/AD10
B8	PC19	E3	VDDIN	G8	PC28	K3	PC12/AD12
B9	PC18	E4	GND	G9	PA4/PGMNCMD	K4	PA20/PGMD8/AD3
B10	TDO/TRACESWO/PB5	E5	GND	G10	PA5/PGMRDY	K5	PC5
C1	PB2/AD6	E6	NRST	H1	PA19/PGMD7/AD2	K6	PC3
C2	VDDPLL	E7	PA29	H2	PA23/PGMD11	K7	PC2
C3	PC25	E8	PA30	H3	PC7	K8	PA9/PGMM1
C4	PC23	E9	PC10	H4	PA14/PGMD2	K9	PA8/XOUT32/PGMM0
C5	ERASE/PB12	E10	PA3	H5	PA13/PGMD1	K10	PA7/XIN32/ PGMNVALID

Rd is the destination register.

Rn is the first register holding the operand.

Rm is the second register holding the operand.

Operation

The SEL instruction:

1. Reads the value of each bit of APSR.GE.
2. Depending on the value of APSR.GE, assigns the destination register the value of either the first or second operand register.

Restrictions

None.

Condition Flags

These instructions do not change the flags.

Examples

```
SADD16 R0, R1, R2    ; Set GE bits based on result
SEL    R0, R0, R3    ; Select bytes from R0 or R3, based on GE.
```

12.6.6.12 SDIV and UDIV

Signed Divide and Unsigned Divide.

Syntax

```
SDIV{cond} {Rd,} Rn, Rm
UDIV{cond} {Rd,} Rn, Rm
```

where:

cond is an optional condition code, see “Conditional Execution” .

Rd is the destination register. If *Rd* is omitted, the destination register is *Rn*.

Rn is the register holding the value to be divided.

Rm is a register holding the divisor.

Operation

SDIV performs a signed integer division of the value in *Rn* by the value in *Rm*.

UDIV performs an unsigned integer division of the value in *Rn* by the value in *Rm*.

For both instructions, if the value in *Rn* is not divisible by the value in *Rm*, the result is rounded towards zero.

Restrictions

Do not use SP and do not use PC.

Condition Flags

These instructions do not change the flags.

Examples

```
SDIV  R0, R2, R4  ; Signed divide, R0 = R2/R4
UDIV  R8, R8, R1  ; Unsigned divide, R8 = R8/R1
```

12.6.9 Bitfield Instructions

The table below shows the instructions that operate on adjacent sets of bits in registers or bitfields.

Table 12-24. Packing and Unpacking Instructions

Mnemonic	Description
BFC	Bit Field Clear
BFI	Bit Field Insert
SBFX	Signed Bit Field Extract
SXTB	Sign extend a byte
SXTH	Sign extend a halfword
UBFX	Unsigned Bit Field Extract
UXTB	Zero extend a byte
UXTH	Zero extend a halfword

The software reset is entered if at least one of these bits is set by the software. All these commands can be performed independently or simultaneously. The software reset lasts three slow clock cycles.

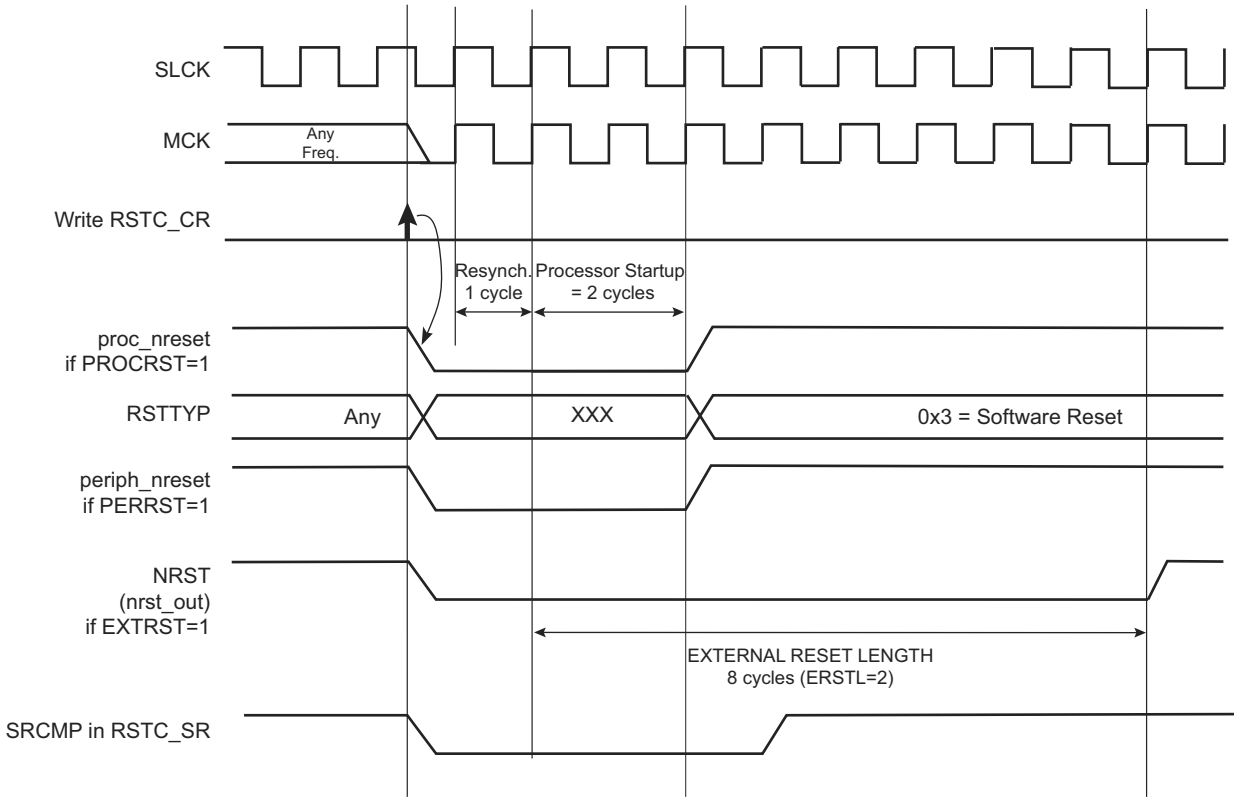
The internal reset signals are asserted as soon as the register write is performed. This is detected on the Master Clock (MCK). They are released when the software reset has ended, i.e., synchronously to SLCK.

If EXTRST is set, the nrst_out signal is asserted depending on the configuration of field RSTC_MR.ERSTL. However, the resulting falling edge on NRST does not lead to a user reset.

If and only if the PROCRST bit is set, the Reset Controller reports the software status in field RSTC_SR.RSTTYP. Other software resets are not reported in RSTTYP.

As soon as a software operation is detected, the bit SRCMP (Software Reset Command in Progress) is set in the RSTC_SR. SRCMP is cleared at the end of the software reset. No other software reset can be performed while the SRCMP bit is set, and writing any value in the RSTC_CR has no effect.

Figure 14-5. Software Reset



14.4.3.5 User Reset

The user reset is entered when a low level is detected on the NRST pin and bit URSTEN in the RSTC_MR is at 1. The NRST input signal is resynchronized with SLCK to insure proper behavior of the system.

The user reset is entered as soon as a low level is detected on NRST. The processor reset and the peripheral reset are asserted.

The user reset ends when NRST rises, after a two-cycle resynchronization time and a three-cycle processor startup. The processor clock is re-enabled as soon as NRST is confirmed high.

When the processor reset signal is released, field RSTC_SR.RSTTYP is loaded with the value 0x4, indicating a user reset.

- **WDDBGHLT: Watchdog Debug Halt**

0: The watchdog runs when the processor is in debug state.

1: The watchdog stops when the processor is in debug state.

- **WDIDLEHLT: Watchdog Idle Halt**

0: The watchdog runs when the system is in idle mode.

1: The watchdog stops when the system is in idle state.

22.5.10 Cache Controller Monitor Status Register

Name: CMCC_MSR

Address: 0x4007C034

Access: Read-only

31	30	29	28	27	26	25	24
EVENT_CNT							

23	22	21	20	19	18	17	16
EVENT_CNT							

15	14	13	12	11	10	9	8
EVENT_CNT							

7	6	5	4	3	2	1	0
EVENT_CNT							

- **EVENT_CNT: Monitor Event Counter**

For more details about VID/PID for End Product/Systems, please refer to the Vendor ID form available from the USB Implementers Forum on www.usb.org.

Atmel provides an INF example to see the device as a new serial port and also provides another custom driver used by the SAM-BA application: atm6124.sys. Refer to the application note “USB Basic Application”, Atmel literature number 6123, for more details.

24.5.3.1 Enumeration Process

The USB protocol is a master/slave protocol. This is the host that starts the enumeration sending requests to the device through the control endpoint. The device handles standard requests as defined in the USB Specification.

Table 24-3. Handled Standard Requests

Request	Definition
GET_DESCRIPTOR	Returns the current device configuration value.
SET_ADDRESS	Sets the device address for all future device access.
SET_CONFIGURATION	Sets the device configuration.
GET_CONFIGURATION	Returns the current device configuration value.
GET_STATUS	Returns status for the specified recipient.
SET_FEATURE	Set or Enable a specific feature.
CLEAR_FEATURE	Clear or Disable a specific feature.

The device also handles some class requests defined in the CDC class.

Table 24-4. Handled Class Requests

Request	Definition
SET_LINE_CODING	Configures DTE rate, stop bits, parity and number of character bits.
GET_LINE_CODING	Requests current DTE rate, stop bits, parity and number of character bits.
SET_CONTROL_LINE_STATE	RS-232 signal used to tell the DCE device the DTE device is now present.

Unhandled requests are STALLed.

24.5.3.2 Communication Endpoints

There are two communication endpoints and endpoint 0 is used for the enumeration process. Endpoint 1 is a 64-byte Bulk OUT endpoint and endpoint 2 is a 64-byte Bulk IN endpoint. SAM-BA Boot commands are sent by the host through endpoint 1. If required, the message is split by the host into several data payloads by the host driver.

If the command requires a response, the host can send IN transactions to pick up the response.

26.16.1 SMC Setup Register

Name: SMC_SETUP[0..3]

Address: 0x400E0000 [0], 0x400E0010 [1], 0x400E0020 [2], 0x400E0030 [3]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	NCS_RD_SETUP					

23	22	21	20	19	18	17	16
–	–	NRD_SETUP					

15	14	13	12	11	10	9	8
–	–	NCS_WR_SETUP					

7	6	5	4	3	2	1	0
–	–	NWE_SETUP					

This register can only be written if the WPEN bit is cleared in the “SMC Write Protection Mode Register” .

- **NWE_SETUP: NWE Setup Length**

The NWE signal setup length is defined as:

NWE setup length = (128* NWE_SETUP[5] + NWE_SETUP[4:0]) clock cycles

- **NCS_WR_SETUP: NCS Setup Length in WRITE Access**

In write access, the NCS signal setup length is defined as:

NCS setup length = (128* NCS_WR_SETUP[5] + NCS_WR_SETUP[4:0]) clock cycles

- **NRD_SETUP: NRD Setup Length**

The NRD signal setup length is defined in clock cycles as:

NRD setup length = (128* NRD_SETUP[5] + NRD_SETUP[4:0]) clock cycles

- **NCS_RD_SETUP: NCS Setup Length in READ Access**

In read access, the NCS signal setup length is defined as:

NCS setup length = (128* NCS_RD_SETUP[5] + NCS_RD_SETUP[4:0]) clock cycles

Prior to instructing the device to enter Wait mode:

1. Select the fast RC oscillator as the master clock source (the CSS field in PMC_MCKR must be written to 1).
2. Disable the PLL if enabled.
3. Clear the internal wake-up sources.

The system enters Wait mode either by setting the WAITMODE bit in CKGR_MOR, or by executing the WaitForEvent (WFE) instruction of the processor while the LPM bit is at 1 in PMC_FSMR. Immediately after setting the WAITMODE bit or using the WFE instruction, wait for the MCKRDY bit to be set in PMC_SR.

A fast startup is enabled upon the detection of a programmed level on one of the 16 wake-up inputs (WKUP) or upon an active alarm from the RTC, RTT and USB Controller. The polarity of the 16 wake-up inputs is programmable by writing the PMC Fast Startup Polarity Register (PMC_FSPR).

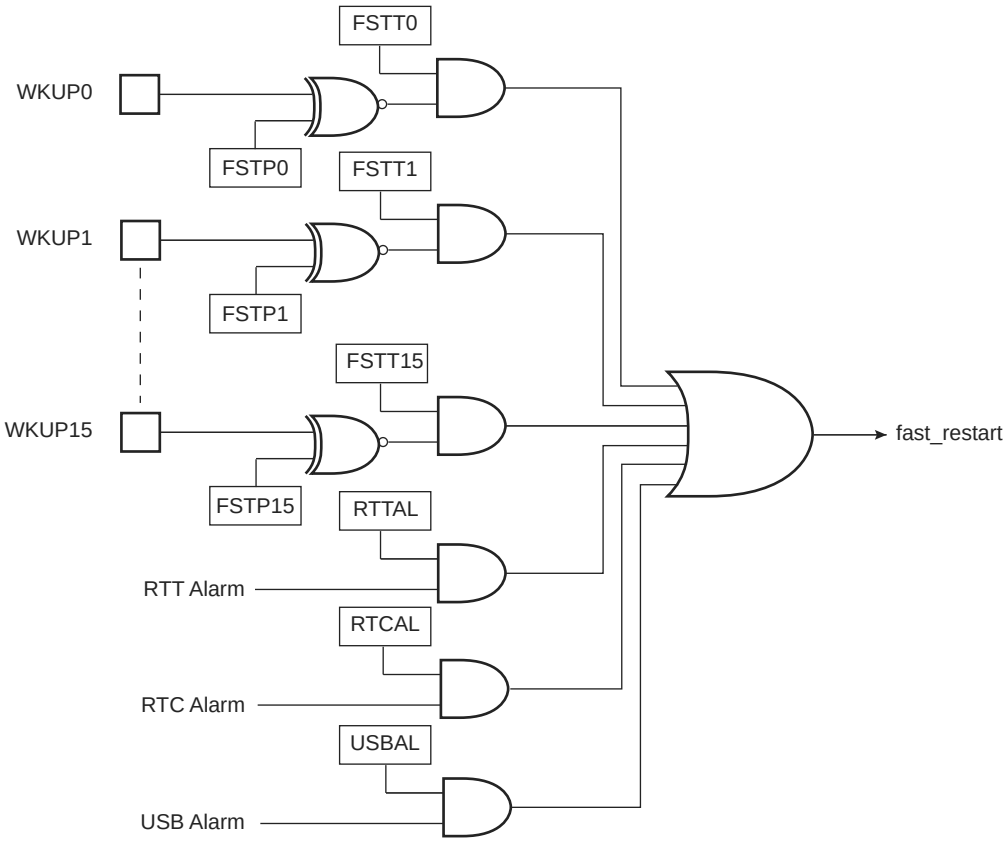
The fast startup circuitry, as shown in Figure 29-4, is fully asynchronous and provides a fast startup signal to the PMC. As soon as the fast startup signal is asserted, the embedded 4/8/12 MHz fast RC oscillator restarts automatically.

When entering Wait mode, the embedded Flash can be placed in one of the Low-power modes (Deep-power-down or Standby modes) depending on the configuration of the FLPM field in the PMC_FSMR. The FLPM field can be programmed at anytime and its value will be applied to the next Wait mode period.

The power consumption reduction is optimal when configuring 1 (Deep-power-down mode) in field FLPM. If 0 is programmed (Standby mode), the power consumption is slightly higher than in Deep-power-down mode.

When programming 2 in field FLPM, the Wait mode Flash power consumption is equivalent to that of the Active mode when there is no read access on the Flash.

Figure 29-4. Fast Startup Circuitry



31.6.44 PIO Fall/Rise - Low/High Status Register

Name: PIO_FRLHSR

Address: 0x400E0ED8 (PIOA), 0x400E10D8 (PIOB), 0x400E12D8 (PIOC)

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0–P31: Edge/Level Interrupt Source Selection**

0: The interrupt source is a falling edge detection (if PIO_ELSR = 0) or low-level detection event (if PIO_ELSR = 1).

1: The interrupt source is a rising edge detection (if PIO_ELSR = 0) or high-level detection event (if PIO_ELSR = 1).

32.8.10 Register Write Protection

To prevent any single software error from corrupting AIC behavior, certain registers in the address space can be write-protected by setting the WPEN bit in the SSC Write Protection Mode Register (SSC_WPMR).

If a write access to a write-protected register is detected, the WPVS flag in the SSC Write Protection Status Register (SSC_WPSR) is set and the field WPVSRC indicates the register in which the write access has been attempted.

The WPVS bit is automatically cleared after reading the SSC_WPSR.

The following registers can be write-protected:

- SSC Clock Mode Register
- SSC Receive Clock Mode Register
- SSC Receive Frame Mode Register
- SSC Transmit Clock Mode Register
- SSC Transmit Frame Mode Register
- SSC Receive Compare 0 Register
- SSC Receive Compare 1 Register

37.7.8 TC Register C

Name: TC_RCx [x=0..2]

Address: 0x4001001C (0)[0], 0x4001005C (0)[1], 0x4001009C (0)[2], 0x4001401C (1)[0], 0x4001405C (1)[1], 0x4001409C (1)[2]

Access: Read/Write

31	30	29	28	27	26	25	24
RC							

23	22	21	20	19	18	17	16
RC							

15	14	13	12	11	10	9	8
RC							

7	6	5	4	3	2	1	0
RC							

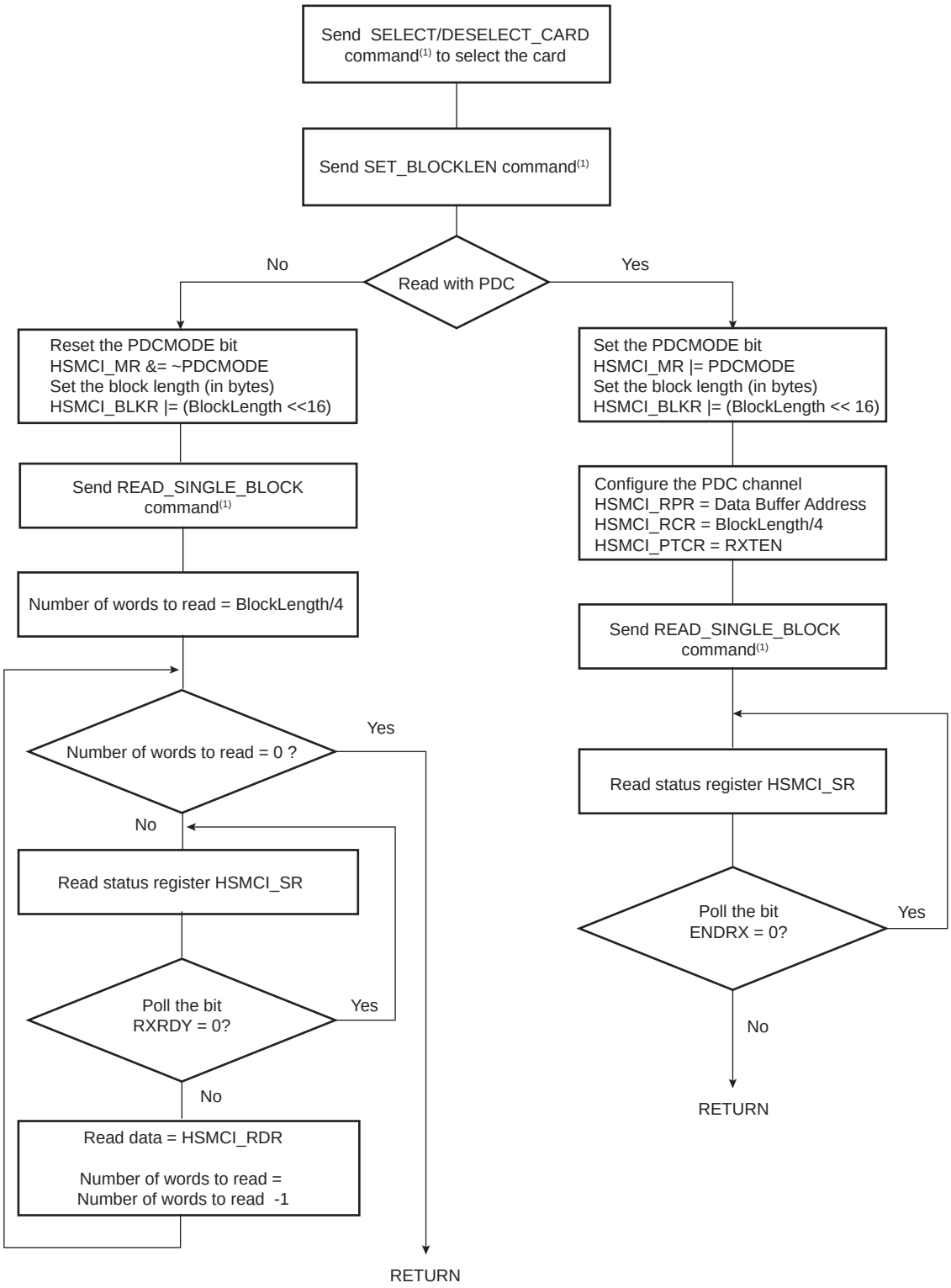
This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

- **RC: Register C**

RC contains the Register C value in real time.

IMPORTANT: For 16-bit channels, RC field size is limited to register bits 15:0.

Figure 38-8. Read Functional Flow Diagram



Note: 1. It is assumed that this command has been correctly sent (see Figure 38-7).

- **WAKEUP: USB Bus Wakeup Interrupt**

0: USB Bus Wakeup Interrupt is disabled

1: USB Bus Wakeup Interrupt is enabled

Note: When the USB block is in suspend mode, the application may power down the USB logic. In this case, any USB HOST resume request that is made must be taken into account and, thus, the reset value of the RXRSM bit of the register UDP_IMR is enabled.

42.2 Embedded Characteristics

- 12-bit Resolution
- 1 MHz Conversion Rate
- On-chip Temperature Sensor Management
- Wide Range of Power Supply Operation
- Selectable Single-Ended or Differential Input Voltage
- Programmable Gain For Maximum Full-Scale Input Range 0–V_{DD}
- Integrated Multiplexer Offering Up to 16 Independent Analog Inputs
- Individual Enable and Disable of Each Channel
- Hardware or Software Trigger
  - External Trigger Pin
  - Timer Counter Outputs (Corresponding TIOA Trigger)
  - PWM Event Line
- Drive of PWM Fault Input
- PDC Support
- Possibility of ADC Timings Configuration
- Two Sleep Modes and Conversion Sequencer
  - Automatic Wakeup on Trigger and Back to Sleep Mode after Conversions of all Enabled Channels
  - Possibility of Customized Channel Sequence
- Standby Mode for Fast Wakeup Time Response
  - Power Down Capability
- Automatic Window Comparison of Converted Values
- Register Write Protection

Figure 42-7. Analog Full Scale Ranges in Single-Ended/Differential Applications Versus Gain and Offset

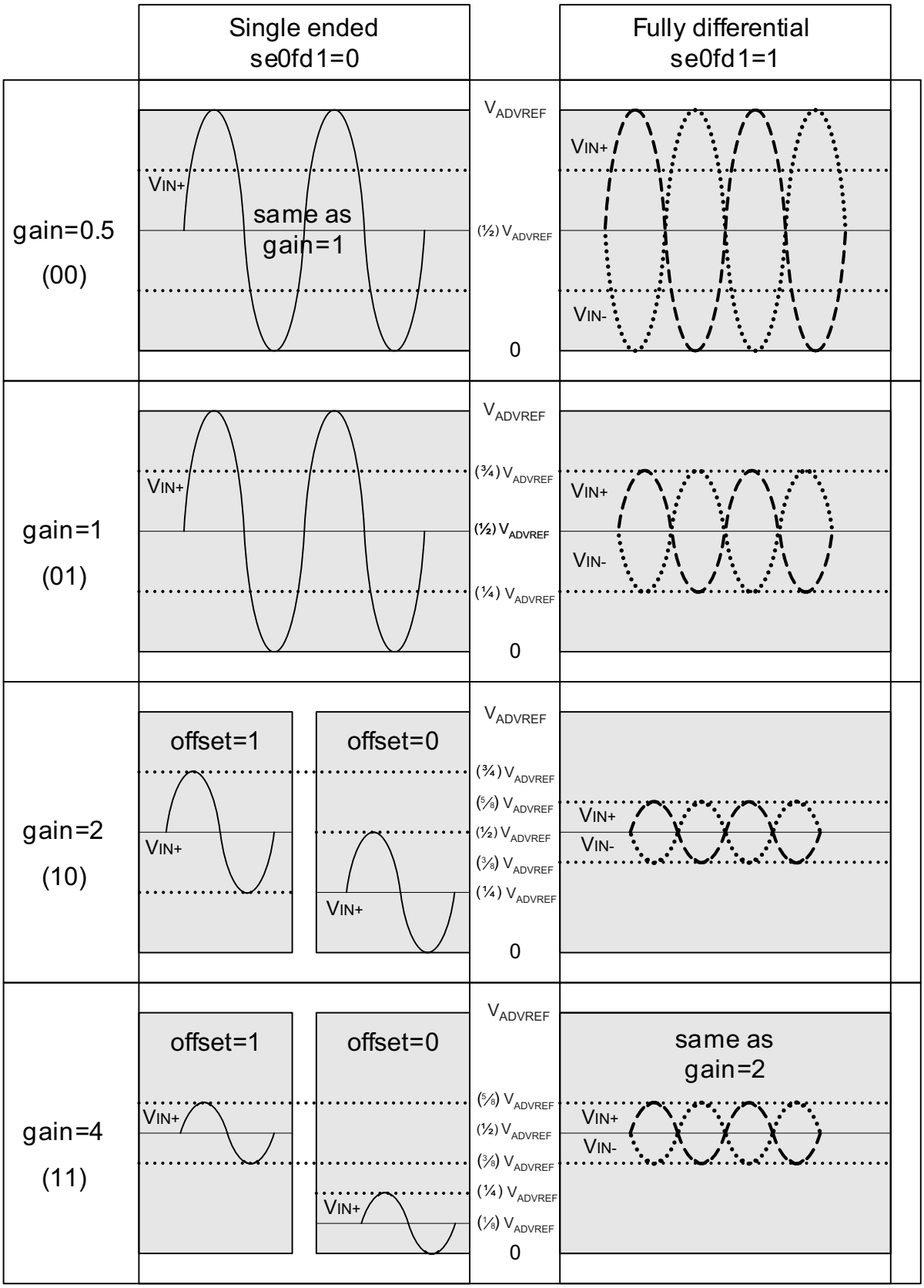


Table 44-16. SAM4SD32/SD16/SA16 Typical Sleep Mode Current Consumption vs Master Clock (MCK) Variation with PLLA

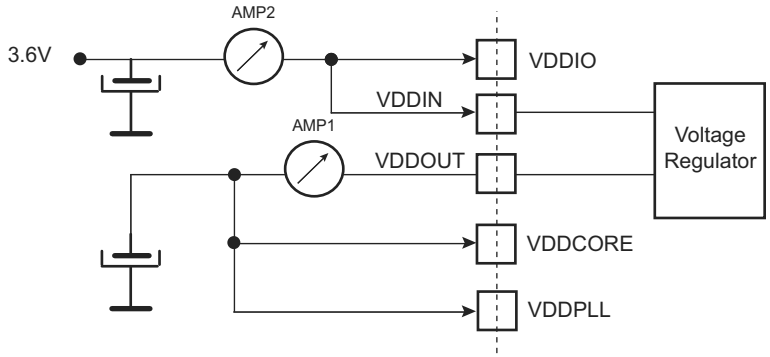
Core Clock/MCK (MHz)	Typical Value @ 25°C		Unit
	VDDCORE Consumption (AMP1)	Total Consumption (AMP2)	
120	8.4	10.6	mA
100	7.1	8.9	
84	6.0	7.5	
64	4.6	5.8	
48	3.5	4.4	
32	2.4	3.1	
24	1.8	2.4	

Table 44-17. SAM4SD32/SD16/SA16 Typical Sleep Mode Current Consumption vs Master Clock (MCK) Variation with Fast RC

Core Clock/MCK (MHz)	Typical Value @ 25°C		Unit
	VDDCORE Consumption (AMP1)	Total Consumption (AMP2)	
12	1.1	1.8	mA
8	0.8	1.2	
4	0.4	0.7	
2	0.3	0.7	
1	0.2	0.5	
0.5	0.2	0.5	

44.4.2.2 Wait Mode

Figure 44-9. Measurement Setup for Wait Mode



- VDDIO = VDDIN = 3.6V
- Core clock and master clock stopped
- Current measurement as shown in the above figure
- BOD disabled
- All peripheral clocks deactivated

Table 44-18 gives current consumption in typical conditions.

Table 49-5. SAM4S Datasheet Rev. 11100G Revision History

Doc. Date	Changes
27-May-14	Table 3-1 ”Signal Description List”: WKUP[15:0] voltage reference type added.
	In Figure 5-4 “Backup Battery”, modified ADC, DAC, Analog Comparator Supply from 2.0V to 2.4V
	Modified Section 6.5 “ERASE Pin”.
	Modified bullet list on use of erase commands depending on sector size in Section 8.1.3.1 “Flash Overview”
	Modified Section 8.1.3.5 “Security Bit”, Section 8.1.3.11 “GPNVM Bits” and Section 8.1.4 “Boot Strategies”.
	Section 24. “Boot Program” Section 24.5.4 “In Application Programming (IAP) Feature”: 5th sentence: added “...the EFC number...”
	Section 29. “Power Management Controller (PMC)” Section 29.17.9 “PMC Clock Generator PLLA Register”: Min value for bit MULA corrected to 4 from 7. Section 29.17.10 “PMC Clock Generator PLLB Register”: Min value for bit MULB corrected to 4 from 1.
	Section 44. “Electrical Characteristics” Added Table 44-24 ”Typical Power Consumption on VDDCORE (VDDIO = 3.3V, TA = 25°C)”. Table 44-73 ”AC Flash Characteristics”: Added parameter Erase Pin Assertion Time.
	Section 48. “Errata” Added Section Issue: and Section Issue: “Incorrect Flash Read May Occur Depending on VDDIO Voltage and Flash Wait State”.