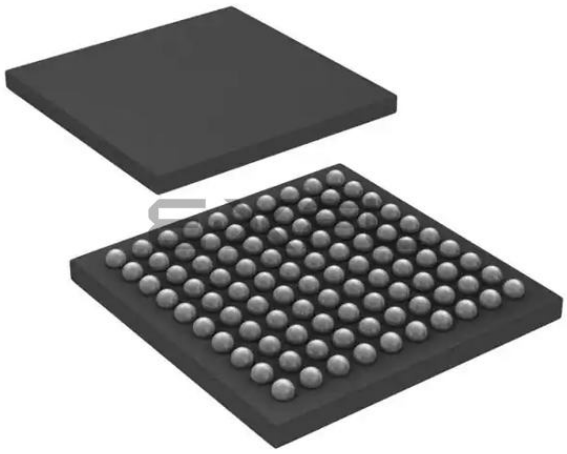

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4s2cb-cfn

6. Input/Output Lines

The SAM4S has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in I/O mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

GPIO Lines are managed by PIO controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to Section 31. “Parallel Input/Output Controller (PIO)”.

Some GPIOs can have alternate function as analog input. When the GPIO is set in analog mode, all digital features of the I/O are disabled.

The input/output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM4S embeds high-speed pads able to handle up to 70 MHz for HSMCI (MCK/2), 70 MHz for SPI clock lines and 46 MHz on other lines. See Section 44.12 “AC Characteristics” for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see Figure 6-1). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM4S) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination

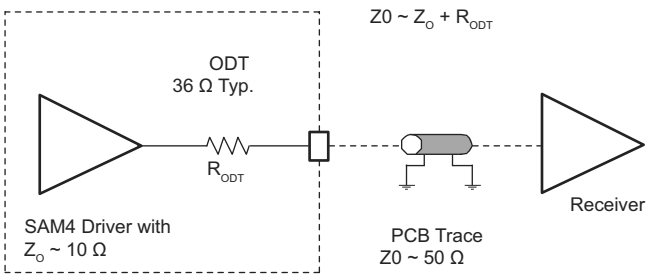


Table 12-11. Faults (Continued)

Fault	Handler	Bit Name	Fault Status Register
Bus error:	Bus fault	–	–
during exception stacking		STKERR	“BFSR: Bus Fault Status Subregister”
during exception unstacking		UNSTKERR	
during instruction prefetch		IBUSERR	
during lazy floating-point state preservation		LSPERR(3)	
Precise data bus error		PRECISERR	
Imprecise data bus error		IMPRECISERR	
Attempt to access a coprocessor	Usage fault	NOCP	“UFSR: Usage Fault Status Subregister”
Undefined instruction		UNDEFINSTR	
Attempt to enter an invalid instruction set state		INVSTATE	
Invalid EXC_RETURN value		INVPC	
Illegal unaligned load or store		UNALIGNED	
Divide By 0		DIVBYZERO	

Notes:
1. Occurs on an access to an XN region even if the processor does not include an MPU or the MPU is disabled.
2. Attempt to use an instruction set other than the Thumb instruction set, or return to a non load/store-multiple instruction with ICI continuation.
3. Only present in a Cortex-M4F device

Fault Escalation and Hard Faults

All faults exceptions except for hard fault have configurable exception priority, see “System Handler Priority Registers” . The software can disable the execution of the handlers for these faults, see “System Handler Control and State Register” .

Usually, the exception priority, together with the values of the exception mask registers, determines whether the processor enters the fault handler, and whether a fault handler can preempt another fault handler, as described in “Exception Model” .

In some situations, a fault with configurable priority is treated as a hard fault. This is called *priority escalation*, and the fault is described as *escalated to hard fault*. Escalation to hard fault occurs when:

- A fault handler causes the same kind of fault as the one it is servicing. This escalation to hard fault occurs because a fault handler cannot preempt itself; it must have the same priority as the current priority level.
- A fault handler causes a fault with the same or lower priority as the fault it is servicing. This is because the handler for the new fault cannot preempt the currently executing fault handler.
- An exception handler causes a fault for which the priority is the same as or lower than the currently executing exception.
- A fault occurs and the handler for that fault is not enabled.

If a bus fault occurs during a stack push when entering a bus fault handler, the bus fault does not escalate to a hard fault. This means that if a corrupted stack causes a fault, the fault handler executes even though the stack push for the handler failed. The fault handler operates but the stack contents are corrupted.

Note: Only Reset and NMI can preempt the fixed priority hard fault. A hard fault can preempt any exception other than Reset, NMI, or another hard fault.

Fault Status Registers and Fault Address Registers

The fault status registers indicate the cause of a fault. For bus faults and memory management faults, the fault address register indicates the address accessed by the operation that caused the fault, as shown in Table 12-12.

14.5.3 Reset Controller Mode Register

Name: RSTC_MR

Address: 0x400E1408

Access: Read/Write

31	30	29	28	27	26	25	24
KEY							

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	ERSTL			

7	6	5	4	3	2	1	0
–	–	–	URSTIEN	–	–	–	URSTEN

This register can only be written if the WPEN bit is cleared in the System Controller Write Protection Mode Register (SYSC_WPMR).

- **URSTEN: User Reset Enable**

0: The detection of a low level on the NRST pin does not generate a user reset.

1: The detection of a low level on the NRST pin triggers a user reset.

- **URSTIEN: User Reset Interrupt Enable**

0: USRTS bit in RSTC_SR at 1 has no effect on rstc_irq.

1: USRTS bit in RSTC_SR at 1 asserts rstc_irq if URSTEN = 0.

- **ERSTL: External Reset Length**

This field defines the external reset length. The external reset is asserted during a time of $2^{(ERSTL+1)}$ slow clock cycles. This allows assertion duration to be programmed between 60 µs and 2 seconds. Note that synchronization cycles must also be considered when calculating the actual reset length as previously described.

- **KEY: Write Access Password**

Value	Name	Description
0xA5	PASSWD	Writing any other value in this field aborts the write operation. Always reads as 0.

29.17.14PMC Interrupt Enable Register

Name: PMC_IER

Address: 0x400E0460

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	CFDEV	MOSCRCS	MOSCSELS
15	14	13	12	11	10	9	8
–	–	–	–	–	PCKRDY2	PCKRDY1	PCKRDY0
7	6	5	4	3	2	1	0
–	–	–	–	MCKRDY	LOCKB	LOCKA	MOSCXTS

The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

- **MOSCXTS: Main Crystal Oscillator Status Interrupt Enable**
- **LOCKA: PLLA Lock Interrupt Enable**
- **LOCKB: PLLB Lock Interrupt Enable**
- **MCKRDY: Master Clock Ready Interrupt Enable**
- **PCKRDYx: Programmable Clock Ready x Interrupt Enable**
- **MOSCSELS: Main Oscillator Selection Status Interrupt Enable**
- **MOSCRCS: Main On-Chip RC Status Interrupt Enable**
- **CFDEV: Clock Failure Detector Event Interrupt Enable**

31.6.2 PIO Disable Register

Name: PIO_PDR

Address: 0x400E0E04 (PIOA), 0x400E1004 (PIOB), 0x400E1204 (PIOC)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in the PIO Write Protection Mode Register.

- **P0–P31: PIO Disable**

0: No effect.

1: Disables the PIO from controlling the corresponding pin (enables peripheral control of the pin).

31.6.37 PIO Additional Interrupt Modes Disable Register

Name: PIO_AIMDR

Address: 0x400E0EB4 (PIOA), 0x400E10B4 (PIOB), 0x400E12B4 (PIOC)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0–P31: Additional Interrupt Modes Disable**

0: No effect.

1: The interrupt mode is set to the default interrupt mode (both-edge detection).

31.6.38 PIO Additional Interrupt Modes Mask Register

Name: PIO_AIMMR

Address: 0x400E0EB8 (PIOA), 0x400E10B8 (PIOB), 0x400E12B8 (PIOC)

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0–P31: IO Line Index**

Selects the IO event type triggering an interrupt.

0: The interrupt source is a both-edge detection event.

1: The interrupt source is described by the registers PIO_ELSR and PIO_FRLHSR.

32.5 SSC Application Examples

The SSC can support several serial communication modes used in audio or high speed serial links. Some standard applications are shown in the following figures. All serial link applications supported by the SSC are not listed here.

Figure 32-3. Audio Application Block Diagram

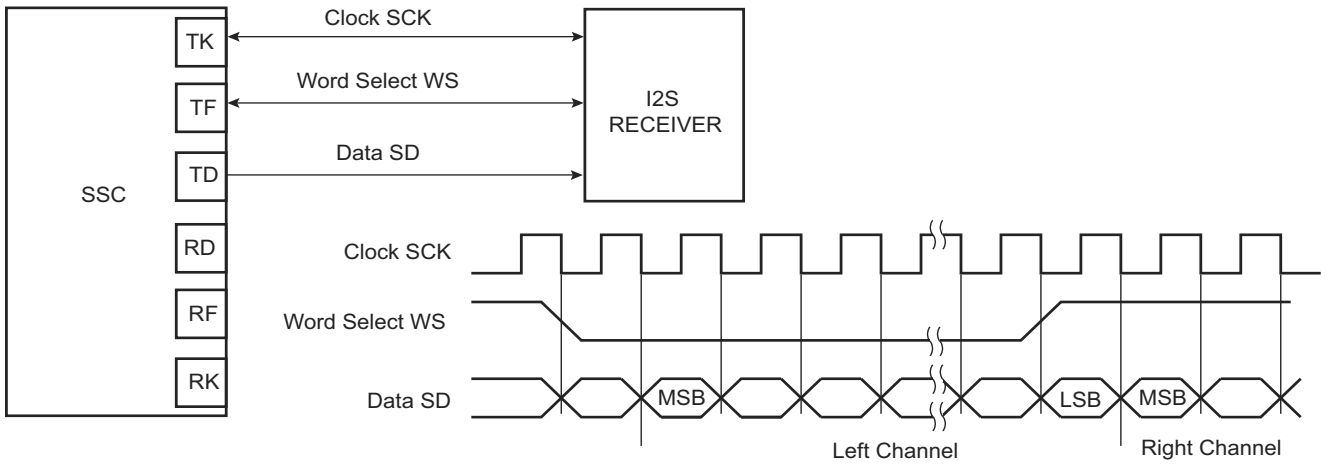


Figure 32-4. Codec Application Block Diagram

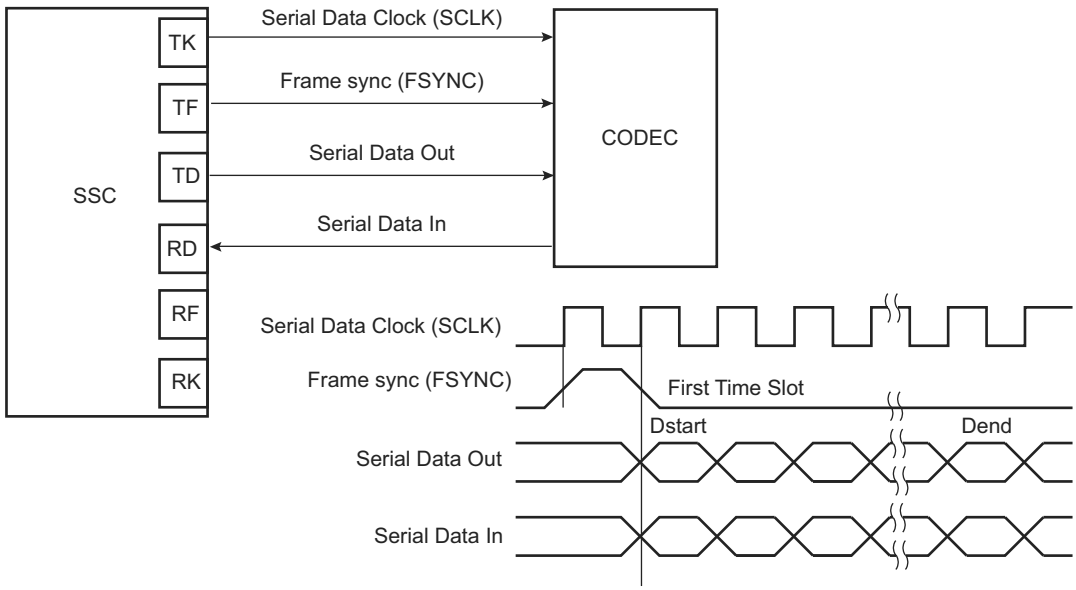
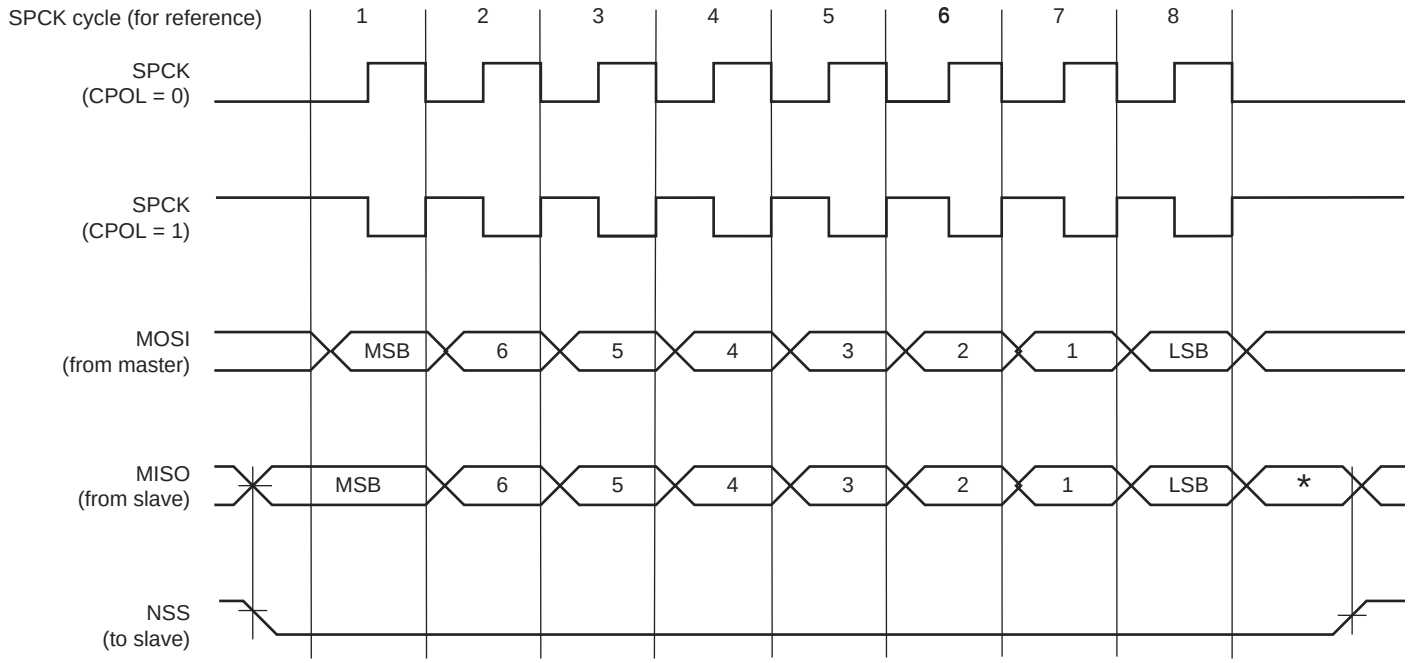
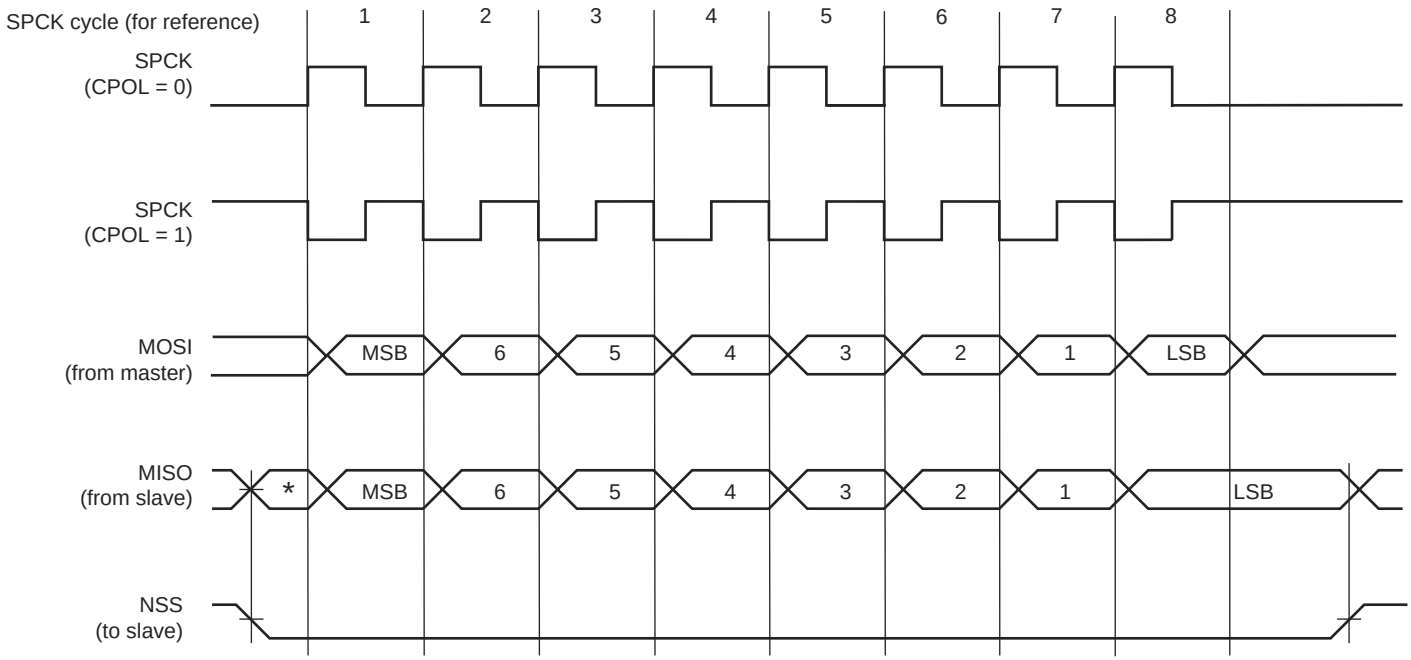


Figure 33-3. SPI Transfer Format (NCPHA = 1, 8 bits per transfer)



* Not defined.

Figure 33-4. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)



* Not defined.

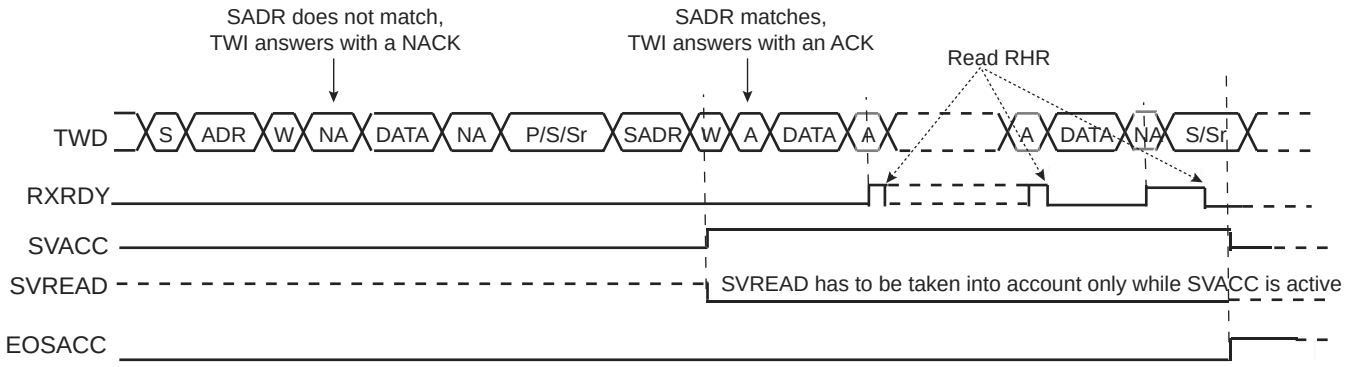
After a START or a REPEATED START, the decoding of the address starts. If the slave address is decoded, SVACC is set and SVREAD indicates the direction of the transfer (SVREAD is low in this case).

Until a STOP or REPEATED START condition is detected, TWI stores the received data in the TWI_RHR.

If a STOP condition or a REPEATED START + an address different from SADR is detected, SVACC is reset.

Figure 34-25 describes the write operation.

Figure 34-25. Write Access Ordered by a Master



Notes: 1. When SVACC is low, the state of SVREAD becomes irrelevant.

2. RXRDY is set when data has been transmitted from the internal shifter to the TWI_RHR and reset when this data is read.

General Call

The general call is performed in order to change the address of the slave.

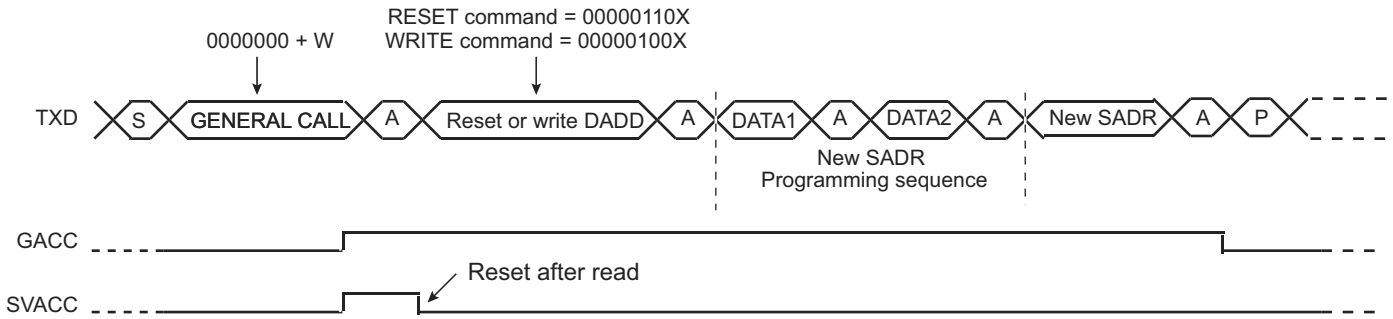
If a GENERAL CALL is detected, GACC is set.

After the detection of GENERAL CALL, it is up to the programmer to decode the commands which come afterwards.

In case of a WRITE command, the programmer has to decode the programming sequence and program a new SADR if the programming sequence matches.

Figure 34-26 describes the GENERAL CALL access.

Figure 34-26. Master Performs a General Call



Note: This method allows the user to create a personal programming sequence by choosing the programming bytes and the number of them. The programming sequence has to be provided to the master.

35.6.2 UART Mode Register

Name: UART_MR

Address: 0x400E0604 (0), 0x400E0804 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
CHMODE		–	–	PAR			–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	–

- **PAR: Parity Type**

Value	Name	Description
0	EVEN	Even Parity
1	ODD	Odd Parity
2	SPACE	Space: parity forced to 0
3	MARK	Mark: parity forced to 1
4	NO	No parity

- **CHMODE: Channel Mode**

Value	Name	Description
0	NORMAL	Normal mode
1	AUTOMATIC	Automatic echo
2	LOCAL_LOOPBACK	Local loopback
3	REMOTE_LOOPBACK	Remote loopback

36.7.1 USART Control Register

Name: US_CR

Address: 0x40024000 (0), 0x40028000 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	RTSDIS	RTSEN	DTRDIS	DTREN

15	14	13	12	11	10	9	8
RETTO	RSTNACK	RSTIT	SENDA	STTTO	STPBRK	STTBRK	RSTSTA

7	6	5	4	3	2	1	0
TXDIS	TXEN	RXDIS	RXEN	RSTTX	RSTRX	–	–

For SPI control, see Section 36.7.2 ”USART Control Register (SPI_MODE)”.

- **RSTRX: Reset Receiver**

0: No effect.

1: Resets the receiver.

- **RSTTX: Reset Transmitter**

0: No effect.

1: Resets the transmitter.

- **RXEN: Receiver Enable**

0: No effect.

1: Enables the receiver, if RXDIS is 0.

- **RXDIS: Receiver Disable**

0: No effect.

1: Disables the receiver.

- **TXEN: Transmitter Enable**

0: No effect.

1: Enables the transmitter if TXDIS is 0.

- **TXDIS: Transmitter Disable**

0: No effect.

1: Disables the transmitter.

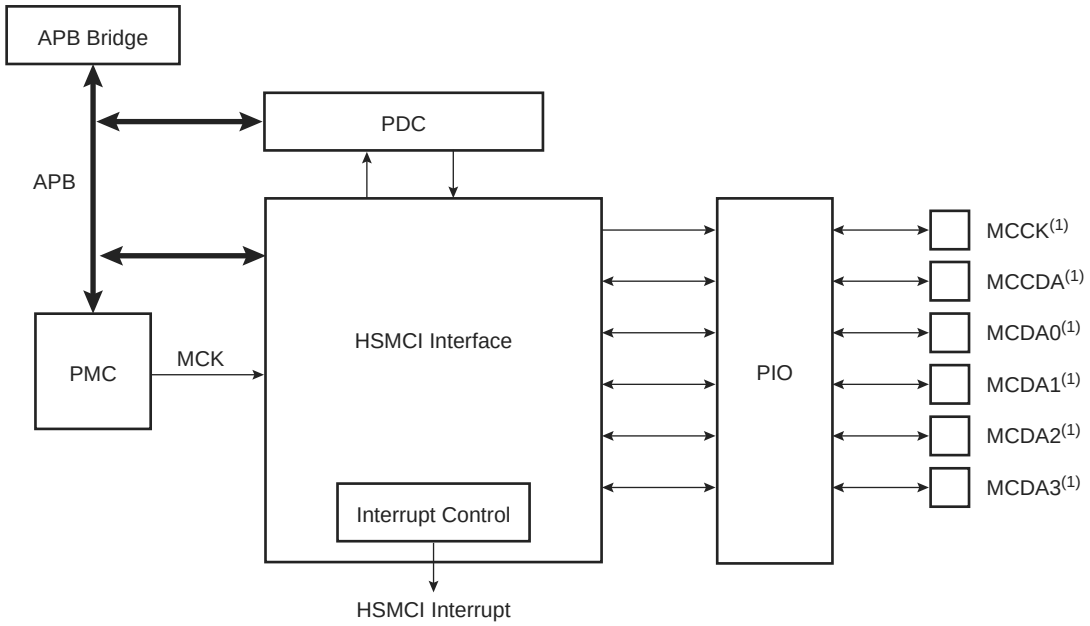
- **RSTSTA: Reset Status Bits**

0: No effect.

1: Resets the status bits PARE, FRAME, OVRE, MANERR and RXBRK in US_CSR.

38.3 Block Diagram

Figure 38-1. Block Diagram (4-bit configuration)



Note: 1. When several HSMCI (x HSMCI) are embedded in a product, MCCK refers to HSMCIx_CK, MCCDA to HSMCIx_CDA, MCDAy to HSMCIx_DAy.

For all the read operations, the NOTBUSY flag is cleared at the end of the host command.
For the Infinite Read Multiple Blocks, the NOTBUSY flag is set at the end of the STOP_TRANSMISSION host command (CMD12).

For the Single Block Reads, the NOTBUSY flag is set at the end of the data read block.

For the Multiple Block Reads with predefined block count, the NOTBUSY flag is set at the end of the last received data block.

The NOTBUSY flag allows to deal with these different states.

0: The HSMCI is not ready for new data transfer. Cleared at the end of the card response.

1: The HSMCI is ready for new data transfer. Set when the busy state on the data line has ended. This corresponds to a free internal data receive buffer of the card.

- **ENDRX: End of RX Buffer (cleared by writing HSMCI_RCR or HSMCI_RNCR(1))**

0: The Receive Counter Register has not reached 0 since the last write in HSMCI_RCR or HSMCI_RNCR.

1: The Receive Counter Register has reached 0 since the last write in HSMCI_RCR or HSMCI_RNCR.

- **ENDTX: End of TX Buffer (cleared by writing HSMCI_TCR or HSMCI_TNCR(1))**

0: The Transmit Counter Register has not reached 0 since the last write in HSMCI_TCR or HSMCI_TNCR.

1: The Transmit Counter Register has reached 0 since the last write in HSMCI_TCR or HSMCI_TNCR.

Note: BLKE and NOTBUSY flags can be used to check that the data has been successfully transmitted on the data lines and not only transferred from the PDC to the HSMCI Controller.

- **SDIOIRQA: SDIO Interrupt for Slot A (cleared on read)**

0: No interrupt detected on SDIO Slot A.

1: An SDIO Interrupt on Slot A occurred.

- **SDIOWAIT: SDIO Read Wait Operation Status**

0: Normal Bus operation.

1: The data bus has entered IO wait state.

- **CSRCV: CE-ATA Completion Signal Received (cleared on read)**

0: No completion signal received since last status read operation.

1: The device has issued a command completion signal on the command line.

- **RXBUFF: RX Buffer Full (cleared by writing HSMCI_RCR or HSMCI_RNCR(1))**

0: HSMCI_RCR or HSMCI_RNCR has a value other than 0.

1: Both HSMCI_RCR and HSMCI_RNCR have a value of 0.

- **TXBUFE: TX Buffer Empty (cleared by writing HSMCI_TCR or HSMCI_TNCR(1))**

0: HSMCI_TCR or HSMCI_TNCR has a value other than 0.

1: Both HSMCI_TCR and HSMCI_TNCR have a value of 0.

Note: BLKE and NOTBUSY flags can be used to check that the data has been successfully transmitted on the data lines and not only transferred from the PDC to the HSMCI Controller.

- **RINDE: Response Index Error (cleared by writing in HSMCI_CMDR)**

0: No error.

1: A mismatch is detected between the command index sent and the response index received.

- **RTOE: Response Time-out Error Interrupt Enable**
- **DCRCE: Data CRC Error Interrupt Enable**
- **DTOE: Data Time-out Error Interrupt Enable**
- **CSTOE: Completion Signal Timeout Error Interrupt Enable**
- **FIFOEMPTY: FIFO empty Interrupt enable**
- **XFRDONE: Transfer Done Interrupt enable**
- **ACKRCV: Boot Acknowledge Interrupt Enable**
- **ACKRCVE: Boot Acknowledge Error Interrupt Enable**
- **OVRE: Overrun Interrupt Enable**
- **UNRE: Underrun Interrupt Enable**

42.7.12 ADC Interrupt Status Register

Name: ADC_ISR

Address: 0x40038030

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	RXBUFF	ENDRX	COMPE	GOVRE	DRDY
23	22	21	20	19	18	17	16
EOCAL	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
EOC15	EOC14	EOC13	EOC12	EOC11	EOC10	EOC9	EOC8
7	6	5	4	3	2	1	0
EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0

- **EOCx: End of Conversion x (automatically set / cleared)**

0: The corresponding analog channel is disabled, or the conversion is not finished. This flag is cleared when reading the corresponding ADC_CDRx registers.

1: The corresponding analog channel is enabled and conversion is complete.

- **EOCAL: End of Calibration Sequence**

0: Calibration sequence is ongoing, or no calibration sequence has been requested.

1: Calibration sequence is complete.

- **DRDY: Data Ready (automatically set / cleared)**

0: No data has been converted since the last read of ADC_LCDR.

1: At least one data has been converted and is available in ADC_LCDR.

- **GOVRE: General Overrun Error (cleared on read)**

0: No general overrun error occurred since the last read of ADC_ISR.

1: At least one general overrun error has occurred since the last read of ADC_ISR.

- **COMPE: Comparison Event (cleared on read)**

0: No comparison event since the last read of ADC_ISR.

1: At least one comparison event (defined in the ADC_EMR and ADC_CWR) has occurred since the last read of ADC_ISR.

- **ENDRX: End of Receive Transfer (cleared by writing ADC_RCR or ADC_RNCR)**

0: The Receive Counter Register has not reached 0 since the last write in ADC_RCR or ADC_RNCR(1).

1: The Receive Counter Register has reached 0 since the last write in ADC_RCR or ADC_RNCR(1).

- **RXBUFF: Receive Buffer Full (cleared by writing ADC_RCR or ADC_RNCR)**

0: ADC_RCR or ADC_RNCR(1) has a value other than 0.

1: Both ADC_RCR and ADC_RNCR(1) have a value of 0.

Note: 1. ADC_RCR and ADC_RNCR are PDC registers

Table 44-4. 1.2V Voltage Regulator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDIN}	DC Input Voltage	(4)	1.6	3.3	3.6	V
V_{DDOUT}	DC Output Voltage	Normal Mode	–	1.2	–	V
		Standby Mode	–	0	–	
$V_{O(accuracy)}$	Output Voltage Accuracy	I_{LOAD} = 0.8mA to 80mA (after trimming)	-3		3	%
I_{LOAD}	Maximum DC Output Current	V_{DDIN} > 1.8V	–	–	80	mA
		$V_{DDIN} \leq$ 1.8V	–	–	40	
$I_{LOAD-START}$	Maximum Peak Current during Startup	(3)	–	–	400	
$V_{DROPOUT}$	Dropout Voltage	V_{DDIN} = 1.6V, I_{LOAD} = Max	–	400	–	mV
V_{LINE}	Line Regulation	V_{DDIN} from 2.7V to 3.6V; I_{LOAD} MAX	–	10	30	mV
$V_{LINE-TR}$	Transient Line Regulation	V_{DDIN} from 2.7V to 3.6V; $t_r = t_f$ = 5µs; I_{LOAD} Max	–	50	150	
V_{LOAD}	Load Regulation	$V_{DDIN} \geq$ 1.8V; I_{LOAD} = 10% to 90% MAX	–	20	40	mV
$V_{LOAD-TR}$	Transient Load Regulation	$V_{DDIN} \geq$ 1.8V; I_{LOAD} = 10% to 90% MAX; $t_r = t_f$ = 5 µs	–	50	150	mV
I_Q	Quiescent Current	Normal Mode, I_{LOAD} = 0 mA	–	5	–	µA
		Normal Mode, I_{LOAD} = 80 mA	–	500	–	
		Standby Mode	–	500	1	
CD_{IN}	Input Decoupling Capacitor	(1)	–	4.7	–	µF
CD_{OUT}	Output Decoupling Capacitor	(2)	1.85	2.2	5.9	µF
		ESR	0.1		10	Ω
t_{on}	Turn-on Time	CD_{OUT} = 2.2µF, V_{DDOUT} reaches 1.2V (± 3%)	–	300	–	µs
t_{off}	Turn-off Time	CD_{OUT} = 2.2µF	–	–	40	ms

Notes:
1. A 4.7µF or higher ceramic capacitor must be connected between VDDIN and the closest GND pin of the device. This large decoupling capacitor is mandatory to reduce startup current, improving transient response and noise rejection.
2. To ensure stability, an external 2.2 µF output capacitor, CD_{OUT} must be connected between the VDDOUT and the closest GND pin of the device. The ESR (Equivalent Series Resistance) of the capacitor must be in the range 0.1 to 10 Ω. Solid tantalum, and multilayer ceramic capacitors are all suitable as output capacitor. A 100 nF bypass capacitor between VDDOUT and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Defined as the current needed to charge external bypass/decoupling capacitor network.
4. See Section 5.2.2 “VDDIO Versus VDDIN”

48.4.3 PIO

Issue: **PB4 Input Low-level Voltage Range**

The undershoot is limited to -0.1V.

In normal operating conditions, the V_{IL} minimum value on PB4 is limited to 0V.

Workaround: The voltage on PB4 with respect to ground must be in the range -0.1V to + VDDIO + 0.4V instead of -0.3V to + VDDIO + 0.4V for all other input pins, as shown in Table 44.1 “Absolute Maximum Ratings”.

The minimum V_{IL} on PB4 must be 0V instead of -0.3V for all other input pins, as shown in Table 44.3 “DC Characteristics”.

Table 49-7. SAM4S Datasheet Rev. 11100E 24-Jul-13 Revision History (Continued)

Doc. Rev. 11100E	Comments	Change Request Ref.
	Ordering Information New ordering codes (105 °C, reel conditioning, WLCSP package) added in Table 47-1, “Ordering Codes for SAM4S Devices”.	8620, rfo
	Errata Added Section Issue: “Watchdog Not Stopped in Wait Mode” and Section Issue: “Unpredictable Behavior if BOD is Disabled, VDDCORE is Lost and VDDIO is Connected”.	9075
	Backpage ARMConnected® logo and corresponding text deleted.	rfo

Table 49-8. SAM4S Datasheet Rev. 11100D 15-Apr-13 Revision History

Doc. Rev. 11100D	Comments	Change Request Ref.
	Introduction Deleted sleep mode for fast start-up in Section 5.8 “Fast Start-up”. Added 32 kHz trimming features in Section “Features”. Notes added in Section 8.1.3.1 “Flash Overview”, below Figure 8-3.	8763 rfo
	Electrical Characteristics In Table 43-26, added 2 lines describing $C_{PARASTANDBY}$ and $R_{PARASTANDBY}$ parameters. In Table 43-62, Endurance line, deleted “Write/erase... @ 25°C” and 100k value. In Table 43-62, added Write Page Mode values.	8614 8850 8860
	Errata Deleted former Chapter 45 “SAM4S Series Errata” (was only a cross-reference to Engineering Samples Erratas), added a new detailed Section 48. “Errata”.	8645
	Backpage ARMPowered® logo replaced with ARMConnected® logo, corresponding text updated.	rfo

Table 49-9. SAM4S Datasheet Rev. 11100C 09-Jan-13 Revision History

Doc. Rev. 11100C	Comments	Change Request Ref.
	Introduction	
	In Section 2. “Block Diagram”, USB linked to Peripheral Bridge instead of AHB Bus Matrix in Figure 2-3, Figure 2-4, Figure 3. and Figure 2-2.	8386
	Reference to the LPM bit removed in the whole datasheet.	8392
	Flash rails mentioned in Section 5.1 “Power Supplies”.	8406
	Section 9. “Real Time Event Management” created.	8439
	WKUP[15:0] pins added on each block diagram in Section 2. “Block Diagram” and in Table 3-1, “Signal Description List”.	8459
	All diagrams updated with Real Time Events in Section 2. “Block Diagram”.	8484
	JTAG and PA7 pins details added in Section 6.2.1 “Serial Wire JTAG Debug Port (SWJ-DP) Pins”.	8547
	CORTEX	
	Section 12.8.3 “Nested Vectored Interrupt Controller (NVIC) User Interface”, offset information for NVIC register mapping updated in Table 12-31 ”Nested Vectored Interrupt Controller (NVIC) Register Mapping”.	8211
	Section 12.9.1 “System Control Block (SCB) User Interface”, deleted lines with MMFSR, BFSR, UFSR and updated the note in Table 12-32, “System Control Block (SCB) Register Mapping”.	
	Table 12-34 ”System Timer (SYST) Register Mapping”: table name updated (SysTick changed to SYST).	
	Harmonized instructions code fonts in Section 12.6 “Cortex-M4 Instruction Set”. Fixed various typos.	8343
	RTT	
	RTC 1Hz calibrated clock feature added in Section 15.1 “Description”, Section 15.4 “Functional Description” and in RTT_MR register, see Section 15.5.1 “Real-time Timer Mode Register”.	
	RTC	
	New bullet “Safety/security features” added in Section 16.2 “Embedded Characteristics”.	8544
	WDT	
	Note added in Section 17.5.3 “Watchdog Timer Status Register”.	8128
	SUPC	
	Offsets updated and SYSC_WPMR in Table 18-1 ”System Controller Registers”. Section 18.4.9 “System Controller Write Protection Mode Register” added.	8253
	Force Wake Up Pin removed from Section 18.1 “Embedded Characteristics”.	8263
	In Section 18.3.3 “Core Voltage Regulator Control/Backup Low-power Mode”, removed informations related to WFE and WFI, deleted reference to 1.8V for voltage regulator.	8363, 8407
	Figure 18-1 Block Diagram updated.	8515
	EEFC	
	In Section 20.5.2 “EEFC Flash Command Register”, table added in FCMD bitfield, details added in table in FARG bitfield.	8352
	Note concerning bit number limitation added in Section 20.4.3.5 “GPNVM Bit”.	8390