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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4s4cb-anr

12.6.11 Miscellaneous Instructions

The table below shows the remaining Cortex-M4 instructions.

Table 12-27. Miscellaneous Instructions

Mnemonic	Description
BKPT	Breakpoint
CPSID	Change Processor State, Disable Interrupts
CPSIE	Change Processor State, Enable Interrupts
DMB	Data Memory Barrier
DSB	Data Synchronization Barrier
ISB	Instruction Synchronization Barrier
MRS	Move from special register to register
MSR	Move from register to special register
NOP	No Operation
SEV	Send Event
SVC	Supervisor Call
WFE	Wait For Event
WFI	Wait For Interrupt

12.8.3.2 Interrupt Clear-enable Registers

Name: NVIC_ICERx [x=0..7]

Access: Read/Write

Reset: 0x000000000

31	30	29	28	27	26	25	24
CLRENA							

23	22	21	20	19	18	17	16
CLRENA							

15	14	13	12	11	10	9	8
CLRENA							

7	6	5	4	3	2	1	0
CLRENA							

These registers disable interrupts, and show which interrupts are enabled.

- **CLRENA: Interrupt Clear-enable**

Write:

0: No effect.

1: Disables the interrupt.

Read:

0: Interrupt disabled.

1: Interrupt enabled.

12.9.1.8 System Handler Priority Registers

The SCB_SHPR1–SCB_SHPR3 registers set the priority level, 0 to of the exception handlers that have configurable priority. They are byte-accessible.

The system fault handlers and the priority field and register for each handler are:

Table 12-33. System Fault Handler Priority Fields

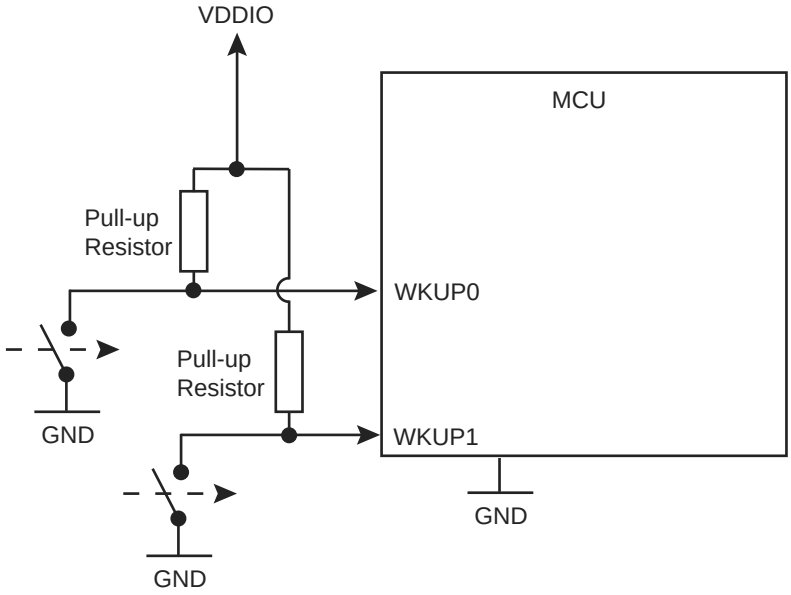
Handler	Field	Register Description
Memory management fault (MemManage)	PRI_4	System Handler Priority Register 1
Bus fault (BusFault)	PRI_5	
Usage fault (UsageFault)	PRI_6	
SVCall	PRI_11	System Handler Priority Register 2
PendSV	PRI_14	System Handler Priority Register 3
SysTick	PRI_15	

Each PRI_N field is 8 bits wide, but the processor implements only bits [7:] of each field, and bits [:0] read as zero and ignore writes.

tamper detection circuitry. If RTCOUTx is not used, the RTC must be configured to create an internal sampling point for the debouncer logic. The period of time between two samples can be configured by programming the TPERIOD field in RTC_MR.

Figure 18-8 illustrates the use of WKUPx without the RTCOUTx pin.

Figure 18-8. Using WKUP Pins Without RTCOUTx Pins



18.4.7.3 Clock Alarms

The RTC and the RTT alarms can generate a wake-up of the core power supply. This can be enabled by setting, respectively, the bits RTCEN and RTTEN in SUPC_WUMR.

The Supply Controller does not provide any status as the information is available in the user interface of either the Real-Time Timer or the Real-Time Clock.

18.4.7.4 Supply Monitor Detection

The supply monitor can generate a wake-up of the core power supply. See Section 18.4.4 ”Supply Monitor”.

The **Memory Write** command **(WRAM)** is optimized for consecutive writes. Write handshaking can be chained; an internal address buffer is automatically increased.

Table 21-14. Write Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	WRAM
2	Write handshaking	ADDR0	Memory Address LSB
3	Write handshaking	ADDR1	Memory Address
4	Write handshaking	DATA	*Memory Address++
5	Write handshaking	DATA	*Memory Address++
...	...	...	...
n	Write handshaking	ADDR0	Memory Address LSB
n+1	Write handshaking	ADDR1	Memory Address
n+2	Write handshaking	DATA	*Memory Address++
n+3	Write handshaking	DATA	*Memory Address++
...	...	...	...

21.3.5.8 Get Version Command

The **Get Version** (GVE) command retrieves the version of the FFPI interface.

Table 21-15. Get Version Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	GVE
2	Read handshaking	DATA	Version

23.6.1 Transfer Address Register

Name: TR_ADDR

Access: Read/Write

31	30	29	28	27	26	25	24
ADDR							
23	22	21	20	19	18	17	16
ADDR							
15	14	13	12	11	10	9	8
ADDR							
7	6	5	4	3	2	1	0
ADDR							

- **ADDR: Transfer Address**

31.6.28 PIO Input Filter Slow Clock Status Register

Name: PIO_IFSCSR

Address: 0x400E0E88 (PIOA), 0x400E1088 (PIOB), 0x400E1288 (PIOC)

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0–P31: Glitch or Debouncing Filter Selection Status**

0: The glitch filter is able to filter glitches with a duration < $t_{peripheral\ clock}/2$.

1: The debouncing filter is able to filter pulses with a duration < $t_{div\_slck}/2$.

31.6.51 PIO Parallel Capture Interrupt Disable Register

Name: PIO_PCIDR

Address: 0x400E0F58 (PIOA), 0x400E1158 (PIOB), 0x400E1358 (PIOC)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	RXBUFF	ENDRX	OVRE	DRDY

The following configuration values are valid for all listed bit names of this register:

0: No effect

1: Disables the corresponding interrupt

- **DRDY: Parallel Capture Mode Data Ready Interrupt Disable**
- **OVRE: Parallel Capture Mode Overrun Error Interrupt Disable**
- **ENDRX: End of Reception Transfer Interrupt Disable**
- **RXBUFF: Reception Buffer Full Interrupt Disable**

32.9.9 SSC Receive Synchronization Holding Register

Name: SSC_RSHR

Address: 0x40004030

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

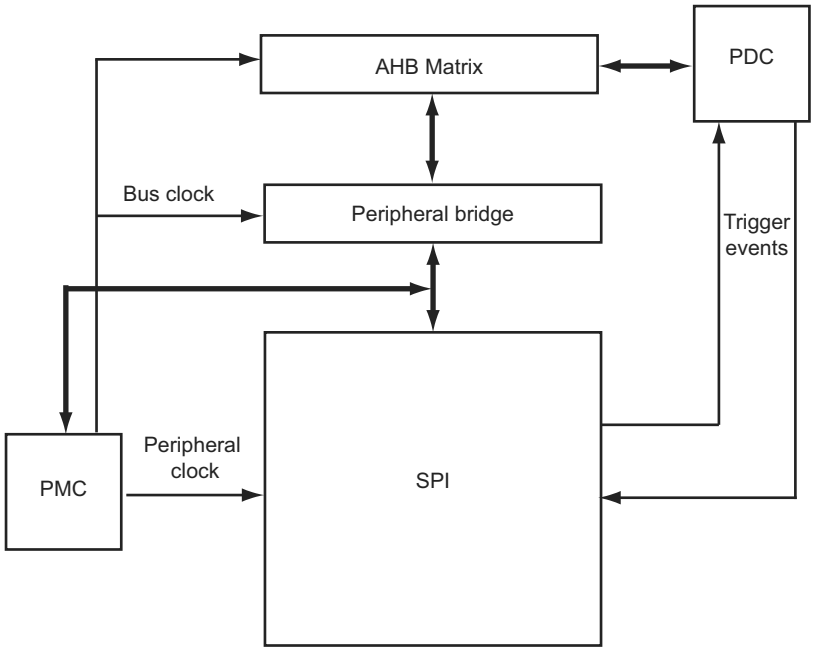
15	14	13	12	11	10	9	8
RSDAT							

7	6	5	4	3	2	1	0
RSDAT							

- **RSDAT: Receive Synchronization Data**

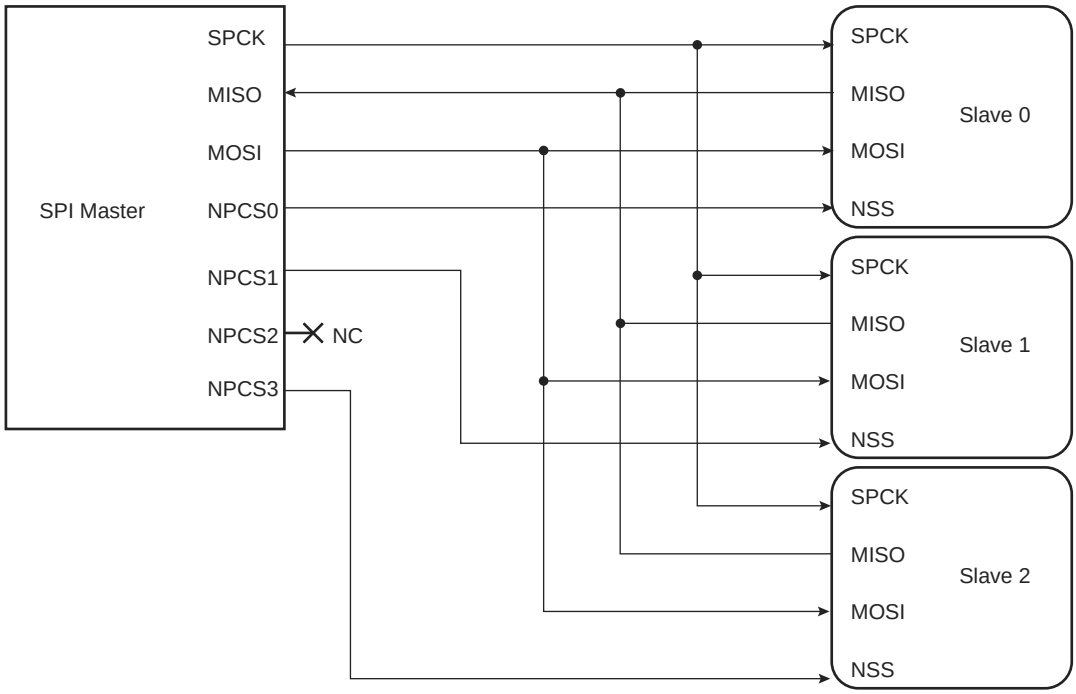
33.3 Block Diagram

Figure 33-1. Block Diagram



33.4 Application Block Diagram

Figure 33-2. Application Block Diagram: Single Master/Multiple Slave Implementation



33.8 Serial Peripheral Interface (SPI) User Interface

Table 33-5. Register Mapping

Offset	Register	Name	Access	Reset
0x00	Control Register	SPI_CR	Write-only	–
0x04	Mode Register	SPI_MR	Read/Write	0x0
0x08	Receive Data Register	SPI_RDR	Read-only	0x0
0x0C	Transmit Data Register	SPI_TDR	Write-only	–
0x10	Status Register	SPI_SR	Read-only	0x000000F0
0x14	Interrupt Enable Register	SPI_IER	Write-only	–
0x18	Interrupt Disable Register	SPI_IDR	Write-only	–
0x1C	Interrupt Mask Register	SPI_IMR	Read-only	0x0
0x20–0x2C	Reserved	–	–	–
0x30	Chip Select Register 0	SPI_CSR0	Read/Write	0x0
0x34	Chip Select Register 1	SPI_CSR1	Read/Write	0x0
0x38	Chip Select Register 2	SPI_CSR2	Read/Write	0x0
0x3C	Chip Select Register 3	SPI_CSR3	Read/Write	0x0
0x40–0xE0	Reserved	–	–	–
0xE4	Write Protection Mode Register	SPI_WPMR	Read/Write	0x0
0xE8	Write Protection Status Register	SPI_WPSR	Read-only	0x0
0xEC–0xF8	Reserved	–	–	–
0xFC	Reserved	–	–	–
0x100–0x124	Reserved for PDC Registers	–	–	–

34.8.1 TWI Control Register

Name: TWI_CR

Address: 0x40018000 (0), 0x4001C000 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
SWRST	QUICK	SVDIS	SVEN	MSDIS	MSEN	STOP	START

- **START: Send a START Condition**

0: No effect.

1: A frame beginning with a START bit is transmitted according to the features defined in the TWI Master Mode Register (TWI_MMR).

This action is necessary for the TWI to read data from a slave. When configured in Master mode with a write operation, a frame is sent as soon as the user writes a character in the Transmit Holding Register (TWI_THR).

- **STOP: Send a STOP Condition**

0: No effect.

1: STOP condition is sent just after completing the current byte transmission in Master read mode.

– In single data byte master read, the START and STOP must both be set.

– In multiple data bytes master read, the STOP must be set after the last data received but one.

– In Master read mode, if a NACK bit is received, the STOP is automatically performed.

– In master data write operation, a STOP condition is sent when transmission of the current data has ended.

- **MSEN: TWI Master Mode Enabled**

0: No effect.

1: Enables the Master mode (MSDIS must be written to 0).

Note: Switching from Slave to Master mode is only permitted when TXCOMP = 1.

- **MSDIS: TWI Master Mode Disabled**

0: No effect.

1: The Master mode is disabled, all pending data is transmitted. The shifter and holding characters (if it contains data) are transmitted in case of write operation. In read operation, the character being transferred must be completely received before disabling.

34.8.6 TWI Status Register

Name: TWI_SR

Address: 0x40018020 (0), 0x4001C020 (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TXBUFE	RXBUFF	ENDTX	ENDRX	EOSACC	SCLWS	ARBLST	NACK

7	6	5	4	3	2	1	0
–	OVRE	GACC	SVACC	SVREAD	TXRDY	RXRDY	TXCOMP

- **TXCOMP: Transmission Completed (cleared by writing TWI_THR)**

TXCOMP used in Master mode:

0: During the length of the current frame.

1: When both holding register and internal shifter are empty and STOP condition has been sent.

TXCOMP behavior in Master mode can be seen in Figure 34-7 and in Figure 34-9.

TXCOMP used in Slave mode:

0: As soon as a START is detected.

1: After a STOP or a REPEATED START + an address different from SADR is detected.

TXCOMP behavior in Slave mode can be seen in Figure 34-27, Figure 34-28, Figure 34-29 and Figure 34-30.

- **RXRDY: Receive Holding Register Ready (cleared by reading TWI_RHR)**

0: No character has been received since the last TWI_RHR read operation.

1: A byte has been received in the TWI_RHR since the last read.

RXRDY behavior in Master mode can be seen in Figure 34-9.

RXRDY behavior in Slave mode can be seen in Figure 34-25, Figure 34-28, Figure 34-29 and Figure 34-30.

- **TXRDY: Transmit Holding Register Ready (cleared by writing TWI_THR)**

TXRDY used in Master mode:

0: The transmit holding register has not been transferred into internal shifter. Set to 0 when writing into TWI_THR.

1: As soon as a data byte is transferred from TWI_THR to internal shifter or if a NACK error is detected, TXRDY is set at the same time as TXCOMP and NACK. TXRDY is also set when MSEN is set (enable TWI).

TXRDY behavior in Master mode can be seen in Figure 34.7.3.4.

TXRDY used in Slave mode:

0: As soon as data is written in the TWI_THR, until this data has been transmitted and acknowledged (ACK or NACK).

1: It indicates that the TWI_THR is empty and that data has been transmitted and acknowledged.

If STTTO is performed, the counter clock is stopped until a first character is received. The idle state on RXD before the start of the frame does not provide a time-out. This prevents having to obtain a periodic interrupt and enables a wait of the end of frame when the idle state on RXD is detected.

If RETTO is performed, the counter starts counting down immediately from the value TO. This enables generation of a periodic interrupt so that a user time-out can be handled, for example when no key is pressed on a keyboard.

Figure 36-23 shows the block diagram of the Receiver Time-out feature.

Figure 36-23. Receiver Time-out Block Diagram

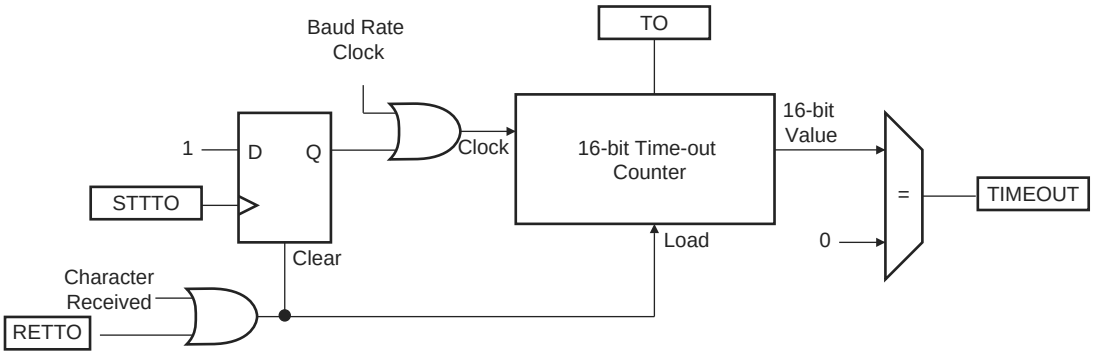


Table 36-10 gives the maximum time-out period for some standard baud rates.

Table 36-10. Maximum Time-out Period

Baud Rate (bit/s)	Bit Time (µs)	Time-out (ms)
600	1,667	109,225
1,200	833	54,613
2,400	417	27,306
4,800	208	13,653
9,600	104	6,827
14,400	69	4,551
19,200	52	3,413
28,800	35	2,276
38,400	26	1,704
56,000	18	1,170
57,600	17	1,138
200,000	5	328

36.6.3.12 Framing Error

The receiver is capable of detecting framing errors. A framing error happens when the stop bit of a received character is detected at level 0. This can occur if the receiver and the transmitter are fully desynchronized.

A framing error is reported on the FRAME bit of US_CSR. The FRAME bit is asserted in the middle of the stop bit as soon as the framing error is detected. It is cleared by writing a 1 to the RSTSTA bit in the US_CR.

38.14.19HSMCI FIFOx Memory Aperture

Name: HSMCI_FIFOx [x=0..255]

Address: 0x40000200

Access: Read/Write

31	30	29	28	27	26	25	24
DATA							
23	22	21	20	19	18	17	16
DATA							
15	14	13	12	11	10	9	8
DATA							
7	6	5	4	3	2	1	0
DATA							

- **DATA: Data to Read or Data to Write**

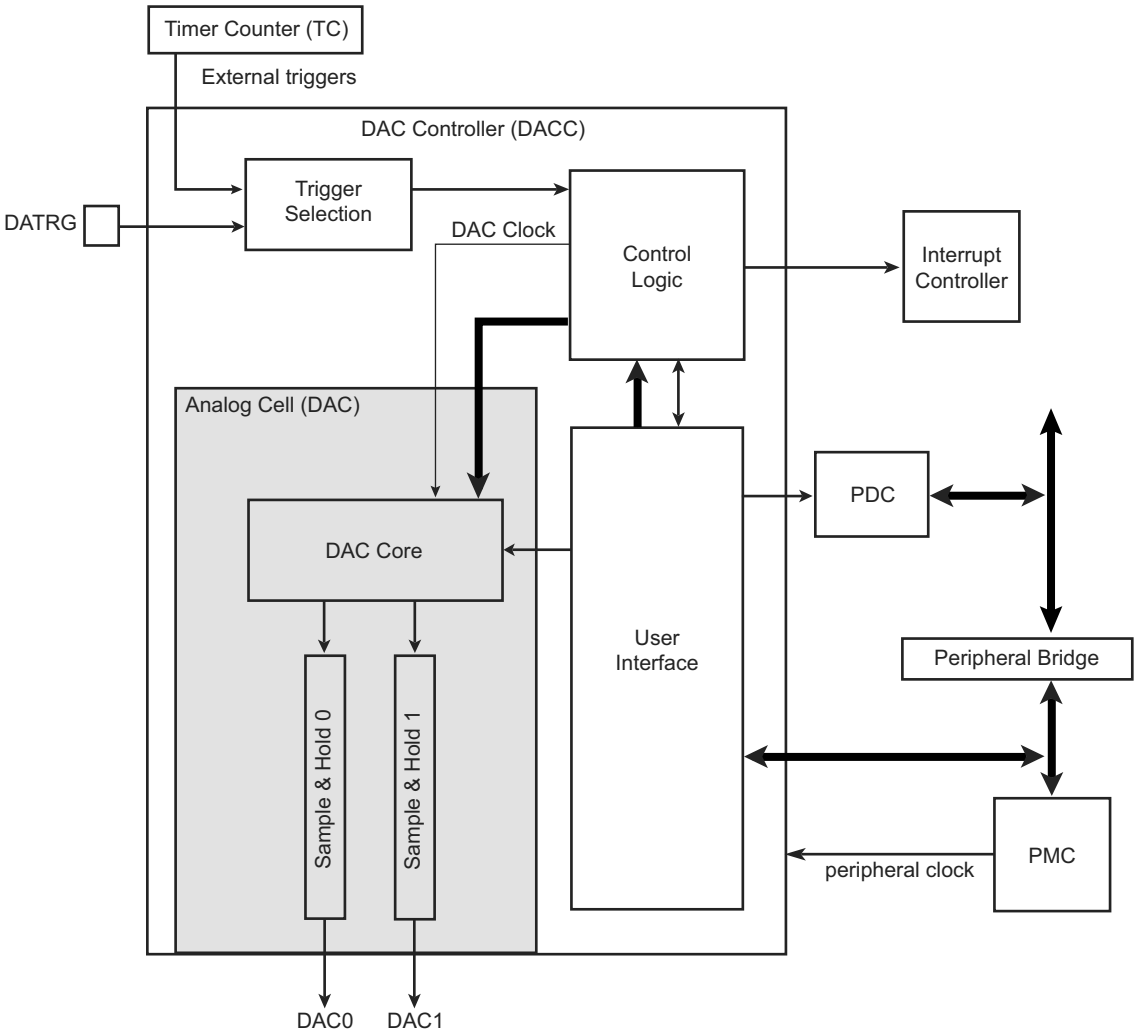
Table 39-6. Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x1AC	PWM Comparison 7 Mode Update Register	PWM_CMPMUPD7	Write-only	–
0x1B0–0x1FC	Reserved	–	–	–
0x200 + ch_num * 0x20 + 0x00	PWM Channel Mode Register(1)	PWM_CMR	Read/Write	0x0
0x200 + ch_num * 0x20 + 0x04	PWM Channel Duty Cycle Register(1)	PWM_CDTY	Read/Write	0x0
0x200 + ch_num * 0x20 + 0x08	PWM Channel Duty Cycle Update Register(1)	PWM_CDTYUPD	Write-only	–
0x200 + ch_num * 0x20 + 0x0C	PWM Channel Period Register(1)	PWM_CPRD	Read/Write	0x0
0x200 + ch_num * 0x20 + 0x10	PWM Channel Period Update Register(1)	PWM_CPRDUPD	Write-only	–
0x200 + ch_num * 0x20 + 0x14	PWM Channel Counter Register(1)	PWM_CCNT	Read-only	0x0
0x200 + ch_num * 0x20 + 0x18	PWM Channel Dead Time Register(1)	PWM_DT	Read/Write	0x0
0x200 + ch_num * 0x20 + 0x1C	PWM Channel Dead Time Update Register(1)	PWM_DTUPD	Write-only	–

Notes: 1. Some registers are indexed with “ch_num” index ranging from 0 to 3.

43.3 Block Diagram

Figure 43-1. DACC Block Diagram



43.4 Signal Description

Table 43-1. DACC Pin Description

Pin Name	Description
DAC0–DAC1	Analog output channels
DATRG	External triggers

43.5 Product Dependencies

43.5.1 Power Management

The user must first enable the DAC Controller Clock in the Power Management Controller (PMC) before using the DACC.

The DACC becomes active as soon as a conversion is requested and at least one channel is enabled. The DACC is automatically deactivated when no channels are enabled.

44.9 12-bit DAC Characteristics

Table 44-56. Analog Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDIN}	Analog Supply		2.4	3.0	3.6	V
I_{VDDIN}	Current Consumption	Sleep Mode (Clock OFF)	–		3	µA
		Fast Wake Up (Standby Mode, clock ON)	–	2	3	mA
		Normal Mode with 1 output ON (DACC_ACR.IBCTLDACCORE = 01, DACC_ACR.IBCTLCHx = 10)	–	4.3	5.6	mA
		Normal Mode with 2 outputs ON (DACC_ACR.IBCTLDACCORE = 01, DACC_ACR.IBCTLCHx = 10)	–	5	6.5	mA

Table 44-57. Channel Conversion Time and DAC Clock

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DAC}	Clock Frequency		1	–	50	MHz
t_{CP_DAC}	Clock Period		–	–	20	ns
$t_{REFRESH}$	Refresh Time	8-bit Accuracy	24	–	–	us
t_{START}	Startup Time	From Sleep Mode to Normal Mode: - Voltage reference OFF - DAC core OFF	20	30	40	µs
		From Fast Wake Up to Normal Mode: - Voltage reference ON - DAC core OFF	2.5	3.75	5	
t_{CONV}	Conversion Time		–	–	25	t_{CP_DAC}

External voltage reference for DAC is V_{ADVREF}. See the ADC voltage reference characteristics in Table 44-40 on page 1173.

Table 44-58. Static Performance Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
	Resolution	DAC Clock (f_{DAC}) = 5 MHz, f_S = 200 kHz, ADC_ACR.IBCTL = 01	–	–	12	–	bit
INL	Integral Non-linearity		2.4V < V_{DDIN} < 2.7V	-6	–	+6	LSB
			2.7V < V_{DDIN} < 3.6V	-2	±1	+2	
DNL	Differential Non-linearity		2.4V < V_{DDIN} < 2.7V	-2.5	±1	+2.5	LSB
			2.7V < V_{DDIN} < 3.6V				
E_O	Offset Error		–	-32	±8	32	LSB
E_G	Gain Error		–	-32	±2	32	LSB

47. Ordering Information

Devices in TFBGA, VFBGA, LQFP and QFN packages can be ordered in trays or in tape and reel. Devices in a WLCSP package are available in tape and reel only.

Table 47-1 provides ordering codes for tray packing. For tape and reel, append an ‘R’ to the tray ordering code; e.g., ATSAM4SD32CA-CUR.

Table 47-1. Ordering Codes for SAM4S Devices

Ordering Code	MRL	Flash (Kbytes)	SRAM (Kbytes)	Package	Carrier Type	Operating Temperature Range
ATSAM4SD32CA-CU	A	2*1024	160	TFBGA100	Tray	Industrial (-40°C to +85°C)
ATSAM4SD32CB-CU	B					
ATSAM4SD32CA-CFU	A	2*1024	160	VFBGA100	Tray	Industrial (-40°C to +85°C)
ATSAM4SD32CB-CFU	B					
ATSAM4SD32CA-AU	A	2*1024	160	LQFP100	Tray	Industrial (-40°C to +85°C)
ATSAM4SD32CB-AU	B					
ATSAM4SD32CA-AN	A	2*1024	160	LQFP100	Tray	Industrial (-40°C to +105°C)
ATSAM4SD32CB-AN	B					
ATSAM4SD32BA-MU	A	2*1024	160	QFN64	Tray	Industrial (-40°C to +85°C)
ATSAM4SD32BB-MU	B					
ATSAM4SD32BA-AU	A	2*1024	160	LQFP64	Tray	Industrial (-40°C to +85°C)
ATSAM4SD32BB-AU	B					
ATSAM4SD32BA-AN	A	2*1024	160	LQFP64	Tray	Industrial (-40°C to +105°C)
ATSAM4SD32BB-AN	B					
ATSAM4SD32BA-UUR	A	2*1024	160	WLCSP64	Tape and reel	Industrial (-40°C to +85°C)
ATSAM4SD32BB-UUR	B					
ATSAM4SD16CA-CU	A	2*512	160	TFBGA100	Tray	Industrial (-40°C to +85°C)
ATSAM4SD16CB-CU	B					
ATSAM4SD16CA-CFU	A	2*512	160	VFBGA100	Tray	Industrial (-40°C to +85°C)
ATSAM4SD16CB-CFU	B					
ATSAM4SD16CA-AU	A	2*512	160	LQFP100	Tray	Industrial (-40°C to +85°C)
ATSAM4SD16CB-AU	B					
ATSAM4SD16CA-AN	A	2*512	160	LQFP100	Tray	Industrial (-40°C to +105°C)
ATSAM4SD16CB-AN	B					
ATSAM4SD16BA-MU	A	2*512	160	QFN64	Tray	Industrial (-40°C to +85°C)
ATSAM4SD16BB-MU	B					
ATSAM4SD16BA-AU	A	2*512	160	LQFP64	Tray	Industrial (-40°C to +85°C)
ATSAM4SD16BB-AU	B					
ATSAM4SD16BA-AN	A	2*512	160	LQFP64	Tray	Industrial (-40°C to +105°C)
ATSAM4SD16BB-AN	B					

48.2 Errata SAM4SD32/SD16/SA16/S16/S8 Rev. B Parts

The errata are applicable to the devices in Table 48-1.

Table 48-2. Device List for Errata Described in Section 48.1

Device Name	Revision	Chip ID
SAM4SD32C	B	0x29A7_0EE1
SAM4SD32B	B	0x2997_0EE1
SAM4SD16C	B	0x29A7_0CE1
SAM4SD16B	B	0x2997_0CE1
SAM4SA16C	B	0x28A7_0CE1
SAM4SA16B	B	0x2897_0CE1
SAM4S16C	B	0x28AC_0CE1
SAM4S16B	B	0x289C_0CE1
SAM4S8C	B	0x28AC_0AE1
SAM4S8B	B	0x289C_0AE1

48.2.1 Flash Controller (EEFC)

Issue: Flash Buffer Not Cleared

The Write Buffer in the embedded Flash is not cleared after trying to write to a locked region. Therefore, the data that was previously loaded into the Write Buffer would remain in the buffer while the next page write command (e.g., WP) is being executed.

Workaround: Do not do partial programming (Fill completely the Write Buffer). Note that this problem occurs only if the software tries to write into a locked region.

Issue: Code Loop Optimization Cannot Be Disabled

The EFC does not work after the buffer for loop optimization is disabled, in Flash Mode Register (EEFC_FMR) CLOE = 0.

Workaround: The CLOE bit must be kept at 1.

Issue: Erase Sector Command Cannot Be Performed If a Subsector Is Locked (ONLY in Flash Sector0)

If one of subsector (Small Sector 0, Small Sector1 and Larger Sector) is locked, the Erase Sector Command (ES) is not possible on non-locked subsectors.

Workaround: All the lock bits of the sector0 must be cleared prior to issuing the ES command. After the ES command has been issued, the first sector lock bits must be reverted to the state before clearing them.