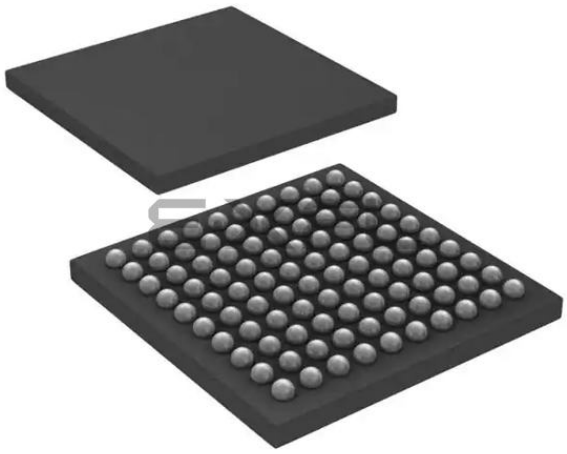

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4s4cb-cfnr

4.2.4 64-lead LQFP and QFN Pinout

Table 4-4. 64-pin SAM4SD32/SD16/SA16/S16/S8/S4/S2 Pinout

1	ADVREF	17	GND	33	TDI/PB4	49	TDO/TRACESWO/PB5
2	GND	18	VDDIO	34	PA6/PGMNOE	50	JTAGSEL
3	PB0/AD4	19	PA16/PGMD4	35	PA5/PGMRDY	51	TMS/SWDIO/PB6
4	PB1/AD5	20	PA15/PGMD3	36	PA4/PGMNCMD	52	PA31
5	PB2/AD6	21	PA14/PGMD2	37	PA27/PGMD15	53	TCK/SWCLK/PB7
6	PB3/AD7	22	PA13/PGMD1	38	PA28	54	VDDCORE
7	VDDIN	23	PA24/PGMD12	39	NRST	55	ERASE/PB12
8	VDDOUT	24	VDDCORE	40	TST	56	DDM/PB10
9	PA17/PGMD5/AD0	25	PA25/PGMD13	41	PA29	57	DDP/PB11
10	PA18/PGMD6/AD1	26	PA26/PGMD14	42	PA30	58	VDDIO
11	PA21/PGMD9/AD8	27	PA12/PGMD0	43	PA3	59	PB13/DAC0
12	VDDCORE	28	PA11/PGMM3	44	PA2/PGMEN2	60	GND
13	PA19/PGMD7/AD2	29	PA10/PGMM2	45	VDDIO	61	XOUT/PB8
14	PA22/PGMD10/AD9	30	PA9/PGMM1	46	GND	62	XIN/PGMCK/PB9
15	PA23/PGMD11	31	PA8/XOUT32/PGMM0	47	PA1/PGMEN1	63	PB14/DAC1
16	PA20/PGMD8/AD3	32	PA7/XIN32/PGMNVALID	48	PA0/PGMEN0	64	VDDPLL

Note: The bottom pad of the QFN package must be connected to ground.

12.4.1.12 Exception Mask Registers

The exception mask registers disable the handling of exceptions by the processor. Disable exceptions where they might impact on timing critical tasks.

To access the exception mask registers use the MSR and MRS instructions, or the CPS instruction to change the value of PRIMASK or FAULTMASK. See “MRS” , “MSR” , and “CPS” for more information.

12.4.1.13 Priority Mask Register

Name: PRIMASK

Access: Read/Write

Reset: 0x000000000

31	30	29	28	27	26	25	24
–							

23	22	21	20	19	18	17	16
–							

15	14	13	12	11	10	9	8
–							

7	6	5	4	3	2	1	0
–							PRIMASK

The PRIMASK register prevents the activation of all exceptions with a configurable priority.

- **PRIMASK**

0: No effect

1: Prevents the activation of all exceptions with a configurable priority.

```
ITT     EQ                  ; IT instruction for STREXEQ and CMPEQ
STREXEQ R0, R1, [LockAddr]  ; Try and claim the lock
CMPEQ   R0, #0              ; Did this succeed?
BNE     try                 ; No – try again
....                        ; Yes – we have the lock
```

12.6.4.9 CLREX

Clear Exclusive.

Syntax

`CLREX{`*cond*`}`

where:

cond is an optional condition code, see “Conditional Execution” .

Operation

Use CLREX to make the next STREX, STREXB, or STREXH instruction write a 1 to its destination register and fail to perform the store. It is useful in exception handler code to force the failure of the store exclusive if the exception occurs between a load exclusive instruction and the matching store exclusive instruction in a synchronization operation.

See “Synchronization Primitives” for more information.

Condition Flags

These instructions do not change the flags.

Examples

```
CLREX
```

The **Memory Write** command **(WRAM)** is optimized for consecutive writes. Write handshaking can be chained; an internal address buffer is automatically increased.

Table 21-14. Write Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	WRAM
2	Write handshaking	ADDR0	Memory Address LSB
3	Write handshaking	ADDR1	Memory Address
4	Write handshaking	DATA	*Memory Address++
5	Write handshaking	DATA	*Memory Address++
...	...	...	...
n	Write handshaking	ADDR0	Memory Address LSB
n+1	Write handshaking	ADDR1	Memory Address
n+2	Write handshaking	DATA	*Memory Address++
n+3	Write handshaking	DATA	*Memory Address++
...	...	...	...

21.3.5.8 Get Version Command

The **Get Version** (GVE) command retrieves the version of the FFPI interface.

Table 21-15. Get Version Command

Step	Handshake Sequence	MODE[3:0]	DATA[15:0]
1	Write handshaking	CMDE	GVE
2	Read handshaking	DATA	Version

23.7.11 CRCCU Status Register

Name: CRCCU_SR

Address: 0x4004403C

Access: Read-only

31	30	29	28	27	26	25	24
CRC							
23	22	21	20	19	18	17	16
CRC							
15	14	13	12	11	10	9	8
CRC							
7	6	5	4	3	2	1	0
CRC							

- **CRC: Cyclic Redundancy Check Value**

This register can not be read if the COMPARE bit in the CRCCU_MR is set to true.

26.15 Asynchronous Page Mode

The SMC supports asynchronous burst reads in Page mode, providing that the Page mode is enabled in the SMC_MODE register (PMEN field). The page size must be configured in the SMC_MODE register (PS field) to 4, 8, 16 or 32 bytes.

The page defines a set of consecutive bytes into memory. A 4-byte page (resp. 8-, 16-, 32-byte page) is always aligned to 4-byte boundaries (resp. 8-, 16-, 32-byte boundaries) of memory. The MSB of data address defines the address of the page in memory, the LSB of address define the address of the data in the page as detailed in Table 26-7.

With Page mode memory devices, the first access to one page (t_{pa}) takes longer than the subsequent accesses to the page (t_{sa}) as shown in Figure 26-31. When in Page mode, the SMC enables the user to define different read timings for the first access within one page, and next accesses within the page.

Table 26-7. Page Address and Data Address within a Page

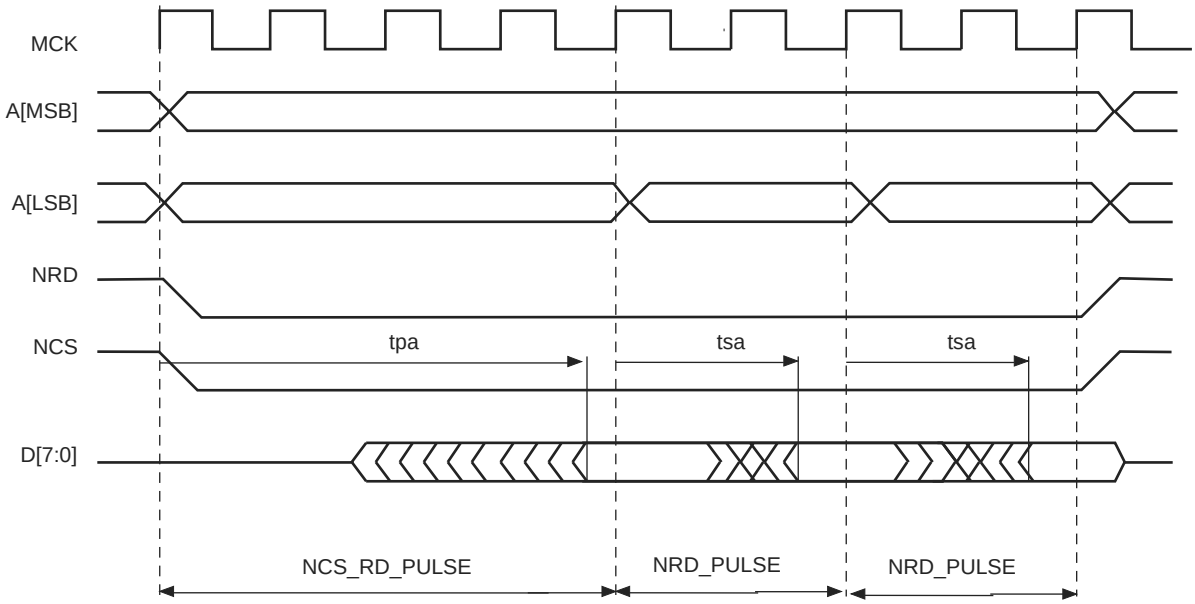
Page Size	Page Address(1)	Data Address in the Page
4 bytes	A[23:2]	A[1:0]
8 bytes	A[23:3]	A[2:0]
16 bytes	A[23:4]	A[3:0]
32 bytes	A[23:5]	A[4:0]

Note: 1. “A” denotes the address bus of the memory device.

26.15.1 Protocol and Timings in Page Mode

Figure 26-31 shows the NRD and NCS timings in Page mode access.

Figure 26-31. Page Mode Read Protocol (Address MSB and LSB are defined in Table 26-7)



The NRD and NCS signals are held low during all read transfers, whatever the programmed values of the setup and hold timings in the User Interface may be. Moreover, the NRD and NCS timings are identical. The pulse length of the first access to the page is defined with the NCS_RD_PULSE field of the SMC_PULSE register. The pulse length of subsequent accesses within the page are defined using the NRD_PULSE parameter.

31.6.23 PIO Pull-Up Status Register

Name: PIO_PUSR

Address: 0x400E0E68 (PIOA), 0x400E1068 (PIOB), 0x400E1268 (PIOC)

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0–P31: Pull-Up Status**

0: Pull-up resistor is enabled on the I/O line.

1: Pull-up resistor is disabled on the I/O line.

31.6.48 PIO Schmitt Trigger Register

Name: PIO_SCHMITT

Address: 0x400E0F00 (PIOA), 0x400E1100 (PIOB), 0x400E1300 (PIOC)

Access: Read/Write

31	30	29	28	27	26	25	24
SCHMITT31	SCHMITT30	SCHMITT29	SCHMITT28	SCHMITT27	SCHMITT26	SCHMITT25	SCHMITT24
23	22	21	20	19	18	17	16
SCHMITT23	SCHMITT22	SCHMITT21	SCHMITT20	SCHMITT19	SCHMITT18	SCHMITT17	SCHMITT16
15	14	13	12	11	10	9	8
SCHMITT15	SCHMITT14	SCHMITT13	SCHMITT12	SCHMITT11	SCHMITT10	SCHMITT9	SCHMITT8
7	6	5	4	3	2	1	0
SCHMITT7	SCHMITT6	SCHMITT5	SCHMITT4	SCHMITT3	SCHMITT2	SCHMITT1	SCHMITT0

- **SCHMITTx [x=0..31]: Schmitt Trigger Control**

0: Schmitt trigger is enabled.

1: Schmitt trigger is disabled.

- **FSOS: Receive Frame Sync Output Selection**

Value	Name	Description
0	NONE	None, RF pin is an input
1	NEGATIVE	Negative Pulse, RF pin is an output
2	POSITIVE	Positive Pulse, RF pin is an output
3	LOW	Driven Low during data transfer, RF pin is an output
4	HIGH	Driven High during data transfer, RF pin is an output
5	TOGGLING	Toggling at each start of data transfer, RF pin is an output

- **FSEDGE: Frame Sync Edge Detection**

Determines which edge on Frame Sync will generate the interrupt RXSYN in the SSC Status Register.

Value	Name	Description
0	POSITIVE	Positive Edge Detection
1	NEGATIVE	Negative Edge Detection

- **FSLEN_EXT: FSLEN Field Extension**

Extends FSLEN field. For details, refer to FSLEN bit description on page 664.

32.9.12 SSC Receive Compare 1 Register

Name: SSC_RC1R

Address: 0x4000403C

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
CP1							

7	6	5	4	3	2	1	0
CP1							

This register can only be written if the WPEN bit is cleared in the SSC Write Protection Mode Register.

- **CP1: Receive Compare Data 1**

- **RXBUFF: Receive Buffer Full Interrupt Enable**

0: No effect.

1: Enables the Receive Buffer Full Interrupt.

- **CP0: Compare 0 Interrupt Enable**

0: No effect.

1: Enables the Compare 0 Interrupt.

- **CP1: Compare 1 Interrupt Enable**

0: No effect.

1: Enables the Compare 1 Interrupt.

- **TXSYN: Tx Sync Interrupt Enable**

0: No effect.

1: Enables the Tx Sync Interrupt.

- **RXSYN: Rx Sync Interrupt Enable**

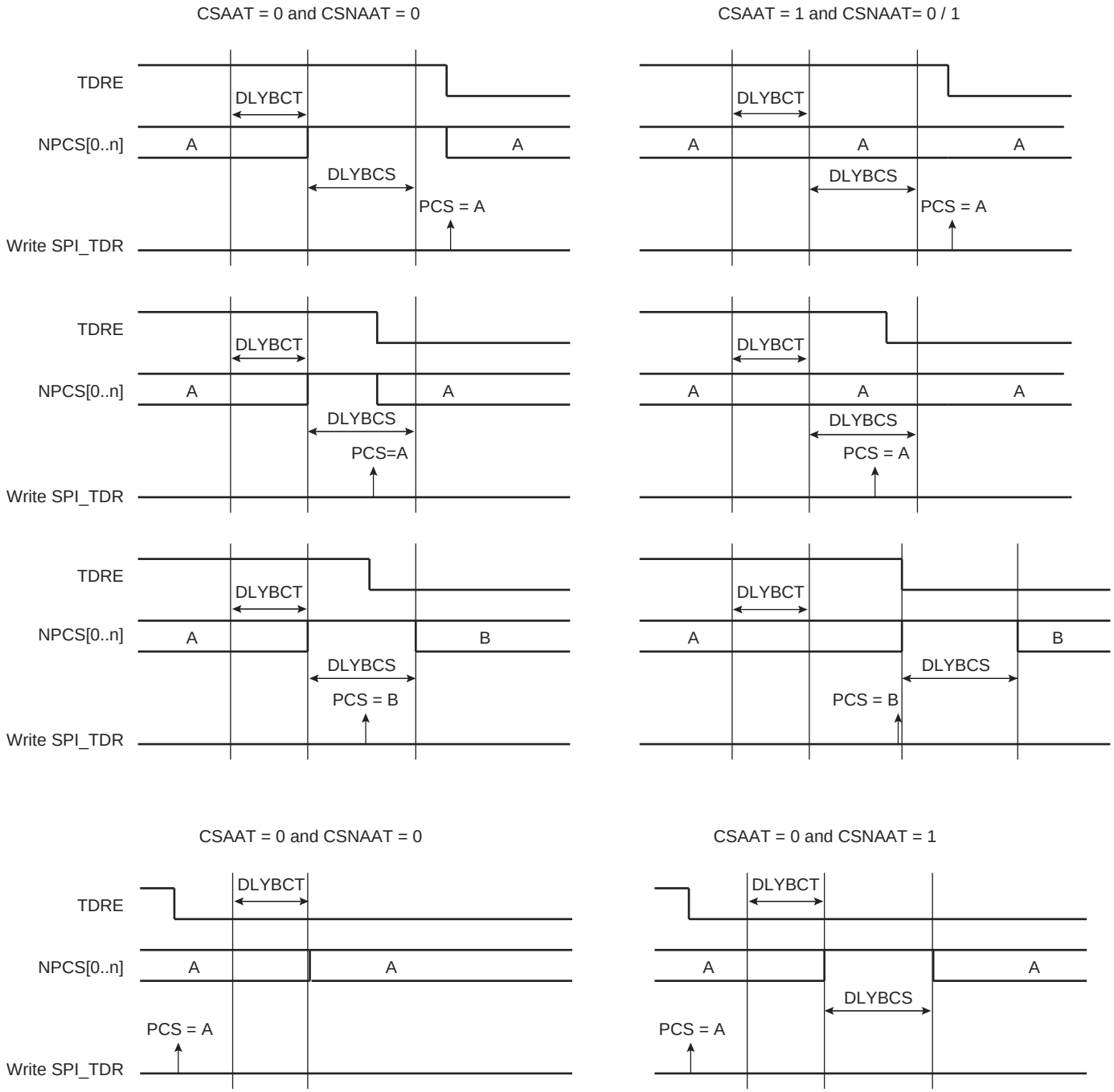
0: No effect.

1: Enables the Rx Sync Interrupt.

interfacing with such devices, the SPI_CSR can be programmed with the Chip Select Not Active After Transfer (CSNAAT) bit to 1. This allows the chip select lines to be de-asserted systematically during a time “DLYBCS” (the value of the CSNAAT bit is processed only if the CSAAT bit is configured to 0 for the same chip select).

Figure 33-12 shows different peripheral deselection cases and the effect of the CSAAT and CSNAAT bits.

Figure 33-12. Peripheral Deselection



33.7.3.10 Mode Fault Detection

The SPI has the capability to operate in multi-master environment. Consequently, the NPCS0/NSS line must be monitored. If one of the masters on the SPI bus is currently transmitting, the NPCS0/NSS line is low and the SPI must not transmit any data. A mode fault is detected when the SPI is programmed in Master mode and a low level

- **TXBUFE: TX Buffer Empty (cleared by writing SPI_TCR or SPI_TNCR)**

0: SPI_TCR(1) or SPI_TNCR(1) has a value other than 0.

1: Both SPI_TCR(1) and SPI_TNCR(1) have a value of 0.

- **NSSR: NSS Rising (cleared on read)**

0: No rising edge detected on NSS pin since the last read of SPI_SR.

1: A rising edge occurred on NSS pin since the last read of SPI_SR.

- **TXEMPTY: Transmission Registers Empty (cleared by writing SPI_TDR)**

0: As soon as data is written in SPI_TDR.

1: SPI_TDR and internal shift register are empty. If a transfer delay has been defined, TXEMPTY is set after the end of this delay.

- **UNDES: Underrun Error Status (Slave mode only) (cleared on read)**

0: No underrun has been detected since the last read of SPI_SR.

1: A transfer starts whereas no data has been loaded in SPI_TDR.

- **SPIENS: SPI Enable Status**

0: SPI is disabled.

1: SPI is enabled.

Note: 1. SPI_RCR, SPI_RNCR, SPI_TCR, SPI_TNCR are PDC registers.

CPOL is used to determine the inactive state value of the serial clock (SPCK). It is used with CPHA to produce the required clock/data relationship between master and slave devices.

- **CLKO: Clock Output Select**

0: The USART does not drive the SCK pin.

1: The USART drives the SCK pin if USCLKS does not select the external clock SCK.

- **WRDBT: Wait Read Data Before Transfer**

0: The character transmission starts as soon as a character is written into US_THR (assuming TXRDY was set).

1: The character transmission starts when a character is written and only if RXRDY flag is cleared (Receive Holding Register has been read).

38.14.16HSMCI Configuration Register

Name: HSMCI_CFG

Address: 0x40000054

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	LSYNC	–	–	–	HSMODE
7	6	5	4	3	2	1	0
–	–	–	FERRCTRL	–	–	–	FIFOMODE

This register can only be written if the WPEN bit is cleared in the HSMCI Write Protection Mode Register.

- **FIFOMODE: HSMCI Internal FIFO control mode**

0: A write transfer starts when a sufficient amount of data is written into the FIFO.

When the block length is greater than or equal to 3/4 of the HSMCI internal FIFO size, then the write transfer starts as soon as half the FIFO is filled. When the block length is greater than or equal to half the internal FIFO size, then the write transfer starts as soon as one quarter of the FIFO is filled. In other cases, the transfer starts as soon as the total amount of data is written in the internal FIFO.

1: A write transfer starts as soon as one data is written into the FIFO.

- **FERRCTRL: Flow Error flag reset control mode**

0: When an underflow/overflow condition flag is set, a new Write/Read command is needed to reset the flag.

1: When an underflow/overflow condition flag is set, a read status resets the flag.

- **HSMODE: High Speed Mode**

0: Default bus timing mode.

1: If set to one, the host controller outputs command line and data lines on the rising edge of the card clock. The Host driver shall check the high speed support in the card registers.

- **LSYNC: Synchronize on the last block**

0: The pending command is sent at the end of the current data block.

1: The pending command is sent at the end of the block transfer when the transfer length is not infinite (block count shall be different from zero).

- **RXSETUP: Received Setup**

This flag generates an interrupt while it is set to one.

Read:

0: No setup packet available.

1: A setup data packet has been sent by the host and is available in the FIFO.

Write:

0: Device firmware notifies the USB peripheral device that it has read the setup data in the FIFO.

1: No effect.

This flag is used to notify the USB device firmware that a valid Setup data packet has been sent by the host and successfully received by the USB device. The USB device firmware may transfer Setup data from the FIFO by reading the UDP_FDRx to the microcontroller memory. Once a transfer has been done, RXSETUP must be cleared by the device firmware.

Ensuing Data OUT transaction is not accepted while RXSETUP is set.

- **ISOERROR: A CRC error has been detected in an isochronous transfer**

This flag generates an interrupt while it is set to one.

Read:

0: No error in the previous isochronous transfer.

1: CRC error has been detected, data available in the FIFO are corrupted.

Write:

0: Resets the ISOERROR flag, clears the interrupt.

1: No effect.

- **TXPKTRDY: Transmit Packet Ready**

This flag is cleared by the USB device.

This flag is set by the USB device firmware.

Read:

0: There is no data to send.

1: The data is waiting to be sent upon reception of token IN.

Write:

0: Can be used in the procedure to cancel transmission data. (See Section 40.6.2.5 “Transmit Data Cancellation” on page 1041)

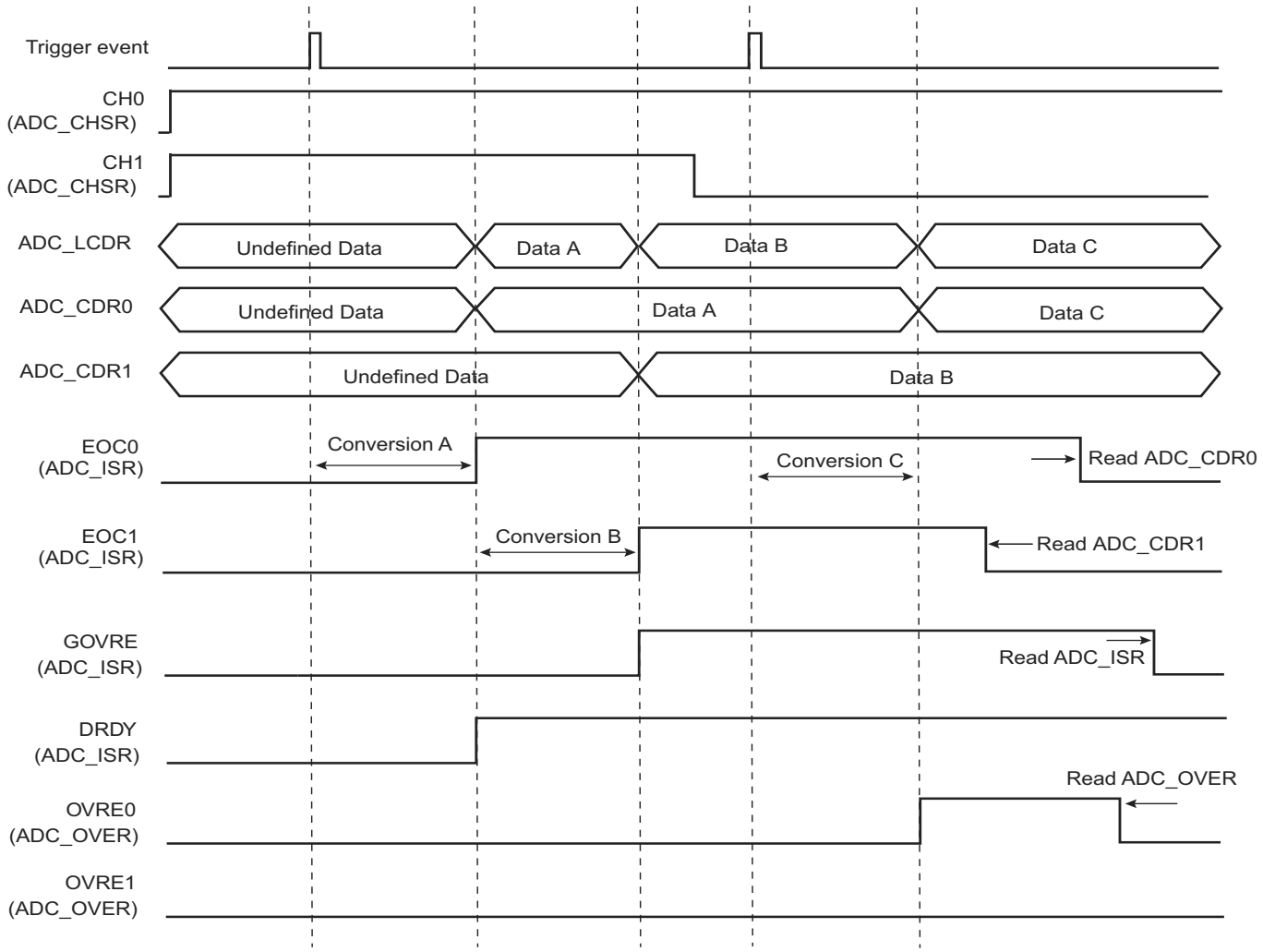
1: A new data payload has been written in the FIFO by the firmware and is ready to be sent.

This flag is used to generate a Data IN transaction (device to host). Device firmware checks that it can write a data payload in the FIFO, checking that TXPKTRDY is cleared. Transfer to the FIFO is done by writing in the UDP_FDRx. Once the data payload has been transferred to the FIFO, the firmware notifies the USB device setting TXPKTRDY to one. USB bus transactions can start. TXCOMP is set once the data payload has been received by the host.

After setting or clearing this bit, a wait time of 3 UDPCK clock cycles and 3 peripheral clock cycles is required before accessing DPR.

The OVREx flag is automatically cleared when ADC_OVER is read, and the GOVRE flag is automatically cleared when ADC_ISR is read.

Figure 42-5. EOCx, OVREx and GOVREx Flag Behavior



Warning: If the corresponding channel is disabled during a conversion or if it is disabled and then reenabled during a conversion, its associated data and corresponding EOCx and GOVRE flags in ADC_ISR and OVREx flags in ADC_OVER are unpredictable.

44.12 AC Characteristics

44.12.1 Master Clock Characteristics

Table 44-63. Master Clock Waveform Parameters

Symbol	Parameter	Conditions	Min	Max	Unit
$1/(t_{CPMCK})$	Master Clock Frequency	VDDCORE @ 1.20V	–	120	MHz
		VDDCORE @ 1.08V	–	100	

44.12.2 I/O Characteristics

Criteria used to define the maximum frequency of the I/Os:

- Output duty cycle (40%–60%)
- Minimum output swing: 100 mV to V_{DDIO} - 100 mV
- Minimum output swing: 100 mV to V_{DDIO} - 100 mV
- Addition of rising and falling time inferior to 75% of the period

Table 44-64. I/O Characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
FreqMax1	Pin Group 1(1) Maximum Output Frequency	10 pF	V_{DDIO} = 1.62V	–	70	MHz
		30 pF		–	45	
PulseminH1	Pin Group 1(1) High Level Pulse Width	10 pF		–	–	ns
		30 pF		11	–	
PulseminL1	Pin Group 1(1) Low Level Pulse Width	10 pF		7.2	–	ns
		30 pF		11	–	
FreqMax2	Pin Group 2(2) Maximum Output Frequency	10 pF		–	46	MHz
		25 pF		–	23	
PulseminH2	Pin Group 2(2) High Level Pulse Width	10 pF		11	–	ns
		25 pF		21.8	–	
PulseminL2	Pin Group 2(2) Low Level Pulse Width	10 pF		11	–	ns
		25 pF		21.8	–	
FreqMax3	Pin Group3(3) Maximum Output Frequency	10 pF		–	70	MHz
		25 pF		–	35	
PulseminH3	Pin Group 3(3) High Level Pulse Width	10 pF		7.2	–	ns
		25 pF		14.2	–	
PulseminL3	Pin Group 3(3) Low Level Pulse Width	10 pF		7.2	–	ns
		25 pF		14.2	–	
FreqMax4	Pin Group 4(4) Maximum Output Frequency	10 pF		–	58	MHz
		25 pF		–	29	
PulseminH4	Pin Group 4(4) High Level Pulse Width	10 pF		8.6	–	ns
		25 pF		17.2	–	
PulseminL4	Pin Group 4(4) Low Level Pulse Width	10 pF		8.6	–	ns
		25 pF		17.2	–	
FreqMax5	Pin Group 5(5) Maximum Output Frequency	25 pF		–	25	MHz
$t_{sk(io)}$	Maximum I/O skew for all I/Os except PB0	30 pF		–	800	ps
	Maximum I/O skew for PB0			–	1200	

Notes: 1. Pin Group 1 = PA14, PA29

49. Revision History

In the tables that follow, the most recent version of the document appears first.

Table 49-1. SAM4S Datasheet Rev. 11100K Revision History

Doc. Date	Changes
09-Jun-15	**"Features":** updated "Memories" section.
	Added section "Safety Features Highlight".
	Section 8., "Memories" Added Section 8.1.3.4 "Error Code Correction (ECC)".
	Section 44., "Electrical Characteristics" Added Table 44-24, "SAM4SD32/SA16/SD16 Typical Active Power Consumption with VDDCORE@ 1.2V running from Flash Memory (AMP2) or SRAM".

Table 49-2. SAM4S Datasheet Rev. 11100J Revision History

Doc. Date	Changes
28-May-15	**"Features":** updated "System" and "Peripherals" sections
	Section 2., "Block Diagram" Updated Figures
	Section 4., "Package and Pinout" Modified AD13 and AD14 position in Table 4-2 "SAM4SD32/SD16/SA16/S16/S8/S4/S2 100-ball TFBGA Pinout" and Table 4-3 "SAM4SD32/SD16/SA16/S16/S8/S4/S2 100-ball VFBGA Pinout"
	Section 44., "Electrical Characteristics" Updated Table 44-41, "ADC Timing Characteristics" Table 44-74, "AC Flash Characteristics": added one "Endurance" value
	Section 48., "Errata" Section 48.1.5, "Low-power Mode" and Section 48.3.4, "Low-power Mode": modified Workaround 2 (code example)

Table 49-3. SAM4S Datasheet Rev. 11100I Revision History (Continued)

Doc. Date	Changes
03-Apr-15	**Section 37., "Timer Counter (TC)"**
	"Master clock" or "MCK" replaced with "peripheral clock"
	Replaced all occurrences of 'quadrature decoder logic' with 'quadrature decoder' or 'QDEC'
	Modified Section 37.1, "Description"
	Modified Section 37.2, "Embedded Characteristics"
	Modified Section 37.5.2, "Power Management" and Section 37.5.3, "Interrupt Sources"
	Section 37.6.14.2, "Input Pre-processing": deleted sentence "Filters can be disabled using the FILTER bit in the TC_BMR"
	Updated Figure 37-16, "Input Stage"
	Section 37.6.14, "Quadrature Decoder": removed subsection "Missing Pulse Detection and Auto-correction"
	Modified Section 37.6.14.4, "Position and Rotation Measurement" and Section 37.6.14.5, "Speed Measurement"
	Updated Section 37.6.17, "Register Write Protection"
	Section 37.7.2, "TC Channel Mode Register: Capture Mode": in 'Name' line, replaced "(WAVE = 0)" with "(CAPTURE_MODE)"
	Section 37.7.3, "TC Channel Mode Register: Waveform Mode": in 'Name' line, replaced "(WAVE = 1)" with "(WAVEFORM_MODE)"
	Updated Section 37.7.5, "TC Counter Value Register", Section 37.7.6 "TC Register A", Section 37.7.7 "TC Register B" , Section 37.7.8 "TC Register C", Section 37.7.9 "TC Status Register" and , Section 37.7.14, "TC Block Mode Register"Section 37.7.18, "TC QDEC Interrupt Status Register" and Section 37.7.20, "TC Write Protection Mode Register"
	Section 38., "High Speed Multimedia Card Interface (HSMCI)"
	Section 38.1, "Description": removed sentence "Only one slot can be selected at a time (slots are multiplexed)"
	Added Section 38.14.19, "HSMCI FIFOx Memory Aperture"
	Section 39., "Pulse Width Modulation Controller (PWM)"
	Updated Section 39.2, "Embedded Characteristics"
	Section 39.6.2.2, "Comparator": Corrected the PWM waveform period formulas.
	Updated Table 39-4 "Fault Inputs" and Figure 39-5. "Waveform Properties".
	Replaced "Master Clock (MCK)", "MCK" or "master clock" with "peripheral clock";
	Updated Section 39.5.2, "Power Management" and Section 39.5.3, "Interrupt Sources"
	Corrected register name PWM_CPRx to PWM_CPRDx
	Section 39.6.2.7, "Synchronous Channels": corrected paragraph beginning with'If a channel x is defined as a synchronous channel'.
	Updated Table 39-6 "Register Mapping"
	Updated Section 39.7.23, "PWM Fault Mode Register", Section 39.7.24, "PWM Fault Status Register", Section 39.7.25, "PWM Fault Clear Register", Section 39.7.27, "PWM Fault Protection Enable Register"
	Section 39.7.30, "PWM Write Protection Control Register" and Section 39.7.31, "PWM Write Protection Status Register": removed reset values.
	Changed CPRE bit description in Section 39.7.36, "PWM Channel Mode Register".
	Added Table 39-17 "Event Line Generation Waveform (Example)"
	Section 40., "USB Device Port (UDP)"
	Table 40-6, Register Mapping: modified footnote No. 1.
	Section 40.7.4, "UDP Interrupt Enable Register": modified WAKEUP bit description
	"Using Endpoints With Ping-pong Attributes": Replaced Bank 0 with Bank 1 in step 12