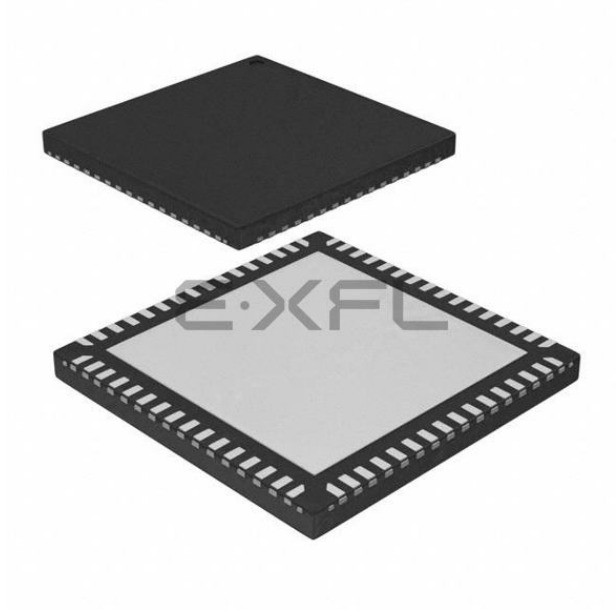

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	47
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 11x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4sd16bb-mnr

6. Input/Output Lines

The SAM4S has several kinds of input/output (I/O) lines such as general purpose I/Os (GPIO) and system I/Os. GPIOs can have alternate functionality due to multiplexing capabilities of the PIO controllers. The same PIO line can be used whether in I/O mode or by the multiplexed peripheral. System I/Os include pins such as test pins, oscillators, erase or analog inputs.

6.1 General Purpose I/O Lines

GPIO Lines are managed by PIO controllers. All I/Os have several input or output modes such as pull-up or pull-down, input Schmitt triggers, multi-drive (open-drain), glitch filters, debouncing or input change interrupt. Programming of these modes is performed independently for each I/O line through the PIO controller user interface. For more details, refer to Section 31. “Parallel Input/Output Controller (PIO)”.

Some GPIOs can have alternate function as analog input. When the GPIO is set in analog mode, all digital features of the I/O are disabled.

The input/output buffers of the PIO lines are supplied through VDDIO power supply rail.

The SAM4S embeds high-speed pads able to handle up to 70 MHz for HSMCI (MCK/2), 70 MHz for SPI clock lines and 46 MHz on other lines. See Section 44.12 “AC Characteristics” for more details. Typical pull-up and pull-down value is 100 kΩ for all I/Os.

Each I/O line also embeds an ODT (On-Die Termination), (see Figure 6-1). It consists of an internal series resistor termination scheme for impedance matching between the driver output (SAM4S) and the PCB trace impedance preventing signal reflection. The series resistor helps to reduce IOs switching current (di/dt) thereby reducing in turn, EMI. It also decreases overshoot and undershoot (ringing) due to inductance of interconnect between devices or between boards. In conclusion ODT helps diminish signal integrity issues.

Figure 6-1. On-Die Termination

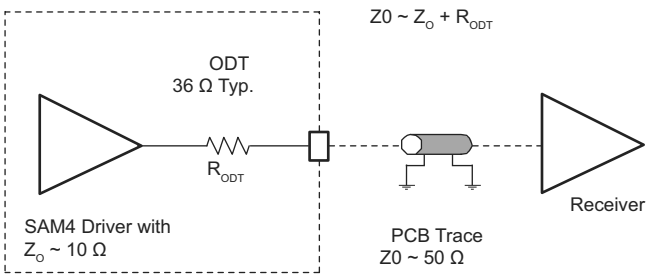
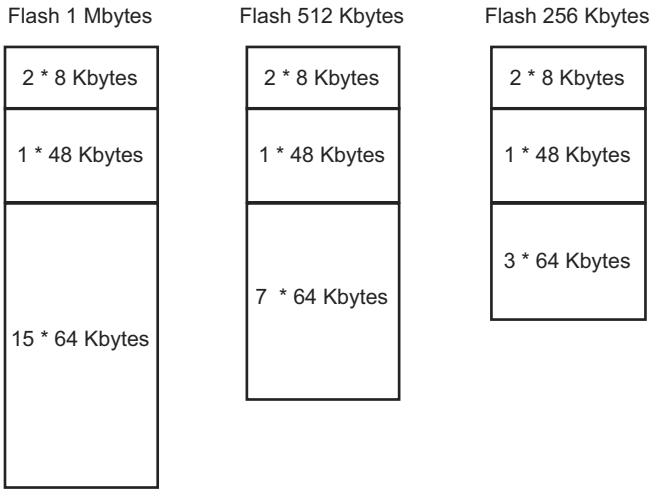


Figure 8-3. Flash Size



The following erase commands can be used depending on the sector size:

- 8 Kbyte small sector
  - Erase and write page (EWP)
  - Erase and write page and lock (EWPL)
  - Erase sector (ES) with FARG set to a page number in the sector to erase
  - Erase pages (EPA) with FARG [1:0] = 0 to erase four pages or FARG [1:0] = 1 to erase eight pages. FARG [1:0] = 2 and FARG [1:0] = 3 must not be used.
- 48 Kbyte and 64 Kbyte sectors
  - One block of 8 pages inside any sector, with the command Erase pages (EPA) with FARG[1:0] = 1
  - One block of 16 pages inside any sector, with the command Erase pages (EPA) and FARG[1:0] = 2
  - One block of 32 pages inside any sector, with the command Erase pages (EPA) and FARG[1:0] = 3
  - One sector with the command Erase sector (ES) and FARG set to a page number in the sector to erase
- Entire memory plane
  - The entire Flash, with the command Erase all (EA)

The Write commands of the Flash cannot be used under 330 kHz.

8.1.3.2 Enhanced Embedded Flash Controller

The Enhanced Embedded Flash Controller manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped on the APB.

The Enhanced Embedded Flash Controller ensures the interface of the Flash block.

It manages the programming, erasing, locking and unlocking sequences of the Flash using a full set of commands.

One of the commands returns the embedded Flash descriptor definition that informs the system about the Flash organization, thus making the software generic.

8.1.3.3 Flash Speed

The user must set the number of wait states depending on the frequency used.

For more details, refer to Section 44.12 “AC Characteristics”.

9. Real Time Event Management

The events generated by peripherals are designed to be directly routed to peripherals managing/using these events without processor intervention. Peripherals receiving events contain logic by which to select the one required.

9.1 Embedded Characteristics

- Timers, PWM, IO peripherals generate event triggers which are directly routed to event managers such as ADC or DACC, for example, to start measurement/conversion without processor intervention.
- UART, USART, SPI, TWI, SSC, PWM, HSMCI, ADC, DACC, PIO also generate event triggers directly connected to Peripheral DMA Controller (PDC) for data transfer without processor intervention.
- Parallel capture logic is directly embedded in PIO and generates trigger event to PDC to capture data without processor intervention.
- PWM security events (faults) are in combinational form and directly routed from event generators (ADC, ACC, PMC, TIMER) to PWM module.
- PMC security event (clock failure detection) can be programmed to switch the MCK on reliable main RC internal clock without processor intervention.

Examples

```
QADD16   R7, R4, R2  ; Adds halfwords of R4 with corresponding halfword of
                     ; R2, saturates to 16 bits and writes to
                     ; corresponding halfword of R7
QADD8    R3, R1, R6  ; Adds bytes of R1 to the corresponding bytes of R6,
                     ; saturates to 8 bits and writes to corresponding
                     ; byte of R3
QSUB16   R4, R2, R3  ; Subtracts halfwords of R3 from corresponding
                     ; halfword of R2, saturates to 16 bits, writes to
                     ; corresponding halfword of R4
QSUB8    R4, R2, R5  ; Subtracts bytes of R5 from the corresponding byte
                     ; in R2, saturates to 8 bits, writes to corresponding
                     ; byte of R4.
```

12.6.7.4 QASX and QSAX

Saturating Add and Subtract with Exchange and Saturating Subtract and Add with Exchange, signed.

Syntax

op{cond} {Rd}, Rm, Rn

where:

op — is one of:

QASX Add and Subtract with Exchange and Saturate.

QSAX Subtract and Add with Exchange and Saturate.

cond — is an optional condition code, see “Conditional Execution” .

Rd — is the destination register.

Rn, Rm — are registers holding the first and second operands.

Operation

The QASX instruction:

1. Adds the top halfword of the source operand with the bottom halfword of the second operand.
2. Subtracts the top halfword of the second operand from the bottom highword of the first operand.
3. Saturates the result of the subtraction and writes a 16-bit signed integer in the range $-2^{15} \le x \le 2^{15} - 1$, where *x* equals 16, to the bottom halfword of the destination register.
4. Saturates the results of the sum and writes a 16-bit signed integer in the range $-2^{15} \le x \le 2^{15} - 1$, where *x* equals 16, to the top halfword of the destination register.

The QSAX instruction:

1. Subtracts the bottom halfword of the second operand from the top highword of the first operand.
2. Adds the bottom halfword of the source operand with the top halfword of the second operand.
3. Saturates the results of the sum and writes a 16-bit signed integer in the range $-2^{15} \le x \le 2^{15} - 1$, where *x* equals 16, to the bottom halfword of the destination register.
4. Saturates the result of the subtraction and writes a 16-bit signed integer in the range $-2^{15} \le x \le 2^{15} - 1$, where *x* equals 16, to the top halfword of the destination register.

Restrictions

Do not use SP and do not use PC.

Condition Flags

These instructions do not affect the condition code flags.

Operation

The register access operation in MSR depends on the privilege level. Unprivileged software can only access the APSR. See “Application Program Status Register” . Privileged software can access all special registers.

In unprivileged software writes to unallocated or execution state bits in the PSR are ignored.

Note: When the user writes to BASEPRI_MAX, the instruction writes to BASEPRI only if either:
Rn is non-zero and the current BASEPRI value is 0
Rn is non-zero and less than the current BASEPRI value.

See “MRS” .

Restrictions

Rn must not be SP and must not be PC.

Condition Flags

This instruction updates the flags explicitly based on the value in *Rn*.

Examples

```
MSR  CONTROL, R1 ; Read R1 value and write it to the CONTROL register
```

12.6.11.8 NOP

No Operation.

Syntax

`NOP{cond}`

where:

cond is an optional condition code, see “Conditional Execution” .

Operation

NOP does nothing. NOP is not necessarily a time-consuming NOP. The processor might remove it from the pipeline before it reaches the execution stage.

Use NOP for padding, for example to place the following instruction on a 64-bit boundary.

Condition Flags

This instruction does not change the flags.

Examples

```
NOP  ; No operation
```

12.9.1 System Control Block (SCB) User Interface

Table 12-32. System Control Block (SCB) Register Mapping

Offset	Register	Name	Access	Reset
0xE000E008	Auxiliary Control Register	SCB_ACTLR	Read/Write	0x00000000
0xE000ED00	CPUID Base Register	SCB_CPUID	Read-only	0x410FC240
0xE000ED04	Interrupt Control and State Register	SCB_ICSR	Read/Write(1)	0x00000000
0xE000ED08	Vector Table Offset Register	SCB_VTOR	Read/Write	0x00000000
0xE000ED0C	Application Interrupt and Reset Control Register	SCB_AIRCR	Read/Write	0xFA050000
0xE000ED10	System Control Register	SCB_SCR	Read/Write	0x00000000
0xE000ED14	Configuration and Control Register	SCB_CCR	Read/Write	0x00000200
0xE000ED18	System Handler Priority Register 1	SCB_SHPR1	Read/Write	0x00000000
0xE000ED1C	System Handler Priority Register 2	SCB_SHPR2	Read/Write	0x00000000
0xE000ED20	System Handler Priority Register 3	SCB_SHPR3	Read/Write	0x00000000
0xE000ED24	System Handler Control and State Register	SCB_SHCSR	Read/Write	0x00000000
0xE000ED28	Configurable Fault Status Register	SCB_CFSR(2)	Read/Write	0x00000000
0xE000ED2C	HardFault Status Register	SCB_HFSR	Read/Write	0x00000000
0xE000ED34	MemManage Fault Address Register	SCB_MMFAR	Read/Write	Unknown
0xE000ED38	BusFault Address Register	SCB_BFAR	Read/Write	Unknown
0xE000ED3C	Auxiliary Fault Status Register	SCB_AFSR	Read/Write	0x00000000

Notes: 1. See the register description for more information.

2. This register contains the subregisters: “MMFSR: Memory Management Fault Status Subregister” (0xE000ED28 - 8 bits), “BFSR: Bus Fault Status Subregister” (0xE000ED29 - 8 bits), “UFSR: Usage Fault Status Subregister” (0xE000ED2A - 16 bits).

23.7.8 CRCCU DMA Interrupt Status Register

Name: CRCCU_DMA_ISR

Address: 0x40044020

Access: Read-only

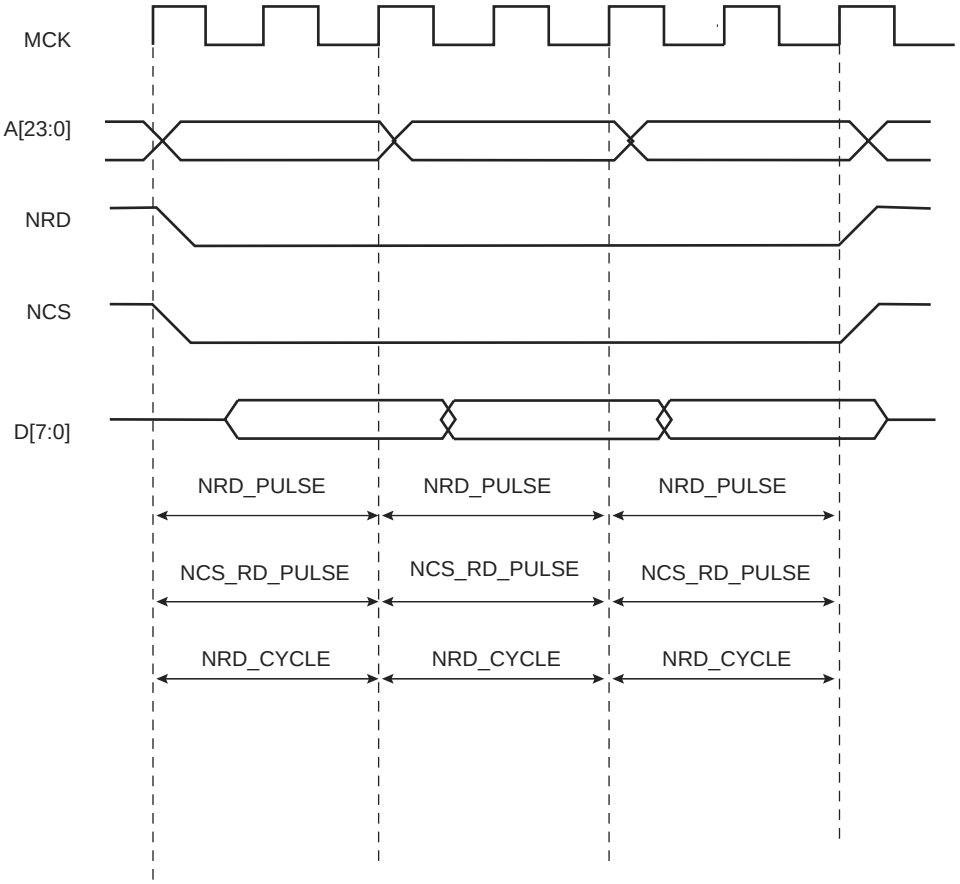
31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DMAISR

- **DMAISR: Interrupt Status**

0: DMA buffer transfer has not yet started or transfer still in progress

1: DMA buffer transfer has terminated. This flag is reset after read.

Figure 26-6. No Setup, No Hold on NRD and NCS Read Signals



26.9.1.5 Null Pulse

Programming null pulse is not permitted. Pulse must be at least set to 1. A null value leads to unpredictable behavior.

26.9.2 Read Mode

As NCS and NRD waveforms are defined independently of one other, the SMC needs to know when the read data is available on the data bus. The SMC does not compare NCS and NRD timings to know which signal rises first. The READ_MODE parameter in the SMC_MODE register of the corresponding chip select indicates which signal of NRD and NCS controls the read operation.

26.9.2.1 Read is Controlled by NRD (READ_MODE = 1):

Figure 26-7 shows the waveforms of a read operation of a typical asynchronous RAM. The read data is available t_{PACC} after the falling edge of NRD, and turns to ‘Z’ after the rising edge of NRD. In this case, the READ_MODE must be set to 1 (read is controlled by NRD), to indicate that data is available with the rising edge of NRD. The SMC samples the read data internally on the rising edge of Master Clock that generates the rising edge of NRD, whatever the programmed waveform of NCS may be.

26.16.7 SMC OCMS Key2 Register

Name: SMC_KEY2

Address: 0x400E0088

Access: Write Once

31	30	29	28	27	26	25	24
KEY2							

23	22	21	20	19	18	17	16
KEY2							

15	14	13	12	11	10	9	8
KEY2							

7	6	5	4	3	2	1	0
KEY2							

- **KEY2: Off Chip Memory Scrambling (OCMS) Key Part 2**

When off-chip memory scrambling is enabled, setting the SMC_OCMS and SMC_TIMINGS registers in accordance, the data scrambling depends on KEY2 and KEY1 values.

27.6.5 Receive Next Pointer Register

Name: PERIPH_RNPR

Access: Read/Write

31	30	29	28	27	26	25	24
RXNPTR							
23	22	21	20	19	18	17	16
RXNPTR							
15	14	13	12	11	10	9	8
RXNPTR							
7	6	5	4	3	2	1	0
RXNPTR							

- **RXNPTR: Receive Next Pointer**

RXNPTR contains the next receive buffer address.

When a half-duplex peripheral is connected to the PDC, RXNPTR = TXNPTR.

Table 29-3. Register Mapping (Continued)

Offset	Register	Name	Access	Reset
0x0110	Oscillator Calibration Register	PMC_OCR	Read/Write	0x0040_4040
0x114–0x120	Reserved	–	–	–
0134–0x144	Reserved	–	–	–

Note: If an offset is not listed in the table it must be considered as “reserved”.

29.17.24PMC Peripheral Clock Disable Register 1

Name: PMC_PCDR1

Address: 0x400E0504

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	–	PID34	PID33	PID32

This register can only be written if the WPEN bit is cleared in the PMC Write Protection Mode Register.

- **PIDx: Peripheral Clock x Disable**

0: No effect.

1: Disables the corresponding peripheral clock.

Note: The values for PIDx are defined in the section “Peripheral Identifiers” in the product datasheet.

31.6.28 PIO Input Filter Slow Clock Status Register

Name: PIO_IFSCSR

Address: 0x400E0E88 (PIOA), 0x400E1088 (PIOB), 0x400E1288 (PIOC)

Access: Read-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0–P31: Glitch or Debouncing Filter Selection Status**

0: The glitch filter is able to filter glitches with a duration < $t_{peripheral\ clock}/2$.

1: The debouncing filter is able to filter pulses with a duration < $t_{div\_slck}/2$.

31.6.37 PIO Additional Interrupt Modes Disable Register

Name: PIO_AIMDR

Address: 0x400E0EB4 (PIOA), 0x400E10B4 (PIOB), 0x400E12B4 (PIOC)

Access: Write-only

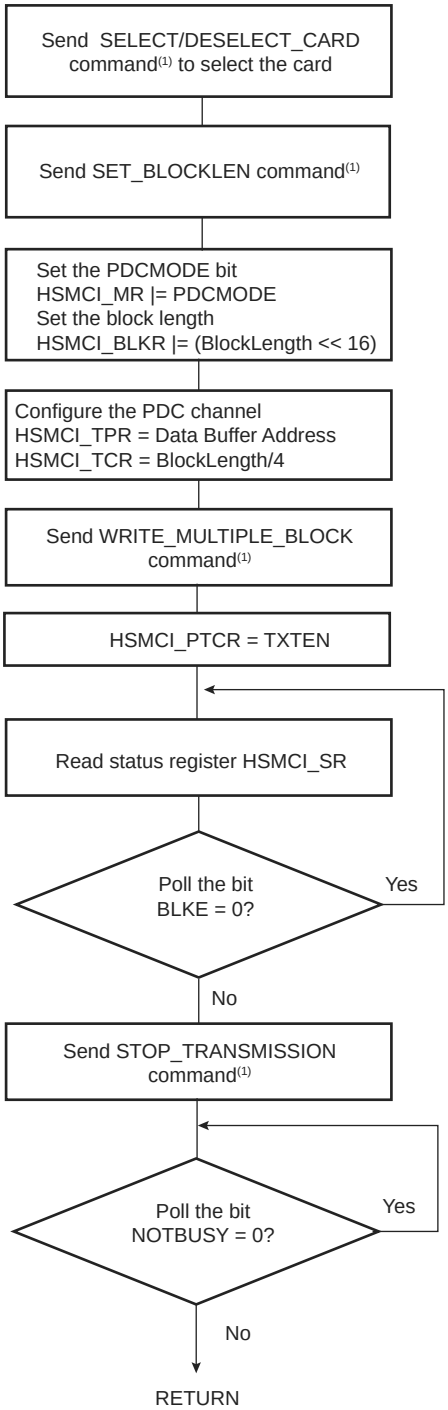
31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0–P31: Additional Interrupt Modes Disable**

0: No effect.

1: The interrupt mode is set to the default interrupt mode (both-edge detection).

Figure 38-10. Multiple Write Functional Flow Diagram



Note: 1. It is assumed that this command has been correctly sent (see Figure 38-7).

38.9 SD/SDIO Card Operation

The High Speed MultiMedia Card Interface allows processing of SD Memory (Secure Digital Memory Card) and SDIO (SD Input Output) Card commands.

SD/SDIO cards are based on the MultiMedia Card (MMC) format, but are physically slightly thicker and feature higher data transfer rates, a lock switch on the side to prevent accidental overwriting and security features. The

39.7.29 PWM Stepper Motor Mode Register

Name: PWM_SMMR

Address: 0x400200B0

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	DOWN1	DOWN0
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	GCEN1	GCEN0

- **GCENx: Gray Count ENable**

0: Disable gray count generation on PWML[2*x], PWMH[2*x], PWML[2*x +1], PWMH[2*x +1]

1: Enable gray count generation on PWML[2*x], PWMH[2*x], PWML[2*x +1], PWMH[2*x +1.

- **DOWNx: DOWN Count**

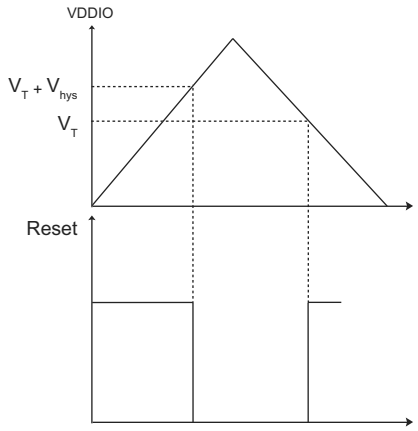
0: Up counter.

1: Down counter.

Table 44-7. Threshold Selection

Digital Code	Threshold Min (V)	Threshold Typ (V)	Threshold Max (V)
0000	1.56	1.6	1.64
0001	1.68	1.72	1.76
0010	1.79	1.84	1.89
0011	1.91	1.96	2.01
0100	2.03	2.08	2.13
0101	2.15	2.2	2.23
0110	2.26	2.32	2.38
0111	2.38	2.44	2.50
1000	2.50	2.56	2.62
1001	2.61	2.68	2.75
1010	2.73	2.8	2.87
1011	2.85	2.92	2.99
1100	2.96	3.04	3.12
1101	3.08	3.16	3.24
1110	3.20	3.28	3.36
1111	3.32	3.4	3.49

Figure 44-2. VDDIO Supply Monitor



44.8.5.2 ADC Electrical Performances

Single-ended Static Performances

Table 44-50. Single-ended Static Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INL	ADC Integral Non-linearity		-2	±1	2	LSB
DNL	ADC Differential Non-linearity		-1	±0.5	1	LSB

Single-ended Dynamic Performances

Table 44-51. Single-ended Dynamic Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNR	Signal to Noise Ratio	ADC Clock (f_{ADC}) = 20 MHz, f_S = 1 MHz, f_{IN} = 127 kHz, Frequency band = [1 kHz–500 kHz] Nyquist conditions fulfilled	56	64	72	dB
THD	Total Harmonic Distortion		66	74	84	dB
SINAD	Signal to Noise and Distortion		55	62	71	dB
ENOB	Effective Number of Bits		9	10.5	12	bits

Differential Static Performances

Table 44-52. Differential Static Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INL	Integral Non-linearity		-2	±1	2	LSB
DNL	Differential Non-linearity		-1	±0.5	1	LSB

Differential Dynamic Performances

Table 44-53. Differential Dynamic Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNR	Signal to Noise Ratio	ADC Clock (f_{ADC}) = 20 MHz, f_S = 1 MHz, f_{IN} = 127 kHz, Frequency band = [1 kHz–500 kHz] Nyquist conditions fulfilled	60	70	74	dB
THD	Total Harmonic Distortion		72	80	84	dB
SINAD	Signal to Noise and Distortion		60	68	73	dB
ENOB	Effective Number of Bits		9.5	11	12	bits

48.3.3 Brownout Detector

Issue: Unpredictable Behavior if BOD is Disabled, VDDCORE is Lost and VDDIO is Connected

In active mode or in wait mode, if the Brownout Detector is disabled (SUPC_MR.BODDIS = 1) and power is lost on VDDCORE while VDDIO is powered, the device might not be properly reset and may behave unpredictably.

Workaround: When the Brownout Detector is disabled in active or in wait mode, VDDCORE always needs to be powered.

48.3.4 Low-power Mode

Issue: Unpredictable Behavior When Entering Sleep Mode

When entering Sleep mode, if an interrupt occurs during WFI or WFE (PMC_FSMR.LPM = 0) instruction processing, the ARM core may read an incorrect data, thus leading to unpredictable behavior of the software. This issue is not present in Wait mode.

Workaround: The following conditions must be met:

1. The interrupt vector table must be located in Flash.
2. The Matrix slave interface for the Flash must be set to 'No default master'. This is done by setting the field DEFMSTR_TYPE to 0 in the register MATRIX_SCFG. The code example below can be used to program the NO_DEFAULT_MASTER state:

```
MATRIX_SCFG[2] = MATRIX_SCFG_SLOT_CYCLE(0xFF) | MATRIX_SCFG_DEFMSTR_TYPE(0x0);
```

   This must be done once in the software before entering Sleep mode.

48.3.5 PIO

Issue: PB4 Input Low-level Voltage Range

The undershoot is limited to -0.1V.

In normal operating conditions, the V_{IL} minimum value on PB4 is limited to 0V.

Workaround: The voltage on PB4 with respect to ground must be in the range -0.1V to + VDDIO + 0.4V instead of -0.3V to + VDDIO + 0.4V for all other input pins, as shown in Table 44.1 "Absolute Maximum Ratings".

The minimum V_{IL} on PB4 must be 0V instead of -0.3V for all other input pins, as shown in Table 44.3 "DC Characteristics".

Table 49-6. SAM4S Datasheet Rev. 11100F 29-Jan-14 Revision History (Continued)

Doc. Date	Changes
	Section 20. "Enhanced Embedded Flash Controller (EEFC)" Corrected partial programming boundary from 32-bit to 64-bit and reworked Section 20.4.3.2 "Write Commands" and all sub-sections with figures Figure 20-7 Full Page Programming to Figure 20-9 Programming Bytes in the Flash. In Section 20.4.3.3 "Erase Commands", modified paragraph on Erase pages (EPA) and Erase sector (ES) commands, as well as Table 20-4 "FARG Field for EPA Command". Added "small sector" text as limitations in Table 20-4 "FARG Field for EPA Command". Added notes when FARG exceeds limits in Section 20.4.3.4 "Lock Bit Protection". Re-worked Section 20.4.3.5 "GPNVM Bit" and added title in Section 20.4.3.6 "Calibration Bit". In Section 20.5.2 "EEFC Flash Command Register", changed the description of FARG field accordingly. Replaced NVIC by "interrupt controller" everywhere in the document.
	Section 23. "Cyclic Redundancy Check Calculation Unit (CRCCU)" Section 23.1 "Description": added sentence with information on CRCCU and data integrity check. Section 23.2 "Embedded Characteristics": removed bullet 'Single AHB Master Interface'. Inserted two new bullets on data integrity check and background task. Added note. Modified access type of Section 23.7.7 "CRCCU DMA Interrupt Mask Register". Section 23.6.2 "Transfer Control Register": updated IEN bit description Section 23.6.3 "Transfer Reference Register": replaced "compared with that register" with "compared with this field" in REFCRC field description Updated bit descriptions in Section 23.7.2 "CRCCU DMA Enable Register" to Section 23.7.6 "CRCCU DMA Interrupt Disable Register", in Section 23.7.8 "CRCCU DMA Interrupt Status Register", in Section 23.7.9 "CRCCU Control Register" and in Section 23.7.12 "CRCCU Interrupt Enable Register" to Section 23.7.15 "CRCCU Interrupt Status Register".
	Section 27. "Peripheral DMA Controller (PDC)" Replaced "on- and/or off-chip" with "target" in Section 27.1 "Description"and Section 27.4.2 "Memory Pointers". Added last paragraph to Section 27.4.1 "Configuration" specifying that the peripheral clock must be enabled for a PDC transfer.
	Section 28. "Clock Generator" Added Section 28.5.5 "Switching Main Clock between the Main RC Oscillator and Fast Crystal Oscillator".
	Section 29. "Power Management Controller (PMC)" Reworked Section 29.11 "Fast Startup" and added Section 29.12 "Start-up from Embedded Flash" Reworked Section 29.13 "Main Clock Failure Detector". Enhanced Section 29.14 "Programming Sequence" Enhanced Section 29.14 "Programming Sequence" Section 29.16 "Register Write Protection": Changed section title and re-worked content. In Section 29.17.21 "PMC Write Protection Mode Register" and Section 29.17.25 "PMC Peripheral Clock Status Register 1": Changed register names and modified bit and field descriptions.
	Section 30. "Chip Identifier (CHIPID)" Section 30.3.1 "Chip ID Register": Modified "ARCH: Architecture Identifier" bit description table to show only SAM4S.
	Section 31. "Parallel Input/Output Controller (PIO)" Section 31.5.14 "Register Write Protection": Changed section title and revised content. Section 31.7.46 "PIO Write Protection Mode Register": Modified register name and aligned bit descriptions. Replaced list of protectable registers with cross-reference to section "Register Write Protection". Section 31.7.47 "PIO Write Protection Status Register": Modified register name and aligned bit descriptions. Removed note.