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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4sd16cb-anr

4. Refer to “Fault Mode” in “Analog Comparator Controller (ACC)” .
5. Refer to “Fault Output” in Section 42. “Analog-to-Digital Converter (ADC)”.
6. Refer to “Fault Mode” in Section 37. “Timer Counter (TC)”
7. Refer to “Parallel Capture Mode” in “Parallel Input/Output Controller (PIO)” .
8. Refer to “Conversion Triggers” and the ADC Mode Register (ADC_MR) in Section 42., “Analog-to-Digital Converter (ADC)”.
9. Refer to PWM Comparison Value Register (PWM_CMPV) in Section 39. “Pulse Width Modulation Controller (PWM)”.
10. Refer to “PWM Comparison Units” and “PWM Event Lines” in Section 39. “Pulse Width Modulation Controller (PWM)”.
11. Refer to Section 39.6.2.2 “Comparator” in Section 39. “Pulse Width Modulation Controller (PWM)”.
12. Refer to Section 37. “Timer Counter (TC)”.
13. Refer to DACC Trigger Register (DACC_TRIGR) in Section 43. “Digital-to-Analog Converter Controller (DACC)”.

12.6.6 Multiply and Divide Instructions

The table below shows the multiply and divide instructions.

Table 12-21. Multiply and Divide Instructions

Mnemonic	Description
MLA	Multiply with Accumulate, 32-bit result
MLS	Multiply and Subtract, 32-bit result
MUL	Multiply, 32-bit result
SDIV	Signed Divide
SMLA[B,T]	Signed Multiply Accumulate (halfwords)
SMLAD, SMLADX	Signed Multiply Accumulate Dual
SMLAL	Signed Multiply with Accumulate (32 × 32 + 64), 64-bit result
SMLAL[B,T]	Signed Multiply Accumulate Long (halfwords)
SMLALD, SMLALDX	Signed Multiply Accumulate Long Dual
SMLAW[B|T]	Signed Multiply Accumulate (word by halfword)
SMLSD	Signed Multiply Subtract Dual
SMLSLD	Signed Multiply Subtract Long Dual
SMMLA	Signed Most Significant Word Multiply Accumulate
SMMLS, SMMLSR	Signed Most Significant Word Multiply Subtract
SMUAD, SMUADX	Signed Dual Multiply Add
SMUL[B,T]	Signed Multiply (word by halfword)
SMMUL, SMMULR	Signed Most Significant Word Multiply
SMULL	Signed Multiply (32x32), 64-bit result
SMULWB, SMULWT	Signed Multiply (word by halfword)
SMUSD, SMUSDX	Signed Dual Multiply Subtract
UDIV	Unsigned Divide
UMAAL	Unsigned Multiply Accumulate Accumulate Long (32 × 32 + 32 + 32), 64-bit result
UMLAL	Unsigned Multiply with Accumulate (32 × 32 + 64), 64-bit result
UMULL	Unsigned Multiply (32 × 32), 64-bit result

12.6.7.1 SSAT and USAT

Signed Saturate and Unsigned Saturate to any bit position, with optional shift before saturating.

Syntax

```
op{cond} Rd, #n, Rm {, shift #s}
```

where:

op	is one of:
	SSAT Saturates a signed value to a signed range.
	USAT Saturates a signed value to an unsigned range.
cond	is an optional condition code, see “Conditional Execution” .
Rd	is the destination register.
n	specifies the bit position to saturate to:
n ranges from 1	n ranges from 0 to 31 for USAT.
to 32 for SSAT	
Rm	is the register containing the value to saturate.
shift #s	is an optional shift applied to Rm before saturating. It must be one of the following:
ASR #s	where s is in the range 1 to 31.
LSL #s	where *s* is in the range 0 to 31.

Operation

These instructions saturate to a signed or unsigned *n*-bit value.

The SSAT instruction applies the specified shift, then saturates to the signed range $-2^{n-1} \le x \le 2^{n-1}-1$.

The USAT instruction applies the specified shift, then saturates to the unsigned range $0 \le x \le 2^{n}-1$.

Restrictions

Do not use SP and do not use PC.

Condition Flags

These instructions do not affect the condition code flags.

If saturation occurs, these instructions set the Q flag to 1.

Examples

```
        SSAT    R7, #16, R7, LSL #4  ; Logical shift left value in R7 by 4, then
                                     ; saturate it as a signed 16-bit value and
                                     ; write it back to R7
        USATNE  R0, #7, R5           ; Conditionally saturate value in R5 as an
                                     ; unsigned 7 bit value and write it to R0.
```

12.9.1.1 Auxiliary Control Register

Name: SCB_ACTLR

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	DISOOFP	DISFPCA

7	6	5	4	3	2	1	0
–	–	–	–	–	DISFOLD	DISDEFWBUF	DISMCYCINT

The SCB_ACTLR provides disable bits for the following processor functions:

- IT folding
- Write buffer use for accesses to the default memory map
- Interruption of multi-cycle instructions.

By default, this register is set to provide optimum performance from the Cortex-M4 processor, and does not normally require modification.

- **DISOOFP: Disable Out Of Order Floating Point**

Disables floating point instructions that complete out of order with respect to integer instructions.

- **DISFPCA: Disable FPCA**

Disables an automatic update of CONTROL.FPCA.

- **DISFOLD: Disable Folding**

When set to 1, disables the IT folding.

Note: In some situations, the processor can start executing the first instruction in an IT block while it is still executing the IT instruction. This behavior is called IT folding, and it improves the performance. However, IT folding can cause jitter in looping. If a task must avoid jitter, set the DISFOLD bit to 1 before executing the task, to disable the IT folding.

- **DISDEFWBUF: Disable Default Write Buffer**

When set to 1, it disables the write buffer use during default memory map accesses. This causes BusFault to be precise but decreases the performance, as any store to memory must complete before the processor can execute the next instruction.

This bit only affects write buffers implemented in the Cortex-M4 processor.

- **DISMCYCINT: Disable Multiple Cycle Interruption**

When set to 1, it disables the interruption of load multiple and store multiple instructions. This increases the interrupt latency of the processor, as any LDM or STM must complete before the processor can stack the current state and enter the interrupt handler.

12.10.1.2 SysTick Reload Value Registers

Name: SYST_RVR

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
RELOAD							

15	14	13	12	11	10	9	8
RELOAD							

7	6	5	4	3	2	1	0
RELOAD							

The SYST_RVR specifies the start value to load into the SYST_CVR.

- **RELOAD: SYST_CVR Load Value**

Value to load into the SYST_CVR when the counter is enabled and when it reaches 0.

The RELOAD value can be any value in the range 0x00000001–0x00FFFFFF. A start value of 0 is possible, but has no effect because the SysTick exception request and COUNTFLAG are activated when counting from 1 to 0.

The RELOAD value is calculated according to its use: For example, to generate a multi-shot timer with a period of N processor clock cycles, use a RELOAD value of N-1. If the SysTick interrupt is required every 100 clock pulses, set RELOAD to 99.

12.11 Memory Protection Unit (MPU)

The MPU divides the memory map into a number of regions, and defines the location, size, access permissions, and memory attributes of each region. It supports:

- Independent attribute settings for each region
- Overlapping regions
- Export of memory attributes to the system.

The memory attributes affect the behavior of memory accesses to the region. The Cortex-M4 MPU defines:

- Eight separate memory regions, 0–7
- A background region.

When memory regions overlap, a memory access is affected by the attributes of the region with the highest number. For example, the attributes for region 7 take precedence over the attributes of any region that overlaps region 7.

The background region has the same memory access attributes as the default memory map, but is accessible from privileged software only.

The Cortex-M4 MPU memory map is unified. This means that instruction accesses and data accesses have the same region settings.

If a program accesses a memory location that is prohibited by the MPU, the processor generates a memory management fault. This causes a fault exception, and might cause the termination of the process in an OS environment.

In an OS environment, the kernel can update the MPU region setting dynamically based on the process to be executed. Typically, an embedded OS uses the MPU for memory protection.

The configuration of MPU regions is based on memory types (see "Memory Regions, Types and Attributes").

Table 12-35 shows the possible MPU region attributes. These include Share ability and cache behavior attributes that are not relevant to most microcontroller implementations. See "MPU Configuration for a Microcontroller" for guidelines for programming such an implementation.

Table 12-35. Memory Attributes Summary

Memory Type	Shareability	Other Attributes	Description
Strongly-ordered	–	–	All accesses to Strongly-ordered memory occur in program order. All Strongly-ordered regions are assumed to be shared.
Device	Shared	–	Memory-mapped peripherals that several processors share.
	Non-shared	–	Memory-mapped peripherals that only a single processor uses.
Normal	Shared	Non-cacheable Write-through Cacheable Write-back Cacheable	Normal memory that is shared between several processors.
	Non-shared	Non-cacheable Write-through Cacheable Write-back Cacheable	Normal memory that only a single processor uses.

12.11.1 MPU Access Permission Attributes

This section describes the MPU access permission attributes. The access permission bits (TEX, C, B, S, AP, and XN) of the MPU_RASR control the access to the corresponding memory region. If an access is made to an area of memory without the required permissions, then the MPU generates a permission fault.

The supply monitor can also be enabled during one slow clock period on every one of either 32, 256 or 2048 slow clock periods, depending on the user selection. This is configured in the SMSMPL field in SUPC_SMMR.

Enabling the supply monitor for such reduced times divides the typical supply monitor power consumption by factors of 2, 16 and 128, respectively, if continuous monitoring of the VDDIO power supply is not required.

A supply monitor detection generates either a reset of the core power supply or a wake-up of the core power supply. Generating a core reset when a supply monitor detection occurs is enabled by setting the SMRSTEN bit in SUPC_SMMR.

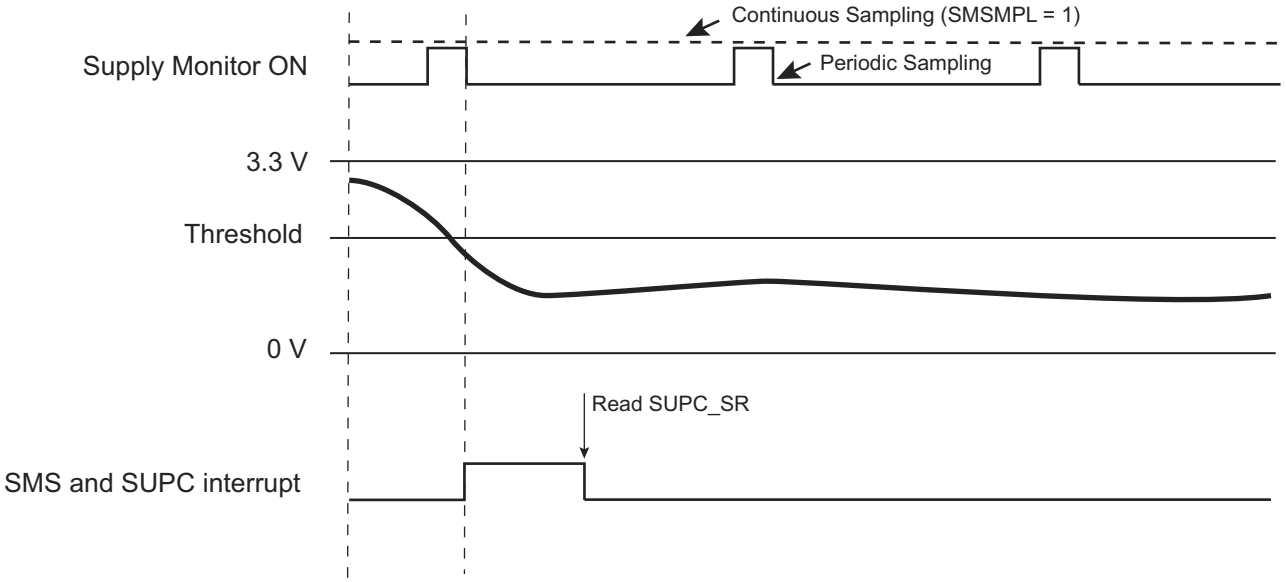
Waking up the core power supply when a supply monitor detection occurs can be enabled by setting the SMEN bit in the Wake-up Mode register (SUPC_WUMR).

The SUPC provides two status bits in the SUPC_SR for the supply monitor that determine whether the last wake-up was due to the supply monitor:

- The SMOS bit provides real-time information, updated at each measurement cycle or updated at each slow clock cycle, if the measurement is continuous.
- The SMS bit provides saved information and shows a supply monitor detection has occurred since the last read of SUPC_SR.

The SMS flag generates an interrupt if the SMIEN bit is set in SUPC_SMMR.

Figure 18-2. Supply Monitor Status Bit and Associated Interrupt



18.4.5 Backup Power Supply Reset

18.4.5.1 Raising the Backup Power Supply

When the backup voltage VDDIO rises, the RC oscillator is powered up and the zero-power power-on reset cell maintains its output low as long as VDDIO has not reached its target voltage. During this period, the SUPC is reset. When the VDDIO voltage becomes valid and the zero-power power-on reset signal is released, a counter is started for five slow clock cycles. This is the time required for the 32 kHz RC oscillator to stabilize.

After this time, the voltage regulator is enabled. The core power supply rises and the brownout detector provides the bodcore_in signal as soon as the core voltage VDDCORE is valid. This results in releasing the vddcore_nreset signal to the Reset Controller after the bodcore_in signal has been confirmed as being valid for at least one slow clock cycle.

18.5.7 Supply Controller Wake-up Inputs Register

Name: SUPC_WUIR

Address: 0x400E1420

Access: Read/Write

31	30	29	28	27	26	25	24
WKUPT15	WKUPT14	WKUPT13	WKUPT12	WKUPT11	WKUPT10	WKUPT9	WKUPT8
23	22	21	20	19	18	17	16
WKUPT7	WKUPT6	WKUPT5	WKUPT4	WKUPT3	WKUPT2	WKUPT1	WKUPT0
15	14	13	12	11	10	9	8
WKUPEN15	WKUPEN14	WKUPEN13	WKUPEN12	WKUPEN11	WKUPEN10	WKUPEN9	WKUPEN8
7	6	5	4	3	2	1	0
WKUPEN7	WKUPEN6	WKUPEN5	WKUPEN4	WKUPEN3	WKUPEN2	WKUPEN1	WKUPEN0

This register is located in the VDDIO domain.

This register can only be written if the WPEN bit is cleared in the System Controller Write Protection Mode Register (SYSC_MR).

- **WKUPEN0 - WKUPENx: Wake-up Input Enable 0 to x**

0 (DISABLE): The corresponding wake-up input has no wake-up effect.

1 (ENABLE): The corresponding wake-up input is enabled for a wake-up of the core power supply.

- **WKUPT0 - WKUPTx: Wake-up Input Type 0 to x**

0 (LOW): A falling edge followed by a low level for a period defined by WKUPDBC on the corresponding wake-up input forces the wake-up of the core power supply.

1 (HIGH): A rising edge followed by a high level for a period defined by WKUPDBC on the corresponding wake-up input forces the wake-up of the core power supply.

23.7.2 CRCCU DMA Enable Register

Name: CRCCU_DMA_EN

Address: 0x40044008

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	DMAEN

- **DMAEN: DMA Enable**

0: No effect

1: Enable CRCCU DMA channel

For more details about VID/PID for End Product/Systems, please refer to the Vendor ID form available from the USB Implementers Forum on www.usb.org.

Atmel provides an INF example to see the device as a new serial port and also provides another custom driver used by the SAM-BA application: atm6124.sys. Refer to the application note “USB Basic Application”, Atmel literature number 6123, for more details.

24.5.3.1 Enumeration Process

The USB protocol is a master/slave protocol. This is the host that starts the enumeration sending requests to the device through the control endpoint. The device handles standard requests as defined in the USB Specification.

Table 24-3. Handled Standard Requests

Request	Definition
GET_DESCRIPTOR	Returns the current device configuration value.
SET_ADDRESS	Sets the device address for all future device access.
SET_CONFIGURATION	Sets the device configuration.
GET_CONFIGURATION	Returns the current device configuration value.
GET_STATUS	Returns status for the specified recipient.
SET_FEATURE	Set or Enable a specific feature.
CLEAR_FEATURE	Clear or Disable a specific feature.

The device also handles some class requests defined in the CDC class.

Table 24-4. Handled Class Requests

Request	Definition
SET_LINE_CODING	Configures DTE rate, stop bits, parity and number of character bits.
GET_LINE_CODING	Requests current DTE rate, stop bits, parity and number of character bits.
SET_CONTROL_LINE_STATE	RS-232 signal used to tell the DCE device the DTE device is now present.

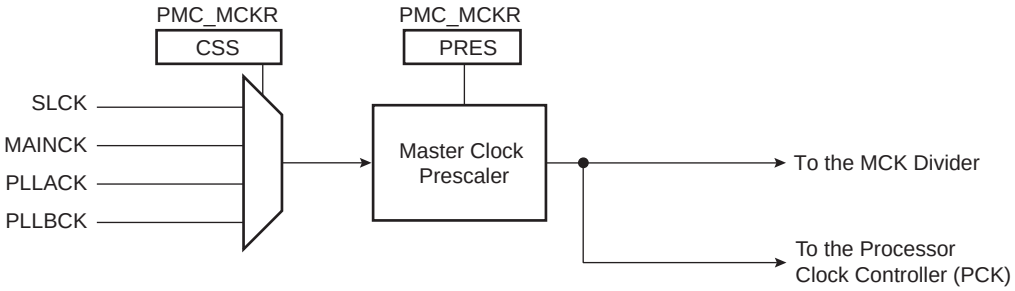
Unhandled requests are STALLed.

24.5.3.2 Communication Endpoints

There are two communication endpoints and endpoint 0 is used for the enumeration process. Endpoint 1 is a 64-byte Bulk OUT endpoint and endpoint 2 is a 64-byte Bulk IN endpoint. SAM-BA Boot commands are sent by the host through endpoint 1. If required, the message is split by the host into several data payloads by the host driver.

If the command requires a response, the host can send IN transactions to pick up the response.

Figure 29-2. Master Clock Controller



29.5 Processor Clock Controller

The PMC features a Processor Clock Controller (HCLK) that implements the processor Sleep mode. These processor clock can be disabled by executing the WFI (WaitForInterrupt) or the WFE (WaitForEvent) processor instruction while the LPM bit is at 0 in the PMC Fast Startup Mode Register (PMC_FSMR).

The Processor Clock Controller HCLK is enabled after a reset and is automatically re-enabled by any enabled interrupt. The processor Sleep mode is entered by disabling the processor clock, which is automatically re-enabled by any enabled fast or normal interrupt, or by the reset of the product.

When processor Sleep mode is entered, the current instruction is finished before the clock is stopped, but this does not prevent data transfers from other masters of the system bus.

29.6 SysTick Clock

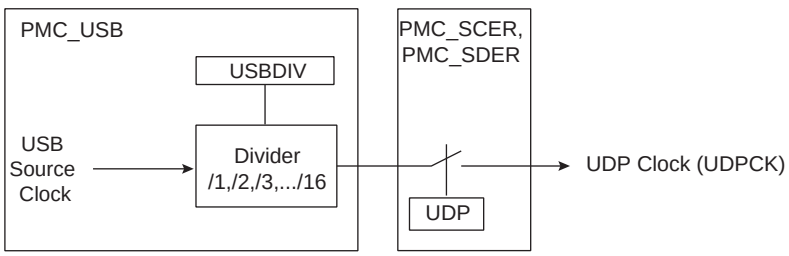
The SysTick calibration value is fixed to 12500 which allows the generation of a time base of 1 ms with SysTick clock to the maximum frequency on MCK divided by 8.

29.7 USB Clock Controller

The user can select the PLLA or the PLLB output as the USB source clock by writing the USBS bit in PMC_USB. If using the USB, the user must program the PLL to generate an appropriate frequency depending on the USBDIV bit in the USB Clock Register (PMC_USB).

When the PLL output is stable, i.e., the LOCK bit is set, the USB device FS clock can be enabled by setting the UDP bit in the System Clock Enable Register (PMC_SCER). To save power on this peripheral when it is not used, the user can set the UDP bit in the System Clock Disable Register (PMC_SCDR). The UDP bit in the System Clock Status Register (PMC_SCSR) gives the activity of this clock. The USB device port requires both the 48 MHz signal and the peripheral clock. The USB peripheral clock may be controlled by means of the Master Clock Controller.

Figure 29-3. USB Clock Controller



Transmit Character Repetition

When the USART is transmitting a character and gets a NACK, it can automatically repeat the character before moving on to the next one. Repetition is enabled by writing the MAX_ITERATION field in the US_MR at a value higher than 0. Each character can be transmitted up to eight times; the first transmission plus seven repetitions.

If MAX_ITERATION does not equal zero, the USART repeats the character as many times as the value loaded in MAX_ITERATION.

When the USART repetition number reaches MAX_ITERATION and the last repeated character is not acknowledged, the ITER bit is set in US_CSR. If the repetition of the character is acknowledged by the receiver, the repetitions are stopped and the iteration counter is cleared.

The ITER bit in US_CSR can be cleared by writing a 1 to the RSTIT bit in the US_CR.

Disable Successive Receive NACK

The receiver can limit the number of successive NACKs sent back to the remote transmitter. This is programmed by setting the bit DSNACK in the US_MR. The maximum number of NACKs transmitted is programmed in the MAX_ITERATION field. As soon as MAX_ITERATION is reached, no error signal is driven on the I/O line and the ITER bit in the US_CSR is set.

36.6.4.3 Protocol T = 1

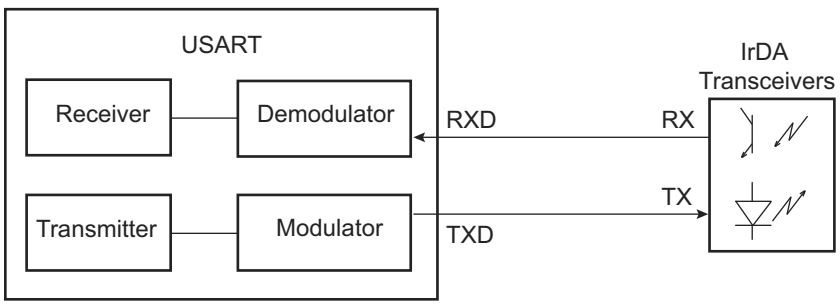
When operating in ISO7816 protocol T = 1, the transmission is similar to an asynchronous format with only one stop bit. The parity is generated when transmitting and checked when receiving. Parity error detection sets the PARE bit in the US_CSR.

36.6.5 IrDA Mode

The USART features an IrDA mode supplying half-duplex point-to-point wireless communication. It embeds the modulator and demodulator which allows a glueless connection to the infrared transceivers, as shown in Figure 36-32. The modulator and demodulator are compliant with the IrDA specification version 1.1 and support data transfer speeds ranging from 2.4 kbit/s to 115.2 kbit/s.

The IrDA mode is enabled by setting the USART_MODE field in US_MR to the value 0x8. The IrDA Filter register (US_IF) is used to configure the demodulator filter. The USART transmitter and receiver operate in a normal Asynchronous mode and all parameters are accessible. Note that the modulator and the demodulator are activated.

Figure 36-32. Connection to IrDA Transceivers



The receiver and the transmitter must be enabled or disabled depending on the direction of the transmission to be managed.

To receive IrDA signals, the following needs to be done:

- Disable TX and Enable RX
- Configure the TXD pin as PIO and set it as an output to 0 (to avoid LED emission). Disable the internal pull-up (better for power consumption).

37.7.2 TC Channel Mode Register: Capture Mode

Name: TC_CMRx [x=0..2] (CAPTURE_MODE)

Address: 0x40010004 (0)[0], 0x40010044 (0)[1], 0x40010084 (0)[2], 0x40014004 (1)[0], 0x40014044 (1)[1], 0x40014084 (1)[2]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	LDRB		LDRA	
15	14	13	12	11	10	9	8
WAVE	CPCTRG	–	–	–	ABETRG	ETRGEDG	
7	6	5	4	3	2	1	0
LDBDIS	LDBSTOP	BURST		CLKI	TCCLKS		

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

- **TCCLKS: Clock Selection**

Value	Name	Description
0	TIMER_CLOCK1	Clock selected: internal MCK/2 clock signal (from PMC)
1	TIMER_CLOCK2	Clock selected: internal MCK/8 clock signal (from PMC)
2	TIMER_CLOCK3	Clock selected: internal MCK/32 clock signal (from PMC)
3	TIMER_CLOCK4	Clock selected: internal MCK/128 clock signal (from PMC)
4	TIMER_CLOCK5	Clock selected: internal SLCK clock signal (from PMC)
5	XC0	Clock selected: XC0
6	XC1	Clock selected: XC1
7	XC2	Clock selected: XC2

- **CLKI: Clock Invert**

0: Counter is incremented on rising edge of the clock.

1: Counter is incremented on falling edge of the clock.

- **BURST: Burst Signal Selection**

Value	Name	Description
0	NONE	The clock is not gated by an external signal.
1	XC0	XC0 is ANDed with the selected clock.
2	XC1	XC1 is ANDed with the selected clock.
3	XC2	XC2 is ANDed with the selected clock.

- **LDBSTOP: Counter Clock Stopped with RB Loading**

0: Counter clock is not stopped when RB loading occurs.

1: Counter clock is stopped when RB loading occurs.

37.7.17 TC QDEC Interrupt Mask Register

Name: TC_QIMR

Address: 0x400100D0 (0), 0x400140D0 (1)

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	QERR	DIRCHG	IDX

- **IDX: Index**

0: The interrupt on IDX input is disabled.

1: The interrupt on IDX input is enabled.

- **DIRCHG: Direction Change**

0: The interrupt on rotation direction change is disabled.

1: The interrupt on rotation direction change is enabled.

- **QERR: Quadrature Error**

0: The interrupt on quadrature error is disabled.

1: The interrupt on quadrature error is enabled.

All of the PWM outputs may or may not be enabled. If an application requires only four channels, then only four PIO lines will be assigned to PWM outputs.

Table 39-2. I/O Lines

Instance	Signal	I/O Line	Peripheral
PWM	PWMFI0	PA9	C
PWM	PWMFI1	PA10	C
PWM	PWMFI2	PA18	D
PWM	PWMH0	PA0	A
PWM	PWMH0	PA11	B
PWM	PWMH0	PA23	B
PWM	PWMH0	PB0	A
PWM	PWMH0	PC18	B
PWM	PWMH1	PA1	A
PWM	PWMH1	PA12	B
PWM	PWMH1	PA24	B
PWM	PWMH1	PB1	A
PWM	PWMH1	PC19	B
PWM	PWMH2	PA2	A
PWM	PWMH2	PA13	B
PWM	PWMH2	PA25	B
PWM	PWMH2	PB4	B
PWM	PWMH2	PC20	B
PWM	PWMH3	PA7	B
PWM	PWMH3	PA14	B
PWM	PWMH3	PA17	C
PWM	PWMH3	PB14	B
PWM	PWMH3	PC21	B
PWM	PWML0	PA19	B
PWM	PWML0	PB5	B
PWM	PWML0	PC0	B
PWM	PWML0	PC13	B
PWM	PWML1	PA20	B
PWM	PWML1	PB12	A
PWM	PWML1	PC1	B
PWM	PWML1	PC15	B
PWM	PWML2	PA16	C
PWM	PWML2	PA30	A
PWM	PWML2	PB13	A
PWM	PWML2	PC2	B

39.7.25 PWM Fault Clear Register

Name: PWM_FCR

Address: 0x40020064

Access: Write-only

31	30	29	28	27	26	25	24
–							

23	22	21	20	19	18	17	16
–							

15	14	13	12	11	10	9	8
–							

7	6	5	4	3	2	1	0
FCLR							

- **FCLR: Fault Clear**

For each bit y of FCLR, where y is the fault input number:

0: No effect.

1: If bit y of FMOD field is set to ‘1’ and if the fault input y is not at the level defined by the bit y of FPOL field, the fault y is cleared and becomes inactive (FMOD and FPOL fields belong to PWM Fault Mode Register), else writing this bit to ‘1’ has no effect.

39.7.38 PWM Channel Duty Cycle Update Register

Name: PWM_CDTYUPDx [x=0..3]

Address: 0x40020208 [0], 0x40020228 [1], 0x40020248 [2], 0x40020268 [3]

Access: Write-only.

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
CDTYUPD							

15	14	13	12	11	10	9	8
CDTYUPD							

7	6	5	4	3	2	1	0
CDTYUPD							

This register acts as a double buffer for the CDTY value. This prevents an unexpected waveform when modifying the waveform duty-cycle.

Only the first 16 bits (channel counter size) are significant.

- **CDTYUPD: Channel Duty-Cycle Update**

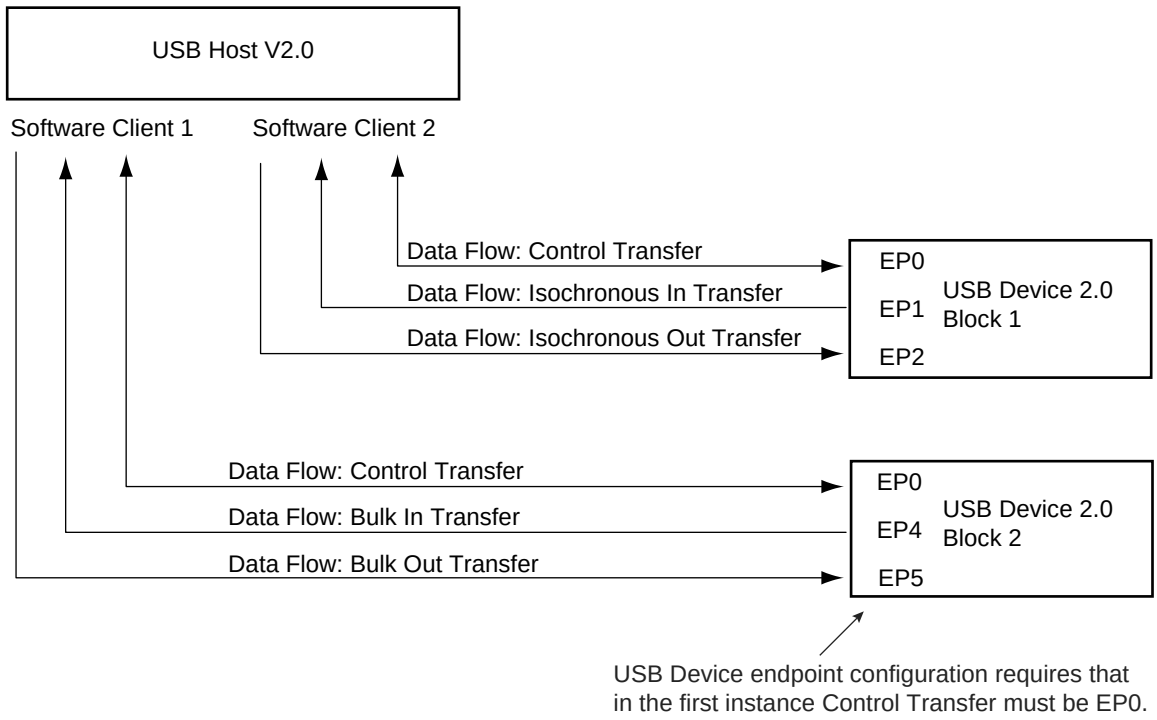
Defines the waveform duty-cycle. This value must be defined between 0 and CPRD (PWM_CPRDx).

40.6 Functional Description

40.6.1 USB 2.0 Full-speed Introduction

The USB 2.0 full-speed provides communication services between host and attached USB devices. Each device is offered with a collection of communication flows (pipes) associated with each endpoint. Software on the host communicates with a USB device through a set of communication flows.

Figure 40-3. Example of USB 2.0 Full-speed Communication Control



The Control Transfer endpoint EP0 is always used when a USB device is first configured (USB 2.0 specifications).

40.6.1.1 USB 2.0 Full-speed Transfer Types

A communication flow is carried over one of four transfer types defined by the USB device.

Table 40-4. USB Communication Flow

Transfer	Direction	Bandwidth	Supported Endpoint Size	Error Detection	Retrying
Control	Bidirectional	Not guaranteed	8, 16, 32, 64	Yes	Automatic
Isochronous	Unidirectional	Guaranteed	512	Yes	No
Interrupt	Unidirectional	Not guaranteed	≤ 64	Yes	Yes
Bulk	Unidirectional	Not guaranteed	8, 16, 32, 64	Yes	Yes

40.6.1.2 USB Bus Transactions

Each transfer results in one or more transactions over the USB bus. There are three kinds of transactions flowing across the bus in packets:

- Setup Transaction
- Data IN Transaction
- Data OUT Transaction

44.8 12-bit ADC Characteristics

Electrical data are in accordance with the following standard conditions unless otherwise specified:

- Operating temperature range from -40°C to + 105°C
- Min and max data are defined as three times the standard deviation of the manufacturing process

44.8.1 ADC Power Supply

Table 44-38. Analog Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDIN}	Supply Voltage Range	Full operational	2.4	–	3.6	V
		(1)	2	–	2.4	
I_{VDDIN}	Analog Current Consumption	ADC Sleep Mode(2)	–	2	4	µA
		ADC Fast Wake-up Mode(3)		2.4	3.5	mA
		ADC Normal Mode		4.3	6	mA
$I_{VDDcore}$	Digital Current Consumption	ADC Sleep Mode (all off)(2)	–	–	0.1	µA
		ADC Normal Mode		0.2	0.4	mA

Notes: 1. See Section "Low Voltage Supply".
2. In Sleep mode the ADC core, sample and hold, and internal reference operational amplifier are off.
3. In Fast Wake-up mode, only the ADC core is off.

44.8.1.1 ADC Bias Current

All current consumption is performed when the field IBCTL in the ADC Analog Control Register (ADC_ACR) is set to 01.

IBCTL controls the ADC biasing current, with the nominal setting IBCTL = 01.

IBCTL = 00 is the required value for a sampling frequency below 500 kHz, and IBCTL = 01 for a sampling frequency between 500 kHz and 1 MHz.

Table 44-39. ADC Bias Current Adjustment

IBCTL = 00	IBCTL = 01	IBCTL = 10	IBCTL = 11
Typ-22%	Typ	Reserved	Reserved

Table 45-8. VFBGA Package Dimensions (Continued)

		Symbol	Common Dimensions (mm)
Ball Diameter:			0.300
Stand Off:		A1	0.160 ~ 0.260
Ball Width:		b	0.270 ~ 0.370
Package Edge Tolerance:		aaa	0.100
Mold Flatness:		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package):		eee	0.150
Ball Offset (Ball):		fff	0.080
Ball Count:		n	100
Edge Ball Center to Center:	X	E1	5.850
	Y	D1	5.850
Corner Ball Center to Package Edge:	X	I	0.575
	Y	J	0.575

Table 45-9. VFBGA Package Reference - Soldering Information (Substrate Level)

Ball Land	Diameter 0.27 mm
Soldering Mask Opening	275 µm

Table 45-10. Device and 100-ball VFBGA Package Maximum Weight

SAM4S	75	mg

Table 45-11. 100-ball VFBGA Package Characteristics

Moisture Sensitivity Level	3

Table 45-12. 100-ball VFBGA Package Reference

JEDEC Drawing Reference	MO-275-BBE-1
JESD97 Classification	e8