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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4sd32ca-cur

Table 12-13. Cortex-M4 Instructions (Continued)

Mnemonic	Operands	Description	Flags
SMULBB, SMULBT SMULTB, SMULTT	{Rd,} Rn, Rm	Signed Multiply (halfwords)	–
SMULL	RdLo, RdHi, Rn, Rm	Signed Multiply (32 × 32), 64-bit result	–
SMULWB, SMULWT	{Rd,} Rn, Rm	Signed Multiply word by halfword	–
SMUSD, SMUSDX	{Rd,} Rn, Rm	Signed dual Multiply Subtract	–
SSAT	Rd, #n, Rm {,shift #s}	Signed Saturate	Q
SSAT16	Rd, #n, Rm	Signed Saturate 16	Q
SSAX	{Rd,} Rn, Rm	Signed Subtract and Add with Exchange	GE
SSUB16	{Rd,} Rn, Rm	Signed Subtract 16	–
SSUB8	{Rd,} Rn, Rm	Signed Subtract 8	–
STM	Rn{!}, reglist	Store Multiple registers, increment after	–
STMDB, STMEA	Rn{!}, reglist	Store Multiple registers, decrement before	–
STMFD, STMIA	Rn{!}, reglist	Store Multiple registers, increment after	–
STR	Rt, [Rn, #offset]	Store Register word	–
STRB, STRBT	Rt, [Rn, #offset]	Store Register byte	–
STRD	Rt, Rt2, [Rn, #offset]	Store Register two words	–
STREX	Rd, Rt, [Rn, #offset]	Store Register Exclusive	–
STREXB	Rd, Rt, [Rn]	Store Register Exclusive byte	–
STREXH	Rd, Rt, [Rn]	Store Register Exclusive halfword	–
STRH, STRHT	Rt, [Rn, #offset]	Store Register halfword	–
STRT	Rt, [Rn, #offset]	Store Register word	–
SUB, SUBS	{Rd,} Rn, Op2	Subtract	N,Z,C,V
SUB, SUBW	{Rd,} Rn, #imm12	Subtract	N,Z,C,V
SVC	#imm	Supervisor Call	–
SXTAB	{Rd,} Rn, Rm,{,ROR #}	Extend 8 bits to 32 and add	–
SXTAB16	{Rd,} Rn, Rm,{,ROR #}	Dual extend 8 bits to 16 and add	–
SXTAH	{Rd,} Rn, Rm,{,ROR #}	Extend 16 bits to 32 and add	–
SXTB16	{Rd,} Rm {,ROR #n}	Signed Extend Byte 16	–
SXTB	{Rd,} Rm {,ROR #n}	Sign extend a byte	–
SXTH	{Rd,} Rm {,ROR #n}	Sign extend a halfword	–
TBB	[Rn, Rm]	Table Branch Byte	–
TBH	[Rn, Rm, LSL #1]	Table Branch Halfword	–
TEQ	Rn, Op2	Test Equivalence	N,Z,C
TST	Rn, Op2	Test	N,Z,C
UADD16	{Rd,} Rn, Rm	Unsigned Add 16	GE
UADD8	{Rd,} Rn, Rm	Unsigned Add 8	GE
USAX	{Rd,} Rn, Rm	Unsigned Subtract and Add with Exchange	GE

12.6.9 Bitfield Instructions

The table below shows the instructions that operate on adjacent sets of bits in registers or bitfields.

Table 12-24. Packing and Unpacking Instructions

Mnemonic	Description
BFC	Bit Field Clear
BFI	Bit Field Insert
SBFX	Signed Bit Field Extract
SXTB	Sign extend a byte
SXTH	Sign extend a halfword
UBFX	Unsigned Bit Field Extract
UXTB	Zero extend a byte
UXTH	Zero extend a halfword

12.6.11.4 DSB

Data Synchronization Barrier.

Syntax

```
DSB{cond}
```

where:

cond is an optional condition code, see “Conditional Execution” .

Operation

DSB acts as a special data synchronization memory barrier. Instructions that come after the DSB, in program order, do not execute until the DSB instruction completes. The DSB instruction completes when all explicit memory accesses before it complete.

Condition Flags

This instruction does not change the flags.

Examples

```
DSB ; Data Synchronisation Barrier
```

12.6.11.5 ISB

Instruction Synchronization Barrier.

Syntax

```
ISB{cond}
```

where:

cond is an optional condition code, see “Conditional Execution” .

Operation

ISB acts as an instruction synchronization barrier. It flushes the pipeline of the processor, so that all instructions following the ISB are fetched from cache or memory again, after the ISB instruction has been completed.

Condition Flags

This instruction does not change the flags.

Examples

```
ISB  ; Instruction Synchronisation Barrier
```

12.9.1.9 System Handler Priority Register 1

Name: SCB_SHPR1

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
PRI_6							

15	14	13	12	11	10	9	8
PRI_5							

7	6	5	4	3	2	1	0
PRI_4							

- **PRI_6: Priority**

Priority of system handler 6, UsageFault.

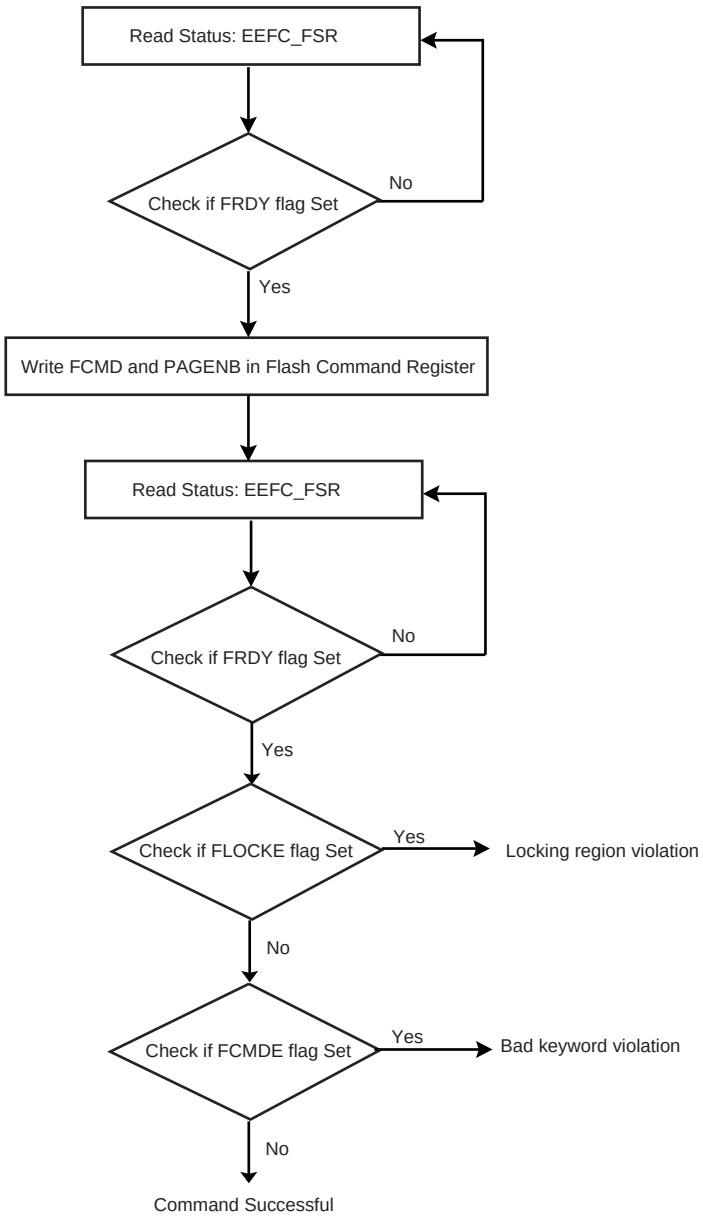
- **PRI_5: Priority**

Priority of system handler 5, BusFault.

- **PRI_4: Priority**

Priority of system handler 4, MemManage.

Figure 20-7. Command State Chart



20.4.3.1 Get Flash Descriptor Command

This command provides the system with information on the Flash organization. The system can take full advantage of this information. For instance, a device could be replaced by one with more Flash capacity, and so the software is able to adapt itself to the new configuration.

To get the embedded Flash descriptor, the application writes the GETD command in EEFC_FCR. The first word of the descriptor can be read by the software application in EEFC_FRR as soon as the FRDY flag in EEFC_FSR rises. The next reads of EEFC_FRR provide the following word of the descriptor. If extra read operations to EEFC_FRR are done after the last word of the descriptor has been returned, the EEFC_FRR value is 0 until the next valid command.

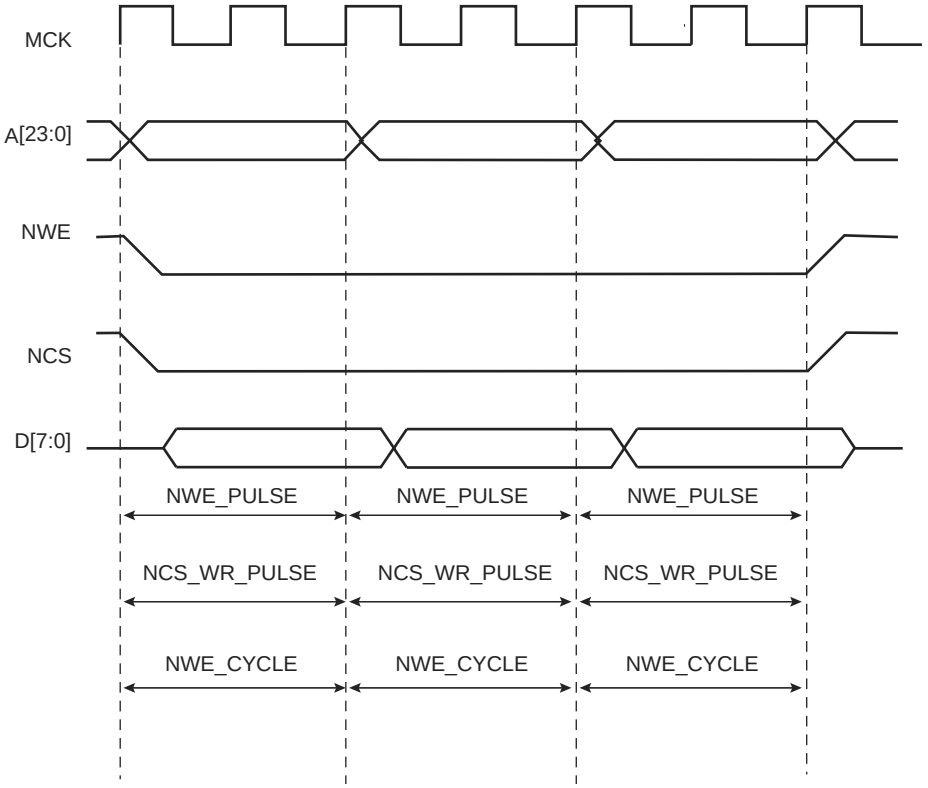
NWE_HOLD = NWE_CYCLE - NWE_SETUP - NWE_PULSE

NCS_WR_HOLD = NWE_CYCLE - NCS_WR_SETUP - NCS_WR_PULSE

26.9.3.4 Null Delay Setup and Hold

If null setup parameters are programmed for NWE and/or NCS, NWE and/or NCS remain active continuously in case of consecutive write cycles in the same memory (see Figure 26-10). However, for devices that perform write operations on the rising edge of NWE or NCS, such as SRAM, either a setup or a hold must be programmed.

Figure 26-10. Null Setup and Hold Values of NCS and NWE in Write Cycle



26.9.3.5 Null Pulse

Programming null pulse is not permitted. Pulse must be at least set to 1. A null value leads to unpredictable behavior.

26.9.4 Write Mode

The bit WRITE_MODE in the SMC_MODE register of the corresponding chip select indicates which signal controls the write operation.

26.9.4.1 Write is Controlled by NWE (WRITE_MODE = 1):

Figure 26-11 shows the waveforms of a write operation with WRITE_MODE set . The data is put on the bus during the pulse and hold steps of the NWE signal. The internal data buffers are switched to Output mode after the NWE_SETUP time, and until the end of the write cycle, regardless of the programmed waveform on NCS.

26.16.4 SMC MODE Register

Name: SMC_MODE[0..3]

Address: 0x400E000C [0], 0x400E001C [1], 0x400E002C [2], 0x400E003C [3]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	PS		–	–	–	PMEN
23	22	21	20	19	18	17	16
–	–	–	TDF_MODE	TDF_CYCLES			
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	EXNW_MODE		–	–	WRITE_MODE	READ_MODE

This register can only be written if the WPEN bit is cleared in the “SMC Write Protection Mode Register” .

- **READ_MODE: Read Mode**

0: The read operation is controlled by the NCS signal.

– If TDF cycles are programmed, the external bus is marked busy after the rising edge of NCS.

– If TDF optimization is enabled (TDF_MODE =1), TDF wait states are inserted after the setup of NCS.

1: The read operation is controlled by the NRD signal.

– If TDF cycles are programmed, the external bus is marked busy after the rising edge of NRD.

– If TDF optimization is enabled (TDF_MODE =1), TDF wait states are inserted after the setup of NRD.

- **WRITE_MODE: Write Mode**

0: The write operation is controlled by the NCS signal.

– If TDF optimization is enabled (TDF_MODE =1), TDF wait states will be inserted after the setup of NCS.

1: The write operation is controlled by the NWE signal.

– If TDF optimization is enabled (TDF_MODE =1), TDF wait states will be inserted after the setup of NWE.

- **EXNW_MODE: NWAIT Mode**

The NWAIT signal is used to extend the current read or write signal. It is only taken into account during the pulse phase of the read and write controlling signal. When the use of NWAIT is enabled, at least one cycle hold duration must be programmed for the read and write controlling signal.

Value	Name	Description
0	DISABLED	Disabled
1	–	Reserved
2	FROZEN	Frozen Mode
3	READY	Ready Mode

- Disabled Mode: The NWAIT input signal is ignored on the corresponding Chip Select.
- Frozen Mode: If asserted, the NWAIT signal freezes the current read or write cycle. After deassertion, the read/write cycle is resumed from the point where it was stopped.

37.7.14 TC Block Mode Register

Name: TC_BMR

Address: 0x400100C4 (0), 0x400140C4 (1)

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	MAXFILT	

23	22	21	20	19	18	17	16
MAXFILT				–	–	IDXPHB	SWAP

15	14	13	12	11	10	9	8
INVIDX	INVB	INVA	EDGPHA	QDTRANS	SPEEDEN	POSEN	QDEN

7	6	5	4	3	2	1	0
–	–	TC2XC2S		TC1XC1S		TC0XC0S	

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

- **TC0XC0S: External Clock Signal 0 Selection**

Value	Name	Description
0	TCLK0	Signal connected to XC0: TCLK0
1	–	Reserved
2	TIOA1	Signal connected to XC0: TIOA1
3	TIOA2	Signal connected to XC0: TIOA2

- **TC1XC1S: External Clock Signal 1 Selection**

Value	Name	Description
0	TCLK1	Signal connected to XC1: TCLK1
1	–	Reserved
2	TIOA0	Signal connected to XC1: TIOA0
3	TIOA2	Signal connected to XC1: TIOA2

- **TC2XC2S: External Clock Signal 2 Selection**

Value	Name	Description
0	TCLK2	Signal connected to XC2: TCLK2
1	–	Reserved
2	TIOA0	Signal connected to XC2: TIOA0
3	TIOA1	Signal connected to XC2: TIOA1

- **QDEN: Quadrature Decoder Enabled**

0: Disabled.

1: Enables the QDEC (filter, edge detection and quadrature decoding).

Quadrature decoding (direction change) can be disabled using QDTRANS bit.

38.14.5 HSMCI Argument Register

Name: HSMCI_ARGR

Address: 0x40000010

Access: Read/Write

31	30	29	28	27	26	25	24
ARG							
23	22	21	20	19	18	17	16
ARG							
15	14	13	12	11	10	9	8
ARG							
7	6	5	4	3	2	1	0
ARG							

- **ARG: Command Argument**

- **OVRE: Overrun (if FERRCTRL = 1, cleared by writing in HSMCI_CMDR or cleared on read if FERRCTRL = 0)**

0: No error.

1: At least one 8-bit received data has been lost (not read).

If FERRCTRL = 1 in HSMCI_CFG, OVRE is cleared on read.

If FERRCTRL = 0 in HSMCI_CFG, OVRE is cleared by writing HSMCI_CMDR.

- **UNRE: Underrun (if FERRCTRL = 1, cleared by writing in HSMCI_CMDR or cleared on read if FERRCTRL = 0)**

0: No error.

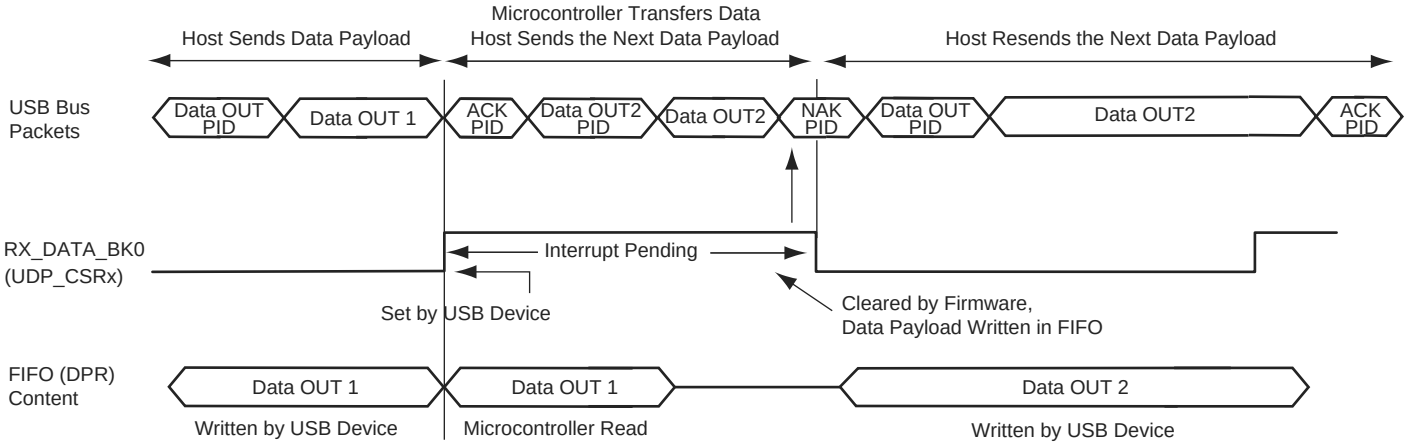
1: At least one 8-bit data has been sent without valid information (not written).

If FERRCTRL = 1 in HSMCI_CFG, OVRE is cleared on read.

If FERRCTRL = 0 in HSMCI_CFG, OVRE is cleared by writing HSMCI_CMDR.

Note: 1. HSMCI_RCR, HSMCI_RNCR, HSMCI_TCR, HSMCI_TNCR are PDC registers.

Figure 40-9. Data OUT Transfer for Non Ping-pong Endpoints

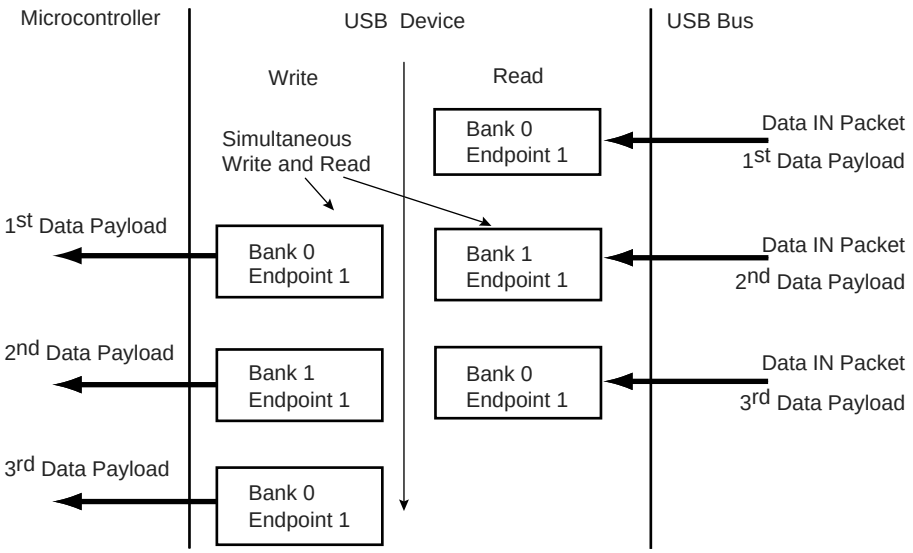


An interrupt is pending while the flag RX_DATA_BK0 is set. Memory transfer between the USB device, the FIFO and microcontroller memory is not possible after RX_DATA_BK0 has been cleared. Otherwise, the USB device would accept the next Data OUT transfer and overwrite the current Data OUT packet in the FIFO.

Using Endpoints With Ping-pong Attributes

During isochronous transfer, using an endpoint with ping-pong attributes is obligatory. To be able to guarantee a constant bandwidth, the microcontroller must read the previous data payload sent by the host, while the current data payload is received by the USB device. Thus two banks of memory are used. While one is available for the microcontroller, the other one is locked by the USB device.

Figure 40-10. Bank Swapping in Data OUT Transfers for Ping-pong Endpoints



When using a ping-pong endpoint, the following procedures are required to perform Data OUT transactions:

1. The host generates a Data OUT packet.
2. This packet is received by the USB device endpoint. It is written in the endpoint's FIFO Bank 0.
3. The USB device sends an ACK PID packet to the host. The host can immediately send a second Data OUT packet. It is accepted by the device and copied to FIFO Bank 1.
4. The microcontroller is notified that the USB device has received a data payload, polling RX_DATA_BK0 in the endpoint's UDP_CSRx. An interrupt is pending for this endpoint while RX_DATA_BK0 is set.

40.6.3.2 Entering Attached State

To enable integrated pull-up, the PUON bit in the UDP_TXVC register must be set.

Warning: To write to the UDP_TXVC register, MCK clock must be enabled on the UDP. This is done in the Power Management Controller.

After pull-up connection, the device enters the powered state. In this state, the UDPCK and MCK must be enabled in the Power Management Controller. The transceiver can remain disabled.

40.6.3.3 From Powered State to Default State

After its connection to a USB host, the USB device waits for an end-of-bus reset. The unmaskable flag ENDBUSRES is set in the UDP_ISR and an interrupt is triggered.

Once the ENDBUSRES interrupt has been triggered, the device enters Default State. In this state, the UDP software must:

- Enable the default endpoint, setting the EPEDS flag in the UDP_CSR0 and, optionally, enabling the interrupt for endpoint 0 by writing 1 to the UDP_IER. The enumeration then begins by a control transfer.
- Configure the interrupt mask register which has been reset by the USB reset detection
- Enable the transceiver clearing the TXVDIS flag in the UDP_TXVC register.

In this state UDPCK and MCK must be enabled.

Warning: Each time an ENDBUSRES interrupt is triggered, the Interrupt Mask Register and UDP_CSRs have been reset.

40.6.3.4 From Default State to Address State

After a set address standard device request, the USB host peripheral enters the address state.

Warning: Before the device enters in address state, it must achieve the Status IN transaction of the control transfer, i.e., the UDP device sets its new address once the TXCOMP flag in the UDP_CSR0 has been received and cleared.

To move to address state, the driver software sets the FADDEN flag in the UDP_GLB_STAT register, sets its new address, and sets the FEN bit in the UDP_FADDR register.

40.6.3.5 From Address State to Configured State

Once a valid Set Configuration standard request has been received and acknowledged, the device enables endpoints corresponding to the current configuration. This is done by setting the EPEDS and EPTYPE fields in the UDP_CSRx and, optionally, enabling corresponding interrupts in the UDP_IER.

40.6.3.6 Entering in Suspend State

When a Suspend (no bus activity on the USB bus) is detected, the RXSUSP signal in the UDP_ISR is set. This triggers an interrupt if the corresponding bit is set in the UDP_IMR. This flag is cleared by writing to the UDP_ICR. Then the device enters Suspend Mode.

In this state bus powered devices must drain no more than 2.5 mA from the 5V VBUS. As an example, the microcontroller switches to slow clock, disables the PLL and main oscillator, and goes into Idle Mode. It may also switch off other devices on the board.

The USB device peripheral clocks can be switched off. Resume event is asynchronously detected. MCK and UDPCK can be switched off in the Power Management controller and the USB transceiver can be disabled by setting the TXVDIS bit in the UDP_TXVC register.

Warning: Read, write operations to the UDP registers are allowed only if MCK is enabled for the UDP peripheral. Switching off MCK for the UDP peripheral must be one of the last operations after writing to the UDP_TXVC register and acknowledging the RXSUSP.

- **TAG: Tag Selection Mode**

Value	Name	Description
0	DIS	Tag selection mode disabled. Using USER_SEL to select the channel for the conversion.
1	EN	Tag selection mode enabled

- **MAXS: Maximum Speed Mode**

Value	Name	Description
0	NORMAL	Normal mode
1	MAXIMUM	Maximum speed mode enabled

- **STARTUP: Startup Time Selection**

Value	Name	Description
0	0	0 periods of peripheral clock
1	8	8 periods of peripheral clock
2	16	16 periods of peripheral clock
3	24	24 periods of peripheral clock
4	64	64 periods of peripheral clock
5	80	80 periods of peripheral clock
6	96	96 periods of peripheral clock
7	112	112 periods of peripheral clock
8	512	512 periods of peripheral clock
9	576	576 periods of peripheral clock
10	640	640 periods of peripheral clock
11	704	704 periods of peripheral clock
12	768	768 periods of peripheral clock
13	832	832 periods of peripheral clock
14	896	896 periods of peripheral clock
15	960	960 periods of peripheral clock
16	1024	1024 periods of peripheral clock
17	1088	1088 periods of peripheral clock
18	1152	1152 periods of peripheral clock
19	1216	1216 periods of peripheral clock
20	1280	1280 periods of peripheral clock
21	1344	1344 periods of peripheral clock
22	1408	1408 periods of peripheral clock
23	1472	1472 periods of peripheral clock
24	1536	1536 periods of peripheral clock
25	1600	1600 periods of peripheral clock
26	1664	1664 periods of peripheral clock
27	1728	1728 periods of peripheral clock

43.7.9 DACC Interrupt Mask Register

Name: DACC_IMR

Address: 0x4003C02C

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	TXBUFE	ENDTX	EOC	TXRDY

The following configuration values are valid for all listed bit names of this register:

0: Corresponding interrupt is not enabled

1: Corresponding interrupt is enabled

- **TXRDY: Transmit Ready Interrupt Mask**
- **EOC: End of Conversion Interrupt Mask**
- **ENDTX: End of Transmit Buffer Interrupt Mask**
- **TXBUFE: Transmit Buffer Empty Interrupt Mask**

Table 44-5. Core Power Supply Brownout Detector Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{T-}	Supply Falling Threshold(1)		0.98	1.0	1.04	V
V_{hys}	Hysteresis Voltage		–	–	110	mV
V_{T+}	Supply Rising Threshold		0.8	1.0	1.08	V
t_{RST}	Reset Period	V_{DDIO} rising from 0 to 1.2V ± 10%	90	–	320	µs
I_{DDON}	Current Consumption on VDDCORE	Brownout Detector enabled	–	–	24	µA
I_{DDOFF}		Brownout Detector disabled	–	–	2	
I_{DD33ON}	Current Consumption on VDDIO	Brownout Detector enabled	–	–	24	µA
$I_{DD33OFF}$		Brownout Detector disabled	–	–	2	
t_{d-}	V_{T-} Detection Propagation Time	VDDCORE = V_{T+} to (V_{T-} - 100mV)	–	200	300	ns
t_{START}	Startup Time	From disabled state to enabled state	–	–	300	µs

Note: 1. The product is guaranteed to be functional at V_{T-}

Figure 44-1. Core Brownout Output Waveform

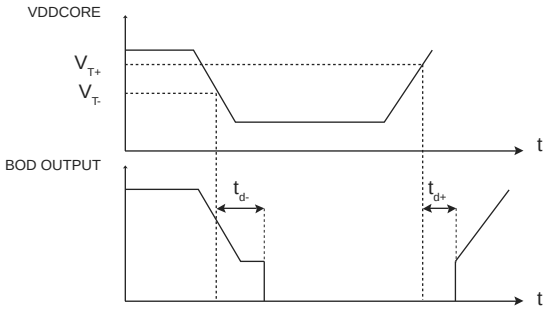


Table 44-6. VDDIO Supply Monitor

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_T	Supply Monitor Threshold	16 selectable steps	1.6	–	3.4	V
$V_{T(accuracy)}$	Threshold Level Accuracy	[-40/+105°C]	-2.5	–	+2.5	%
V_{hys}	Hysteresis Voltage	–	–	20	30	mV
I_{DDON}	Current Consumption	Enabled	–	23	40	µA
I_{DDOFF}		Disabled	–	0.02	2	
t_{START}	Startup Time	From disabled state to enabled state	–	–	300	µs

Table 47-1. Ordering Codes for SAM4S Devices (Continued)

Ordering Code	MRL	Flash (Kbytes)	SRAM (Kbytes)	Package	Carrier Type	Operating Temperature Range
ATSAM4S8CA-CFU	A	512	128	VFBGA100	Tray	Industrial (-40°C to +85°C)
ATSAM4S8CB-CFU	B					
ATSAM4S8CA-AU	A	512	128	LQFP100	Tray	Industrial (-40°C to +85°C)
ATSAM4S8CB-AU	B					
ATSAM4S8CA-CFN	A	512	128	VFBGA100	Tray	Industrial (-40°C to +105°C)
ATSAM4S8CB-CFN	B					
ATSAM4S8CA-AN	A	512	128	LQFP100	Tray	Industrial (-40°C to +105°C)
ATSAM4S8CB-AN	B					
ATSAM4S8BA-MU	A	512	128	QFN64	Tray	Industrial (-40°C to +85°C)
ATSAM4S8BB-MU	B					
ATSAM4S8BA-AU	A	512	128	LQFP64	Tray	Industrial (-40°C to +85°C)
ATSAM4S8BB-AU	B					
ATSAM4S8BA-UUR	A	512	128	WLCSP64	Reel	Industrial (-40°C to +85°C)
ATSAM4S8BB-UUR	B					
ATSAM4S8BA-AN	A	512	128	LQFP64	Tray	Industrial (-40°C to +105°C)
ATSAM4S8BB-AN	B					
ATSAM4S4CA-CU	A	256	64	TFBGA100	Tray	Industrial (-40°C to +85°C)
ATSAM4S4CB-CU	B					
ATSAM4S4CA-CFU	A	256	64	VFBGA100	Tray	Industrial (-40°C to +85°C)
ATSAM4S4CB-CFU	B					
ATSAM4S4CA-AU	A	256	64	LQFP100	Tray	Industrial (-40°C to +85°C)
ATSAM4S4CB-AU	B					
ATSAM4S4CA-AN	A	256	64	LQFP100	Tray	Industrial (-40°C to +105°C)
ATSAM4S4CB-AN	B					
ATSAM4S4BA-MU	A	256	64	QFN64	Tray	Industrial (-40°C to +85°C)
ATSAM4S4BB-MU	B					
ATSAM4S4BA-AU	A	256	64	LQFP64	Tray	Industrial (-40°C to +85°C)
ATSAM4S4BB-AU	B					
ATSAM4S4BA-UUR	A	256	64	WLCSP64	Reel	Industrial (-40°C to +85°C)
ATSAM4S4BB-UUR	B					
ATSAM4S4BA-AN	A	256	64	LQFP64	Tray	Industrial (-40°C to +105°C)
ATSAM4S4BB-AN	B					
ATSAM4S4AA-MU	A	256	64	QFN48	Tray	Industrial (-40°C to +85°C)
ATSAM4S4AB-MU	B					
ATSAM4S4AA-AU	A	256	64	LQFP48	Tray	Industrial (-40°C to +85°C)
ATSAM4S4AB-AU	B					

Table 49-4. SAM4S Datasheet Rev. 11100H Revision History (Continued)

Doc. Date	Changes
08-Jan-15	Added “Symbol” column to Table 44-57 ”Static Performance Characteristics”, Table 44-58 ”Dynamic Performance Characteristics”, Table 44-59 ”Analog Outputs”, and Table 44-60 ”Analog Comparator Characteristics” Section 44.11 “Temperature Sensor”: specified instances of “27°C” as ambient temperature Table 44-63 ”I/O Characteristics”: added parameter “Maximum I/O skew” Section 44.12.3.1 “Maximum SPI Frequency”: - under “Master Write Mode”, replaced “the maximum SPI frequency is the one from the pad” with “the maximum SPI frequency is defined by the pin FreqMax value - updated content under “Master Read Mode” Table 44-65 ”SSC Timings”: in Min/Max values for SSC_4 and SSC_7, corrected links to footnote 2 Section 44.12.9 “Embedded Flash Characteristics”: in first paragraph, corrected “field FWS of the MC_FMR” to “field FWS of the EEFC_FMR”
	Section 45. “Mechanical Characteristics” Inserted heading Section 45.1 “100-lead LQFP Mechanical Characteristics” Inserted heading Section 45.2 “100-ball TFBGA Mechanical Characteristics” Inserted heading Section 45.3 “100-ball VFBGA Mechanical Characteristics” Inserted heading Section 45.4 “64-lead LQFP Mechanical Characteristics” Table 45-16 ”LQFP Package Characteristics”: corrected title (was “LQFP and QFN Package Characteristics”) Inserted heading Section 45.5 “64-lead QFN Mechanical Characteristics” Inserted heading Section 45.6 “64-ball WLCSP Mechanical Characteristics” Inserted heading Section 45.7 “48-lead LQFP Mechanical Characteristics” and added sentence “This package respects the recommendations of the NEMI User Group.” Inserted heading Section 45.8 “48-lead QFN Mechanical Characteristics” and added sentence “This package respects the recommendations of the NEMI User Group.” Table 45-29 ”48-lead QFN Package Characteristics”: corrected title (was “48-lead LQFP Package Characteristics”) and changed Moisture Sensitivity Level from 1 to 3 Table 45-30 ”48-lead QFN Package Reference”: corrected title (was “48-lead LQFP Package Reference”)
	Added Section 46. “Marking”
	Section 47. “Ordering Information”: Table 47-1 ”Ordering Codes for SAM4S Devices”: added ordering codes for MRL ‘B’
	Section 48. “Errata” Section 48.1 “Errata SAM4SD32/SD16/SA16/S16/S8 Rev. A Parts”: added Section 48.1.5 “Low-power Mode” Added Section 48.2 “Errata SAM4SD32/SD16/SA16/S16/S8 Rev. B Parts” Section 48.3 “Errata SAM4S4/S2 Rev. A Parts”: added Section 48.3.4 “Low-power Mode” Added Section 48.4 “Errata SAM4S4/S2 Rev. B Parts”

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Table 49-6. SAM4S Datasheet Rev. 11100F 29-Jan-14 Revision History (Continued)

Doc. Date	Changes
	Section 20. "Enhanced Embedded Flash Controller (EEFC)" Corrected partial programming boundary from 32-bit to 64-bit and reworked Section 20.4.3.2 "Write Commands" and all sub-sections with figures Figure 20-7 Full Page Programming to Figure 20-9 Programming Bytes in the Flash. In Section 20.4.3.3 "Erase Commands", modified paragraph on Erase pages (EPA) and Erase sector (ES) commands, as well as Table 20-4 "FARG Field for EPA Command". Added "small sector" text as limitations in Table 20-4 "FARG Field for EPA Command". Added notes when FARG exceeds limits in Section 20.4.3.4 "Lock Bit Protection". Re-worked Section 20.4.3.5 "GPNVM Bit" and added title in Section 20.4.3.6 "Calibration Bit". In Section 20.5.2 "EEFC Flash Command Register", changed the description of FARG field accordingly. Replaced NVIC by "interrupt controller" everywhere in the document.
	Section 23. "Cyclic Redundancy Check Calculation Unit (CRCCU)" Section 23.1 "Description": added sentence with information on CRCCU and data integrity check. Section 23.2 "Embedded Characteristics": removed bullet 'Single AHB Master Interface'. Inserted two new bullets on data integrity check and background task. Added note. Modified access type of Section 23.7.7 "CRCCU DMA Interrupt Mask Register". Section 23.6.2 "Transfer Control Register": updated IEN bit description Section 23.6.3 "Transfer Reference Register": replaced "compared with that register" with "compared with this field" in REFCRC field description Updated bit descriptions in Section 23.7.2 "CRCCU DMA Enable Register" to Section 23.7.6 "CRCCU DMA Interrupt Disable Register", in Section 23.7.8 "CRCCU DMA Interrupt Status Register", in Section 23.7.9 "CRCCU Control Register" and in Section 23.7.12 "CRCCU Interrupt Enable Register" to Section 23.7.15 "CRCCU Interrupt Status Register".
	Section 27. "Peripheral DMA Controller (PDC)" Replaced "on- and/or off-chip" with "target" in Section 27.1 "Description"and Section 27.4.2 "Memory Pointers". Added last paragraph to Section 27.4.1 "Configuration" specifying that the peripheral clock must be enabled for a PDC transfer.
	Section 28. "Clock Generator" Added Section 28.5.5 "Switching Main Clock between the Main RC Oscillator and Fast Crystal Oscillator".
	Section 29. "Power Management Controller (PMC)" Reworked Section 29.11 "Fast Startup" and added Section 29.12 "Start-up from Embedded Flash" Reworked Section 29.13 "Main Clock Failure Detector". Enhanced Section 29.14 "Programming Sequence" Enhanced Section 29.14 "Programming Sequence" Section 29.16 "Register Write Protection": Changed section title and re-worked content. In Section 29.17.21 "PMC Write Protection Mode Register" and Section 29.17.25 "PMC Peripheral Clock Status Register 1": Changed register names and modified bit and field descriptions.
	Section 30. "Chip Identifier (CHIPID)" Section 30.3.1 "Chip ID Register": Modified "ARCH: Architecture Identifier" bit description table to show only SAM4S.
	Section 31. "Parallel Input/Output Controller (PIO)" Section 31.5.14 "Register Write Protection": Changed section title and revised content. Section 31.7.46 "PIO Write Protection Mode Register": Modified register name and aligned bit descriptions. Replaced list of protectable registers with cross-reference to section "Register Write Protection". Section 31.7.47 "PIO Write Protection Status Register": Modified register name and aligned bit descriptions. Removed note.

Table 49-10. SAM4S Datasheet Rev. 11100B 31-Jul-12 Revision History (Continued)

Doc. Rev. 11100B	Comments	Change Request Ref.
	RTC	
	In Section 16.6.2 “RTC Mode Register” on page 303, formulas associated with conditions HIGHPPM = 1 and HIGHPPM = 0 have been swapped, text has been clarified.	7950
	In Section 16.5.7 “RTC Accurate Clock Calibration” on page 299, paragraph describing RTC clock calibration circuitry correction updated with mention of crystal drift.	7952
	SUPC	
	References to WFE instructions deleted in Section 18.3.3 “Core Voltage Regulator Control/Backup Low-power Mode” on page 328.	rfo
	Supply monitor threshold values modified in Section 18.3.4 “Supply Monitor” on page 328.	
	SMTH bit table replaced by a cross-reference to Electrical characteristics in Section 18.4.4 “Supply Controller Supply Monitor Mode Register” on page 338.	
	Typo in Section 18.4.8 “Supply Controller Status Register” on page 343 is now fixed.	8024
	“half” replaced with “first half” in Section 18.4.6 “Supply Controller Wake-up Mode Register” on page 340 and in Section 18.4.7.2 “Low Power Debouncer Inputs” on page 295.	8067
	Figure 18-4 on page 331 modified.	
	Push-to-Break figure example Figure 18-6 on page 333 added, title of Figure 18-5 on page 333 modified.	8064, 8082
	“square waveform ..” changed to “duty cycle ..” in Section 18.4.7.2 “Low Power Debouncer Inputs” on page 295.	8082 8226
	Switching time of slow crystal oscillator updated in Section 18.3.2 “Slow Clock Generator” on page 328.	8266
	EEFC	
	Added GPNVM command line in Section • “FARG: Flash Command Argument” on page 368.	8076
	Unique identifier address changed in Section 20.4.3.8 “Unique Identifier” on page 363.	8274
	User Signature address changed in Section 20.4.3.9 “User Signature” on page 363.	
	Changed the System Controller base address from 0x400E0800 to 0x400E0A00 in Section 20.5 “Enhanced Embedded Flash Controller (EEFC) User Interface” on page 365.	rfo
	FFPI	
	All references, tables, figures related to 48-bit devices cleared in this whole chapter.	rfo
	CMCC	
	New chapter.	
	CRCCU	
	Typos: CCIT802 corrected to CCITT802, CCIT16 corrected to CCITT16 in Section 23.5.1 “CRC Calculation Unit” on page 399 and Section 23.7.10 “CRCCU Mode Register” on page 414. TRC_RC corrected to TR_CRC in Section 23.7.10 “CRCCU Mode Register” on page 414.	7803
	SMC	
	“turned out” changed to “switched to output mode” in Section 26.8.4 “Write Mode” on page 450.	7925
	Removed DBW which is not required for 8-bit only in Section 26.15.4 “SMC MODE Register” on page 476.	8307