Welcome to E-XFL.COM

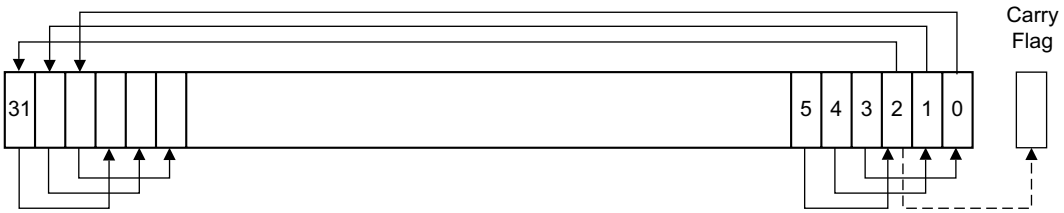
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	EBI/EMI, I²C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4sd32cb-an

Figure 12-11. ROR #3

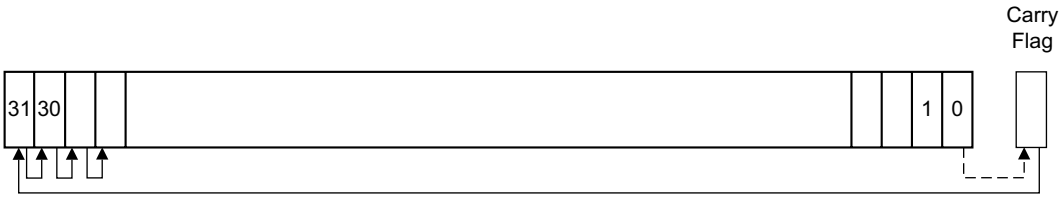


RRX

Rotate right with extend moves the bits of the register *Rm* to the right by one bit; and it copies the carry flag into bit[31] of the result. See Figure 12-12.

When the instruction is RRXS or when RRX is used in *Operand2* with the instructions MOVS, MVNS, ANDS, ORRS, ORNS, EORS, BICS, TEQ or TST, the carry flag is updated to bit[0] of the register *Rm*.

Figure 12-12. RRX



12.6.3.5 Address Alignment

An aligned access is an operation where a word-aligned address is used for a word, dual word, or multiple word access, or where a halfword-aligned address is used for a halfword access. Byte accesses are always aligned.

The Cortex-M4 processor supports unaligned access only for the following instructions:

- LDR, LDRT
- LDRH, LDRHT
- LDRSH, LDRSHT
- STR, STRT
- STRH, STRHT

All other load and store instructions generate a usage fault exception if they perform an unaligned access, and therefore their accesses must be address-aligned. For more information about usage faults, see “Fault Handling” .

Unaligned accesses are usually slower than aligned accesses. In addition, some memory regions might not support unaligned accesses. Therefore, ARM recommends that programmers ensure that accesses are aligned. To avoid accidental generation of unaligned accesses, use the UNALIGN_TRP bit in the Configuration and Control Register to trap all unaligned accesses, see “Configuration and Control Register” .

12.6.3.6 PC-relative Expressions

A PC-relative expression or *label* is a symbol that represents the address of an instruction or literal data. It is represented in the instruction as the PC value plus or minus a numeric offset. The assembler calculates the required offset from the label and the address of the current instruction. If the offset is too big, the assembler produces an error.

- For B, BL, CBNZ, and CBZ instructions, the value of the PC is the address of the current instruction plus 4 bytes.

12.6.5 General Data Processing Instructions

The table below shows the data processing instructions.

Table 12-20. Data Processing Instructions

Mnemonic	Description
ADC	Add with Carry
ADD	Add
ADDW	Add
AND	Logical AND
ASR	Arithmetic Shift Right
BIC	Bit Clear
CLZ	Count leading zeros
CMN	Compare Negative
CMP	Compare
EOR	Exclusive OR
LSL	Logical Shift Left
LSR	Logical Shift Right
MOV	Move
MOVT	Move Top
MOVW	Move 16-bit constant
MVN	Move NOT
ORN	Logical OR NOT
ORR	Logical OR
RBIT	Reverse Bits
REV	Reverse byte order in a word
REV16	Reverse byte order in each halfword
REVSH	Reverse byte order in bottom halfword and sign extend
ROR	Rotate Right
RRX	Rotate Right with Extend
RSB	Reverse Subtract
SADD16	Signed Add 16
SADD8	Signed Add 8
SASX	Signed Add and Subtract with Exchange
SSAX	Signed Subtract and Add with Exchange
SBC	Subtract with Carry
SHADD16	Signed Halving Add 16
SHADD8	Signed Halving Add 8
SHASX	Signed Halving Add and Subtract with Exchange
SHSAX	Signed Halving Subtract and Add with Exchange

In most microcontroller implementations, the shareability and cache policy attributes do not affect the system behavior. However, using these settings for the MPU regions can make the application code more portable. The values given are for typical situations. In special systems, such as multiprocessor designs or designs with a separate DMA engine, the shareability attribute might be important. In these cases, refer to the recommendations of the memory device manufacturer.

15.5.3 Real-time Timer Value Register

Name: RTT_VR

Address: 0x400E1438

Access: Read-only

31	30	29	28	27	26	25	24
CRTV							

23	22	21	20	19	18	17	16
CRTV							

15	14	13	12	11	10	9	8
CRTV							

7	6	5	4	3	2	1	0
CRTV							

- **CRTV: Current Real-time Value**

Returns the current value of the Real-time Timer.

Note: As CRTV can be updated asynchronously, it must be read twice at the same value.

23.7.12 CRCCU Interrupt Enable Register

Name: CRCCU_IER

Address: 0x40044040

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–
15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–
7	6	5	4	3	2	1	0
–	–	–	–	–	–	–	ERRIER

- **ERRIER: CRC Error Interrupt Enable**

0: No effect

1: Enable interrupt

31.6.27 PIO Input Filter Slow Clock Enable Register

Name: PIO_IFSCER

Address: 0x400E0E84 (PIOA), 0x400E1084 (PIOB), 0x400E1284 (PIOC)

Access: Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

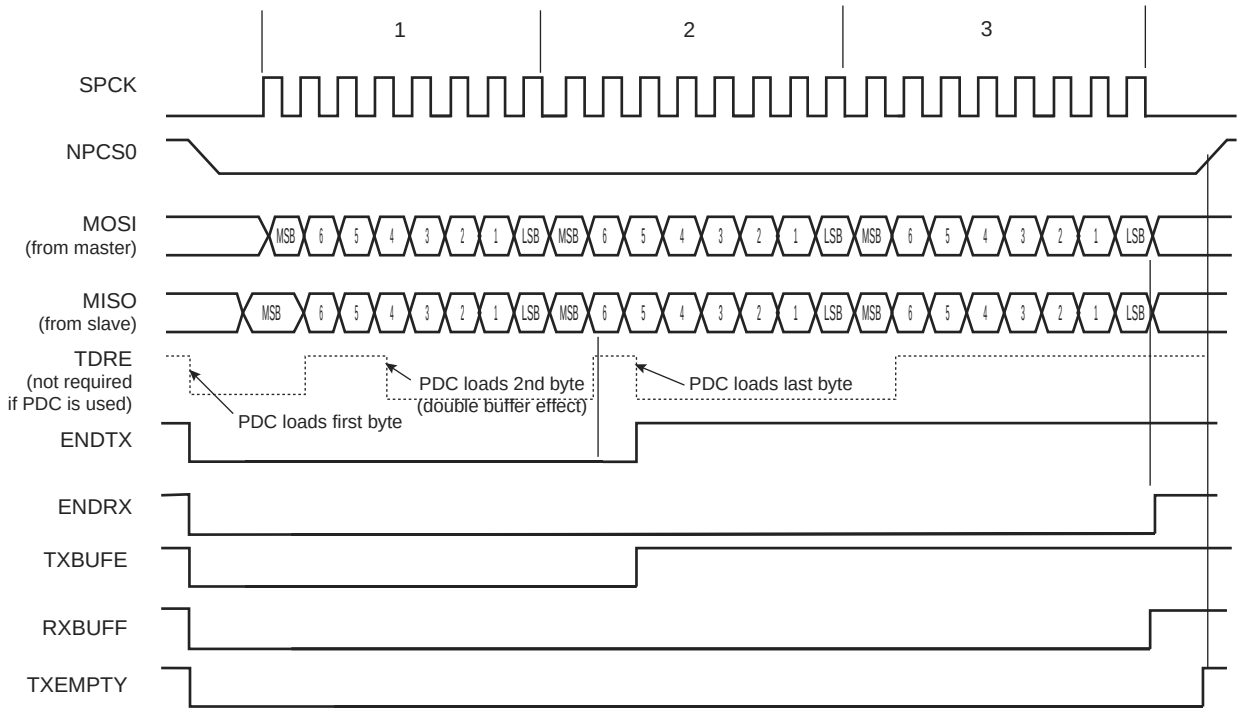
- **P0–P31: Slow Clock Debouncing Filtering Select**

0: No effect.

1: The debouncing filter is able to filter pulses with a duration < $t_{div\_slck}/2$.

Figure 33-9 shows the behavior of Transmission Register Empty (TXEMPTY), End of RX buffer (ENDRX), End of TX buffer (ENDTX), RX Buffer Full (RXBUFF) and TX Buffer Empty (TXBUFE) status flags within the SPI_SR during an 8-bit data transfer in Fixed mode with the PDC involved. The PDC is programmed to transfer and receive three units of data. The next pointer and counter are not used. The RDRF and TDRE are not shown because these flags are managed by the PDC when using the PDC.

Figure 33-9. PDC Status Register Flags Behavior



33.7.3.3 Clock Generation

The SPI Baud rate clock is generated by dividing the peripheral clock by a value between 1 and 255.

If the SCBR field in the SPI_CSR is programmed to 1, the operating baud rate is peripheral clock (see the electrical characteristics section for the SPCK maximum frequency). Triggering a transfer while SCBR is at 0 can lead to unpredictable results.

At reset, SCBR is 0 and the user has to program it to a valid value before performing the first transfer.

The divisor can be defined independently for each chip select, as it has to be programmed in the SCBR field. This allows the SPI to automatically adapt the baud rate for each interfaced peripheral without reprogramming.

33.7.3.4 Transfer Delays

Figure 33-10 shows a chip select transfer change and consecutive transfers on the same chip select. Three delays can be programmed to modify the transfer waveforms:

- Delay between the chip selects—programmable only once for all chip selects by writing the DLYBCS field in the SPI_MR. The SPI slave device deactivation delay is managed through DLYBCS. If there is only one SPI slave device connected to the master, the DLYBCS field does not need to be configured. If several slave devices are connected to a master, DLYBCS must be configured depending on the highest deactivation delay. Refer to the SPI slave device electrical characteristics.
- Delay before SPCK—independently programmable for each chip select by writing the DLYBS field. The SPI slave device activation delay is managed through DLYBS. Refer to the SPI slave device electrical characteristics to define DLYBS.

33.8.5 SPI Status Register

Name: SPI_SR

Address: 0x40008010

Access: Read-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	SPIENS
15	14	13	12	11	10	9	8
–	–	–	–	–	UNDES	TXEMPTY	NSSR
7	6	5	4	3	2	1	0
TXBUFE	RXBUFF	ENDTX	ENDRX	OVRES	MODF	TDRE	RDRF

- **RDRF: Receive Data Register Full (cleared by reading SPI_RDR)**

0: No data has been received since the last read of SPI_RDR.

1: Data has been received and the received data has been transferred from the shift register to SPI_RDR since the last read of SPI_RDR.

- **TDRE: Transmit Data Register Empty (cleared by writing SPI_TDR)**

0: Data has been written to SPI_TDR and not yet transferred to the shift register.

1: The last data written in the SPI_TDR has been transferred to the shift register.

TDRE equals zero when the SPI is disabled or at reset. The SPI enable command sets this bit to 1.

- **MODF: Mode Fault Error (cleared on read)**

0: No mode fault has been detected since the last read of SPI_SR.

1: A mode fault occurred since the last read of SPI_SR.

- **OVRES: Overrun Error Status (cleared on read)**

0: No overrun has been detected since the last read of SPI_SR.

1: An overrun has occurred since the last read of SPI_SR.

An overrun occurs when SPI_RDR is loaded at least twice from the shift register since the last read of the SPI_RDR.

- **ENDRX: End of RX Buffer (cleared by writing SPI_RCR or SPI_RNCR)**

0: The Receive Counter register has not reached 0 since the last write in SPI_RCR(1) or SPI_RNCR(1).

1: The Receive Counter register has reached 0 since the last write in SPI_RCR(1) or SPI_RNCR(1).

- **ENDTX: End of TX Buffer (cleared by writing SPI_TCR or SPI_TNCR)**

0: The Transmit Counter register has not reached 0 since the last write in SPI_TCR(1) or SPI_TNCR(1).

1: The Transmit Counter register has reached 0 since the last write in SPI_TCR(1) or SPI_TNCR(1).

- **RXBUFF: RX Buffer Full (cleared by writing SPI_RCR or SPI_RNCR)**

0: SPI_RCR(1) or SPI_RNCR(1) has a value other than 0.

1: Both SPI_RCR(1) and SPI_RNCR(1) have a value of 0.

34.8.7 TWI Interrupt Enable Register

Name: TWI_IER

Address: 0x40018024 (0), 0x4001C024 (1)

Access: Write-only

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
TXBUFE	RXBUFF	ENDTX	ENDRX	EOSACC	SCL_WS	ARBLST	NACK

7	6	5	4	3	2	1	0
–	OVRE	GACC	SVACC	–	TXRDY	RXRDY	TXCOMP

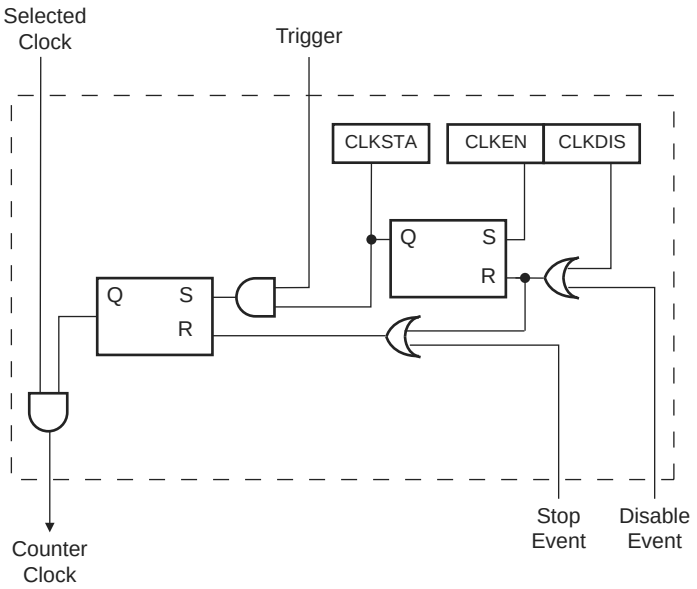
The following configuration values are valid for all listed bit names of this register:

0: No effect.

1: Enables the corresponding interrupt.

- **TXCOMP: Transmission Completed Interrupt Enable**
- **RXRDY: Receive Holding Register Ready Interrupt Enable**
- **TXRDY: Transmit Holding Register Ready Interrupt Enable**
- **SVACC: Slave Access Interrupt Enable**
- **GACC: General Call Access Interrupt Enable**
- **OVRE: Overrun Error Interrupt Enable**
- **NACK: Not Acknowledge Interrupt Enable**
- **ARBLST: Arbitration Lost Interrupt Enable**
- **SCL_WS: Clock Wait State Interrupt Enable**
- **EOSACC: End Of Slave Access Interrupt Enable**
- **ENDRX: End of Receive Buffer Interrupt Enable**
- **ENDTX: End of Transmit Buffer Interrupt Enable**
- **RXBUFF: Receive Buffer Full Interrupt Enable**
- **TXBUFE: Transmit Buffer Empty Interrupt Enable**

Figure 37-4. Clock Control



37.6.5 Operating Modes

Each channel can operate independently in two different modes:

- Capture mode provides measurement on signals.
- Waveform mode provides wave generation.

The TC operating mode is programmed with the WAVE bit in the TC_CMR.

In Capture mode, TIOA and TIOB are configured as inputs.

In Waveform mode, TIOA is always configured to be an output and TIOB is an output if it is not selected to be the external trigger.

37.6.6 Trigger

A trigger resets the counter and starts the counter clock. Three types of triggers are common to both modes, and a fourth external trigger is available to each mode.

Regardless of the trigger used, it will be taken into account at the following active edge of the selected clock. This means that the counter value can be read differently from zero just after a trigger, especially when a low frequency signal is selected as the clock.

The following triggers are common to both modes:

- Software Trigger: Each channel has a software trigger, available by setting SWTRG in TC_CCR.
- SYNC: Each channel has a synchronization signal SYNC. When asserted, this signal has the same effect as a software trigger. The SYNC signals of all channels are asserted simultaneously by writing TC_BCR (Block Control) with SYNC set.
- Compare RC Trigger: RC is implemented in each channel and can provide a trigger when the counter value matches the RC value if CPCTRG is set in the TC_CMR.

The channel can also be configured to have an external trigger. In Capture mode, the external trigger signal can be selected between TIOA and TIOB. In Waveform mode, an external event can be programmed on one of the following signals: TIOB, XC0, XC1 or XC2. This external event can then be programmed to perform a trigger by setting bit ENETRG in the TC_CMR.

If an external trigger is used, the duration of the pulses must be longer than the peripheral clock period in order to be detected.

37.7.2 TC Channel Mode Register: Capture Mode

Name: TC_CMRx [x=0..2] (CAPTURE_MODE)

Address: 0x40010004 (0)[0], 0x40010044 (0)[1], 0x40010084 (0)[2], 0x40014004 (1)[0], 0x40014044 (1)[1], 0x40014084 (1)[2]

Access: Read/Write

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–
23	22	21	20	19	18	17	16
–	–	–	–	LDRB		LDRA	
15	14	13	12	11	10	9	8
WAVE	CPCTRG	–	–	–	ABETRG	ETRGEDG	
7	6	5	4	3	2	1	0
LDBDIS	LDBSTOP	BURST		CLKI	TCCLKS		

This register can only be written if the WPEN bit is cleared in the TC Write Protection Mode Register.

- **TCCLKS: Clock Selection**

Value	Name	Description
0	TIMER_CLOCK1	Clock selected: internal MCK/2 clock signal (from PMC)
1	TIMER_CLOCK2	Clock selected: internal MCK/8 clock signal (from PMC)
2	TIMER_CLOCK3	Clock selected: internal MCK/32 clock signal (from PMC)
3	TIMER_CLOCK4	Clock selected: internal MCK/128 clock signal (from PMC)
4	TIMER_CLOCK5	Clock selected: internal SLCK clock signal (from PMC)
5	XC0	Clock selected: XC0
6	XC1	Clock selected: XC1
7	XC2	Clock selected: XC2

- **CLKI: Clock Invert**

0: Counter is incremented on rising edge of the clock.

1: Counter is incremented on falling edge of the clock.

- **BURST: Burst Signal Selection**

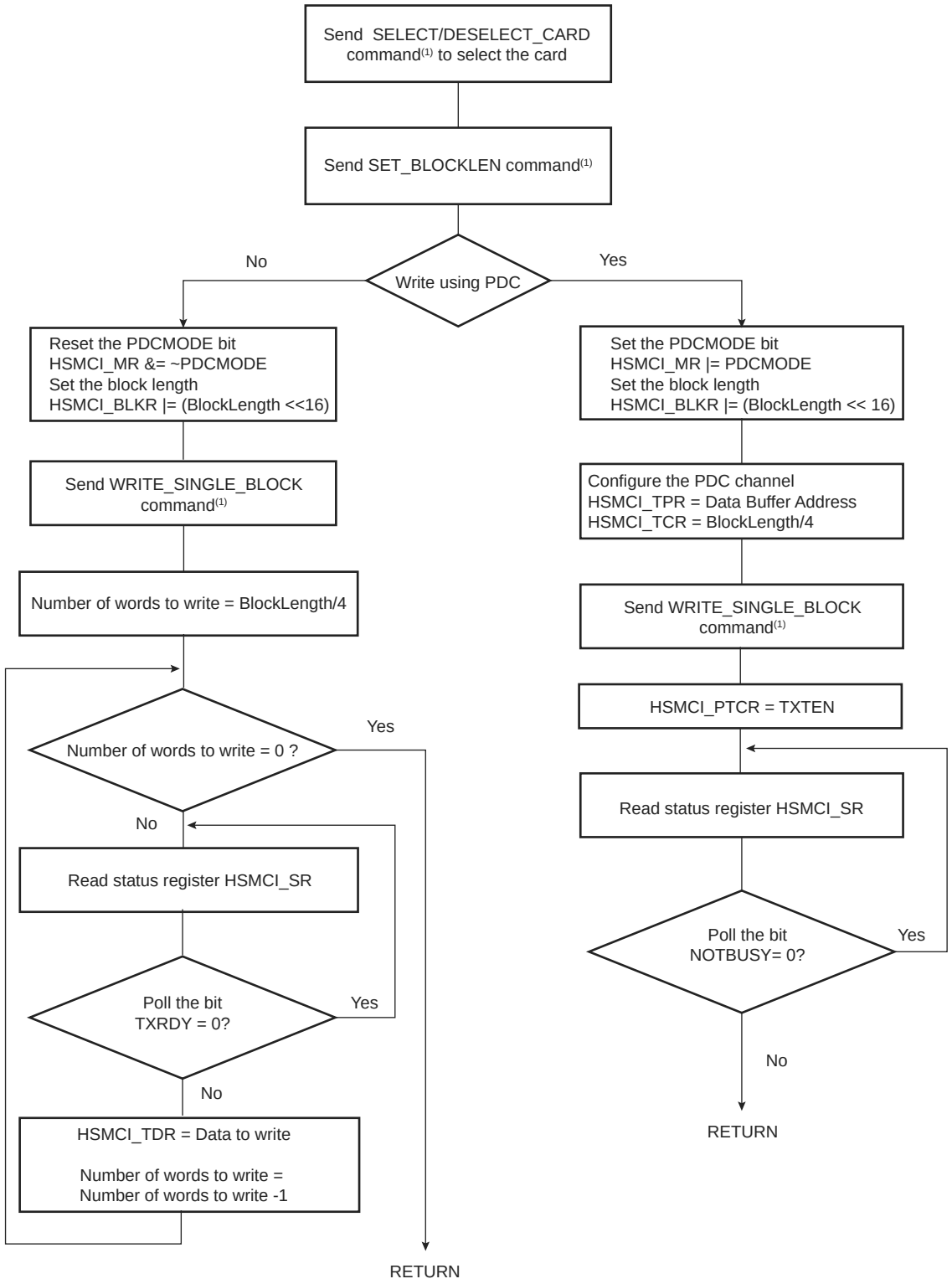
Value	Name	Description
0	NONE	The clock is not gated by an external signal.
1	XC0	XC0 is ANDed with the selected clock.
2	XC1	XC1 is ANDed with the selected clock.
3	XC2	XC2 is ANDed with the selected clock.

- **LDBSTOP: Counter Clock Stopped with RB Loading**

0: Counter clock is not stopped when RB loading occurs.

1: Counter clock is stopped when RB loading occurs.

Figure 38-9. Write Functional Flow Diagram



Note: 1. It is assumed that this command has been correctly sent (see Figure 38-7).

The flowchart in Figure 38-10 shows how to manage a multiple write block transfer with the PDC. Polling or interrupt method can be used to wait for the end of write according to the contents of the HSMCI_IMR.

38.14.7 HSMCI Block Register

Name: HSMCI_BLKR

Address: 0x40000018

Access: Read/Write

31	30	29	28	27	26	25	24
BLKLEN							
23	22	21	20	19	18	17	16
BLKLEN							
15	14	13	12	11	10	9	8
BCNT							
7	6	5	4	3	2	1	0
BCNT							

- **BCNT: MMC/SDIO Block Count - SDIO Byte Count**

This field determines the number of data byte(s) or block(s) to transfer.

The transfer data type and the authorized values for BCNT field are determined by the TRTYP field in the HSMCI Command Register (HSMCI_CMDR).

When TRTYP = 1 (MMC/SDCARD Multiple Block), BCNT can be programmed from 1 to 65535, 0 corresponds to an infinite block transfer.

When TRTYP = 4 (SDIO Byte), BCNT can be programmed from 1 to 511, 0 corresponds to 512-byte transfer. Values in range 512 to 65536 are forbidden.

When TRTYP = 5 (SDIO Block), BCNT can be programmed from 1 to 511, 0 corresponds to an infinite block transfer. Values in range 512 to 65536 are forbidden.

Warning: In SDIO Byte and Block modes (TRTYP = 4 or 5), writing the 7 last bits of BCNT field with a value which differs from 0 is forbidden and may lead to unpredictable results.

- **BLKLEN: Data Block Length**

This field determines the size of the data block.

Bits 16 and 17 must be configured to 0 if FBYTE is disabled.

Note: In SDIO Byte mode, BLKLEN field is not used.

- Method 3 (UPDM = 2): Same as Method 2 apart from the fact that the duty-cycle values of ALL synchronous channels are written by the Peripheral DMA Controller (see “Method 3: Automatic write of duty-cycle values and automatic trigger of the update”). The user can choose to synchronize the Peripheral DMA Controller transfer request with a comparison match (see Section 39.6.3 “PWM Comparison Units”), by the fields PTRM and PTRCS in the PWM_SCM register.

Table 39-5. Summary of the Update of Registers of Synchronous Channels

Register	UPDM = 0	UPDM = 1	UPDM = 2
Period Value (PWM_CPRDUPDx)	Write by the processor		
	Update is triggered at the next PWM period as soon as the bit UPDULOCK is set to ‘1’		
Dead-Time Values (PWM_DTUPDx)	Write by the processor		
	Update is triggered at the next PWM period as soon as the bit UPDULOCK is set to ‘1’		
Duty-Cycle Values (PWM_CDTYUPDx)	Write by the processor	Write by the processor	Write by the Peripheral DMA Controller
	Update is triggered at the next PWM period as soon as the bit UPDULOCK is set to ‘1’	Update is triggered at the next PWM period as soon as the update period counter has reached the value UPR	
Update Period Value (PWM_SCUPUPD)	Not applicable	Write by the processor	
	Not applicable	Update is triggered at the next PWM period as soon as the update period counter has reached the value UPR	

Method 1: Manual write of duty-cycle values and manual trigger of the update

In this mode, the update of the period value, the duty-cycle values and the dead-time values must be done by writing in their respective update registers with the processor (respectively PWM_CPRDUPDx, PWM_CDTYUPDx and PWM_DTUPDx).

To trigger the update, the user must use the bit UPDULOCK in the PWM_SCUC register which allows to update synchronously (at the same PWM period) the synchronous channels:

- If the bit UPDULOCK is set to ‘1’, the update is done at the next PWM period of the synchronous channels.
- If the UPDULOCK bit is not set to ‘1’, the update is locked and cannot be performed.

After writing the UPDULOCK bit to ‘1’, it is held at this value until the update occurs, then it is read 0.

Sequence for Method 1:

1. Select the manual write of duty-cycle values and the manual update by setting the UPDM field to ‘0’ in the PWM_SCM register
2. Define the synchronous channels by the SYNCx bits in the PWM_SCM register.
3. Enable the synchronous channels by writing CHID0 in the PWM_ENA register.
4. If an update of the period value and/or the duty-cycle values and/or the dead-time values is required, write registers that need to be updated (PWM_CPRDUPDx, PWM_CDTYUPDx and PWM_DTUPDx).
5. Set UPDULOCK to ‘1’ in PWM_SCUC.
6. The update of the registers will occur at the beginning of the next PWM period. When the UPDULOCK bit is reset, go to Step 4. for new values.

- **FREERUN: Free Run Mode**

Value	Name	Description
0	OFF	Normal Mode
1	ON	Free Run Mode: Never wait for any trigger.

- **PRESCAL: Prescaler Rate Selection**

PRESCAL = ($f_{peripheral\ clock}$ / ($2 \times f_{ADCCLK}$)) – 1.

- **STARTUP: Startup Time**

Value	Name	Description
0	SUT0	0 periods of ADCCLK
1	SUT8	8 periods of ADCCLK
2	SUT16	16 periods of ADCCLK
3	SUT24	24 periods of ADCCLK
4	SUT64	64 periods of ADCCLK
5	SUT80	80 periods of ADCCLK
6	SUT96	96 periods of ADCCLK
7	SUT112	112 periods of ADCCLK
8	SUT512	512 periods of ADCCLK
9	SUT576	576 periods of ADCCLK
10	SUT640	640 periods of ADCCLK
11	SUT704	704 periods of ADCCLK
12	SUT768	768 periods of ADCCLK
13	SUT832	832 periods of ADCCLK
14	SUT896	896 periods of ADCCLK
15	SUT960	960 periods of ADCCLK

- **SETTLING: Analog Settling Time**

Value	Name	Description
0	AST3	3 periods of ADCCLK
1	AST5	5 periods of ADCCLK
2	AST9	9 periods of ADCCLK
3	AST17	17 periods of ADCCLK

- **ANACH: Analog Change**

Value	Name	Description
0	NONE	No analog change on channel switching: DIFF0, GAIN0 and OFF0 are used for all channels.
1	ALLOWED	Allows different analog settings for each channel. See ADC_CGR and ADC_COR registers.

- **TRACKTIM: Tracking Time**

Tracking Time = (TRACKTIM + 1) × ADCCLK periods

42.7.3 ADC Channel Sequence 1 Register

Name: ADC_SEQR1

Address: 0x40038008

Access: Read/Write

31	30	29	28	27	26	25	24
USCH8				USCH7			
23	22	21	20	19	18	17	16
USCH6				USCH5			
15	14	13	12	11	10	9	8
USCH4				USCH3			
7	6	5	4	3	2	1	0
USCH2				USCH1			

This register can only be written if the WPEN bit is cleared in the ADC Write Protection Mode Register.

- **USCHx: User Sequence Number x**

The sequence number x (USCHx) can be programmed by the channel number CHy where y is the value written in this field. The allowed range is 0 up to 15, thus only the sequencer from CH0 to CH15 can be used.

This register activates only if the USEQ field in ADC_MR field is set to ‘1’.

Any USCHx field is processed only if the CHx field in ADC_CHSR reads logical ‘1’, else any value written in USCHx does not add the corresponding channel in the conversion sequence.

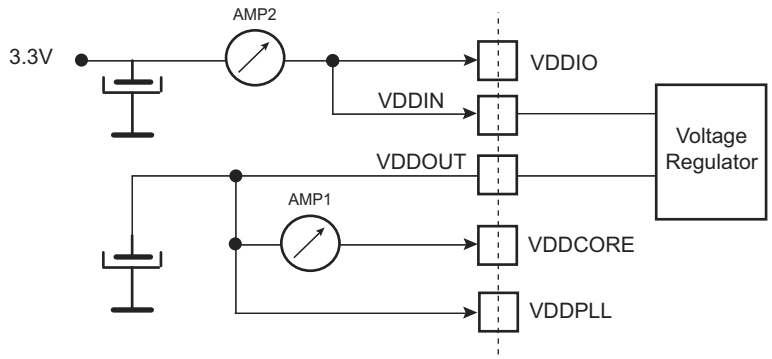
Configuring the same value in different fields leads to multiple samples of the same channel during the conversion sequence. This can be done consecutively, or not, according to user needs.

When configuring consecutive fields with the same value, the associated channel is sampled as many time as the number of consecutive values, this part of the conversion sequence being triggered by a unique event.

44.4.2 Sleep and Wait Mode Current Consumption

The Wait mode and Sleep mode configuration and measurements are defined below.

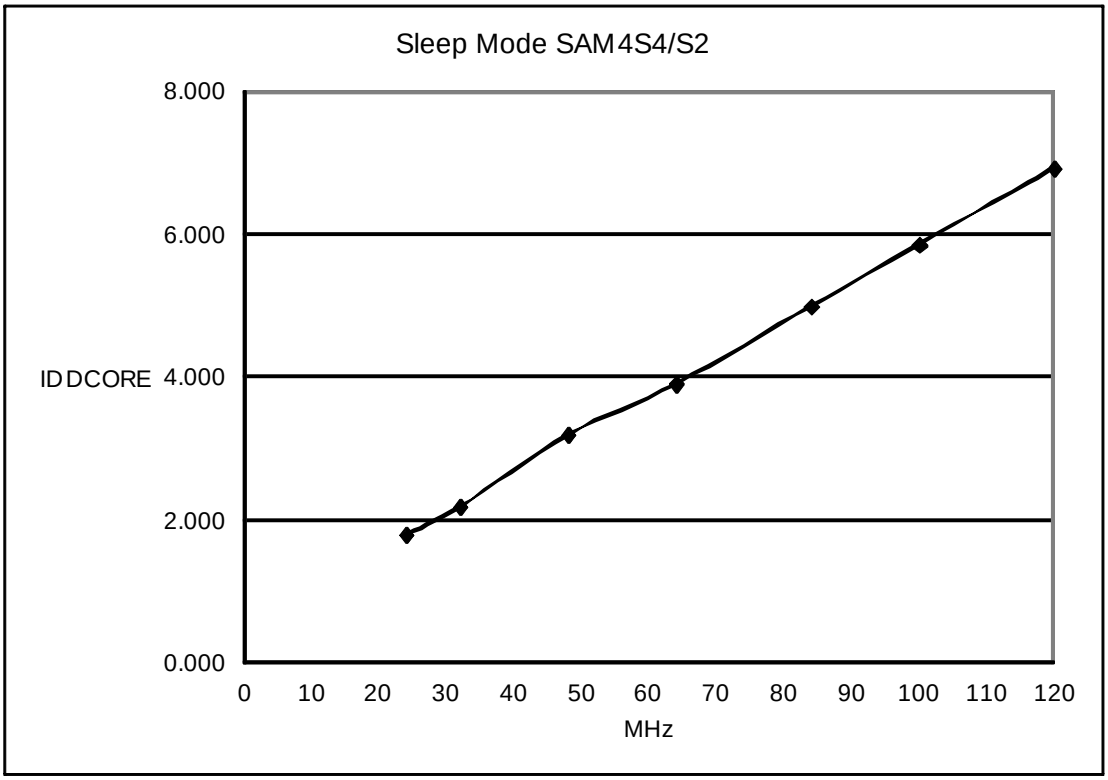
Figure 44-5. Measurement Setup for Sleep Mode



44.4.2.1 Sleep Mode

- Core clock off
- VDDIO = VDDIN = 3.3V
- Master clock (MCK) running at various frequencies with PLLA or the fast RC oscillator
- Fast start-up through pins WKUP0–15
- Current measurement as shown in Figure 44-5
- All peripheral clocks deactivated
- T_A = 25°C

Figure 44-6. SAM4S4/2 Current Consumption in Sleep Mode (AMP1) vs Master Clock Ranges (refer to Table 44-12)

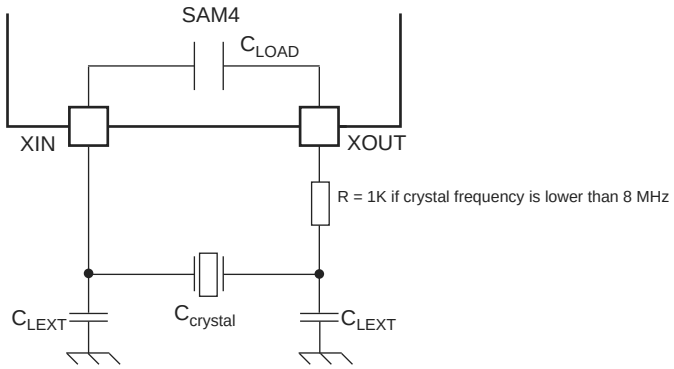


44.5.6 3 to 20 MHz Crystal Oscillator Characteristics

Table 44-31. 3 to 20 MHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Operating Frequency	Normal mode with crystal	3	16	20	MHz
	Duty Cycle		40	50	60	%
t_{START}	Startup Time	3 MHz, C_{SHUNT} = 3 pF 8 MHz, C_{SHUNT} = 7 pF 16 MHz, C_{SHUNT} = 7 pF with C_m = 8 fF 16 MHz, C_{SHUNT} = 7 pF with C_m = 1.6 fF 20 MHz, C_{SHUNT} = 7 pF	–	–	14.5 4 1.4 2.5 1	ms
I_{DDON}	Current Consumption (on VDDIO)	3 MHz 8 MHz 16 MHz 20 MHz	–	230 300 390 450	350 400 470 560	µA
P_{ON}	Drive Level	3 MHz 8 MHz 16 MHz, 20 MHz	–	–	15 30 50	µW
R_f	Internal Resistor	Between XIN and XOUT	–	0.5	–	MΩ
C_{LEXT}	Maximum External Capacitor on XIN and XOUT		–	–	17	pF
$C_{crystal}$	Allowed Crystal Capacitance Load	From crystal specification	12.5	–	17.5	pF
C_{LOAD}	Internal Equivalent Load Capacitance	Integrated load capacitance (XIN and XOUT in series)	7.5	9.5	10.5	pF

Figure 44-15. 3 to 20 MHz Crystal Oscillator Schematic



$C_{LEXT} = 2 \times (C_{crystal} - C_{LOAD} - C_{PCB})$.

Where C_{PCB} is the capacitance of the printed circuit board (PCB) track layout from the crystal to the SAM4 pin.

Table 49-5. SAM4S Datasheet Rev. 11100G Revision History

Doc. Date	Changes
27-May-14	Table 3-1 ”Signal Description List”: WKUP[15:0] voltage reference type added.
	In Figure 5-4 “Backup Battery”, modified ADC, DAC, Analog Comparator Supply from 2.0V to 2.4V
	Modified Section 6.5 “ERASE Pin”.
	Modified bullet list on use of erase commands depending on sector size in Section 8.1.3.1 “Flash Overview”
	Modified Section 8.1.3.5 “Security Bit”, Section 8.1.3.11 “GPNVM Bits” and Section 8.1.4 “Boot Strategies”.
	Section 24. “Boot Program” Section 24.5.4 “In Application Programming (IAP) Feature”: 5th sentence: added “...the EFC number...”
	Section 29. “Power Management Controller (PMC)” Section 29.17.9 “PMC Clock Generator PLLA Register”: Min value for bit MULA corrected to 4 from 7. Section 29.17.10 “PMC Clock Generator PLLB Register”: Min value for bit MULB corrected to 4 from 1.
	Section 44. “Electrical Characteristics” Added Table 44-24 ”Typical Power Consumption on VDDCORE (VDDIO = 3.3V, TA = 25°C)”. Table 44-73 ”AC Flash Characteristics”: Added parameter Erase Pin Assertion Time.
	Section 48. “Errata” Added Section Issue: and Section Issue: “Incorrect Flash Read May Occur Depending on VDDIO Voltage and Flash Wait State”.

Table 49-10. SAM4S Datasheet Rev. 11100B 31-Jul-12 Revision History (Continued)

Doc. Rev. 11100B	Comments	Change Request Ref.
	PMC	
	Added a note in Section 29.17.7 “PMC Clock Generator Main Oscillator Register” on page 528.	7848
	Max MULA/MULB value changed from 2047 to 62 in Section 29.17.9 “PMC Clock Generator PLLA Register” on page 531 and Section 29.17.10 “PMC Clock Generator PLLB Register” on page 532.	8064
	Step 5 in Section 28.2.13 “Programming Sequence” on page 463: Master Clock option added in CSS field.	8170
	Third paragraph added in Section 28.2.12 “Main Crystal Clock Failure Detector” on page 462. WAITMODE bit added in Section 29.17.7 “PMC Clock Generator Main Oscillator Register” on page 528.	8208
	CHIPID	
	Table 30-1 on page 552 modified.	rfo
	TC	
	Changed TIOA1 in TIOB1 in Section 37.6.14.1 “Description” on page 860 and Section 37.6.14.4 “Position and Rotation Measurement” on page 865.	8101
	PWM	
	Font size enlarged in Figure 39-14 on page 964.	7910
	“CMPS” replaced with “CMPM” in whole document.	8021
	ADC	
	EOCAL pin and description added in Section 42.7.12 “ADC Interrupt Status Register” on page 1106.	rfo
	PDC register row added in Section 42.7 “Analog-to-Digital Converter (ADC) User Interface” on page 1092.	7969
	Added comment in Section 42.7.15 “ADC Compare Window Register” on page 1109.	8045
	Features added in Section 42.2 “Embedded Characteristics” on page 1077.	8088
	Comments added, and removed “offset” in Section 42.6.11 “Automatic Calibration” on page 1090.	8133
	Electrical Characteristics	
	Whole chapter updated. In tables, values updated, and missing values added.	8085, 8245
	Comment for flash erasing added in Section 44.12.9 “Embedded Flash Characteristics” on page 1199.	8223
	Updated conditions for $V_{LINE-TR}$ and $V_{LOAD-TR}$ in Table 44-4 on page 1143.	rfo
	Removed the “ADVREF Current” row from Table 43-30 on page 1059.	rfo
	Updated the “Offset Error” parameter description in Table 43-32 on page 1061.	
	Updated the $T_{ACCURACY}$ parameter description in Table 44-6 on page 1144. Updated the temperature sensor description in Section 44.11 “Temperature Sensor” on page 1180 and the slope accuracy parameter data in Table 44-60 on page 1180.	rfo
	Mechanical Characteristics	
	48 pins packages (SAM4S16A and SAM4S8A devices) removed.	8100
	100-ball VFBGA package drawing added in Figure 45-3 on page 1203.	rfo
	Ordering Information	
	Table 47-1 on page 1216 completed with new devices and reordered.	rfo
	Errata	rfo
	Removed the Flash Memory section.	
	Removed the Errata section and added references for two separate errata documents in Section 47. “Ordering Information” on page 1216.	rfo
	Specified the preliminary status of the datasheet.	rfo