What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	46
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2124fbd64-01-15

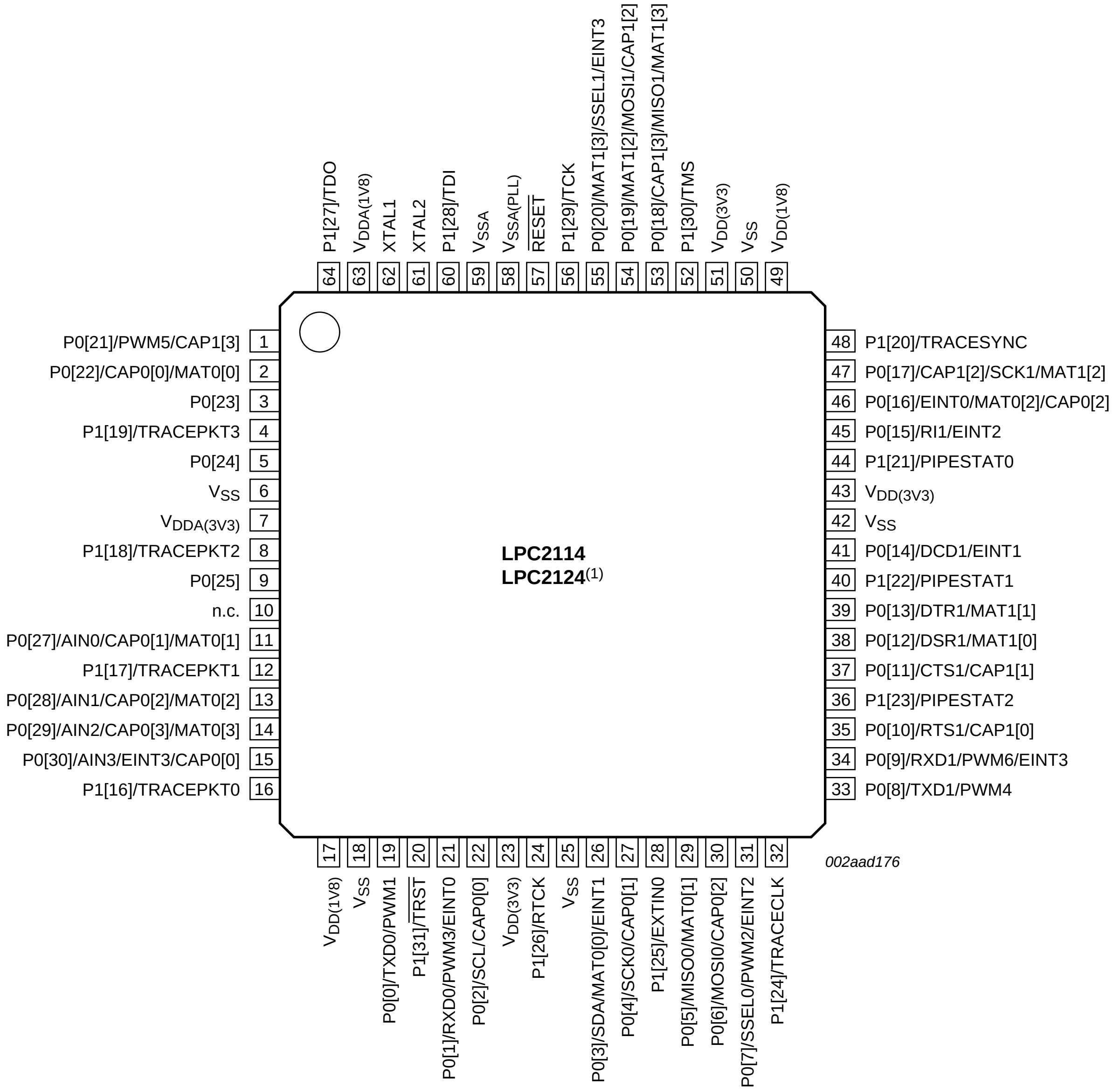
3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Fast GPIO/SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2114FBD64/01	128 kB	16 kB	yes	–40 °C to +85 °C
LPC2124FBD64/01	256 kB	16 kB	yes	–40 °C to +85 °C

5. Pinning information

5.1 Pinning



(1) Pin configuration is identical for devices with and without the /00 and /01 suffixes.

Fig 2. Pin configuration

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/PWM1	19	O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0[1]/RXD0/PWM3/EINT0	21	I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input
P0[2]/SCL/CAP0[0]	22	I/O	**SCL —** I^{2}C-bus clock input/output. Open-drain output (for I^{2}C-bus compliance).
		I	**CAP0[0] —** Capture input for Timer 0, channel 0.
P0[3]/SDA/MAT0[0]/EINT1	26	I/O	**SDA —** I^{2}C-bus data input/output. Open-drain output (for I^{2}C-bus compliance).
		O	**MAT0[0] —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0[4]/SCK0/CAP0[1]	27	I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0[1] —** Capture input for Timer 0, channel 1.
P0[5]/MISO0/MAT0[1]	29	I/O	**MISO0 —** Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0[1] —** Match output for Timer 0, channel 1.
P0[6]/MOSI0/CAP0[2]	30	I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0[2] —** Capture input for Timer 0, channel 2.
P0[7]/SSEL0/PWM2/EINT2	31	I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.
P0[8]/TXD1/PWM4	33	O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
P0[9]/RXD1/PWM6/EINT3	34	I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0[10]/RTS1/CAP1[0]	35	O	**RTS1 —** Request to Send output for UART1.
		I	**CAP1[0] —** Capture input for Timer 1, channel 0.
P0[11]/CTS1/CAP1[1]	37	I	**CTS1 —** Clear to Send input for UART1.
		I	**CAP1[1] —** Capture input for Timer 1, channel 1.
P0[12]/DSR1/MAT1[0]	38	I	**DSR1 —** Data Set Ready input for UART1.
		O	**MAT1[0] —** Match output for Timer 1, channel 0.
P0[13]/DTR1/MAT1[1]	39	O	**DTR1 —** Data Terminal Ready output for UART1.
		O	**MAT1[1] —** Match output for Timer 1, channel 1.
P0[14]/DCD1/EINT1	41	I	**DCD1 —** Data Carrier Detect input for UART1.
		I	**EINT1 —** External interrupt 1 input. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip bootloader to take control of the part after reset.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P1[16]/ TRACEPKT0	16	O	Trace Packet, bit 0. Standard I/O port with internal pull-up.
P1[17]/ TRACEPKT1	12	O	Trace Packet, bit 1. Standard I/O port with internal pull-up.
P1[18]/ TRACEPKT2	8	O	Trace Packet, bit 2. Standard I/O port with internal pull-up.
P1[19]/ TRACEPKT3	4	O	Trace Packet, bit 3. Standard I/O port with internal pull-up.
P1[20]/ TRACESYNC	48	O	Trace Synchronization. Standard I/O port with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[25:16] to operate as Trace port after reset.
P1[21]/ PIPESTAT0	44	O	Pipeline Status, bit 0. Standard I/O port with internal pull-up.
P1[22]/ PIPESTAT1	40	O	Pipeline Status, bit 1. Standard I/O port with internal pull-up.
P1[23]/ PIPESTAT2	36	O	Pipeline Status, bit 2. Standard I/O port with internal pull-up.
P1[24]/ TRACECLK	32	O	Trace Clock. Standard I/O port with internal pull-up.
P1[25]/EXTIN0	28	I	External Trigger Input. Standard I/O with internal pull-up.
P1[26]/RTCK	24	I/O	Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW, enables pins P1[31:26] to operate as Debug port after reset.
P1[27]/TDO	64	O	Test Data out for JTAG interface.
P1[28]/TDI	60	I	Test Data in for JTAG interface.
P1[29]/TCK	56	I	Test Clock for JTAG interface. This clock must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1[30]/TMS	52	I	Test Mode Select for JTAG interface.
P1[31]/$\overline{\text{TRST}}$	20	I	Test Reset for JTAG interface.
n.c.	10		pin not connected.
$\overline{\text{RESET}}$	57	I	external reset input; a LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62	I	input to the oscillator circuit and internal clock generator circuits.
XTAL2	61	O	output from the oscillator amplifier.
V_{SS}	6, 18, 25, 42, 50	I	ground: 0 V reference.
V_{SSA}	59	I	analog ground; 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{SSA(PLL)}$	58	I	PLL analog ground; 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
$V_{DD(1V8)}$	17, 49	I	1.8 V core power supply; this is the power supply voltage for internal circuitry.

6. Functional description

Details of the LPC2114/2124 systems and peripheral functions are described in the following sections.

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set’s 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM’s performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

6.2 On-chip flash program memory

The LPC2114/2124 incorporate a 128 kB and 256 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. When on-chip bootloader is used, 120 kB and 248 kB of flash memory is available for user code.

The LPC2114/2124 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data retention.

On-chip bootloader (as of revision 1.60) provides Code Read Protection (CRP) for the LPC2114/2124 on-chip flash memory. When the CRP is enabled, the JTAG debug port and ISP commands accessing either the on-chip RAM or flash memory are disabled.

Table 4. Interrupt sources *…continued*

Block	Flag(s)	VIC channel #
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
ADC	ADC	18

[1] SSP interface available on LPC2114/01 and LPC2124/01 only.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 General purpose parallel I/O (GPIO) and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the parallel I/O registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.7.2 Features added with the Fast GPIO set of registers available on LPC2114/2124/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.8 10-bit ADC

The LPC2114/2124 each contain a single 10-bit successive approximation analog to digital converter with four multiplexed channels.

the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^{2}C-bus is a multi-master bus; it can be controlled by more than one bus master connected to it.

The I^{2}C-bus implemented in LPC2114/2124 supports a bit rate up to 400 kbit/s (Fast I^{2}C-bus).

6.10.1 Features

- Standard I^{2}C-bus compliant interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^{2}C-bus may be used for test and diagnostic purposes.

6.11 SPI serial I/O controller

The LPC2114/2124 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.11.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of $\frac{1}{8}$ of the input clock rate.

6.11.2 Features available in LPC2114/2124/01 only

- Eight to 16 bits per frame.
- When the SPI interface is used in Master mode, the SSELn pin is not needed (can be used for a different function).

- Match register updates are synchronized with pulse outputs to prevent generation of erroneous pulses. Software must ‘release’ new match values before they can become effective.
- May be used as a standard timer if the PWM mode is not enabled.
- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.

6.17 System control

6.17.1 Crystal oscillator

The oscillator supports crystals in the range of 1 MHz to 30 MHz. The oscillator output frequency is called f_{osc} and the ARM processor clock frequency is referred to as CCLK for purposes of rate equations, etc. f_{osc} and CCLK are the same value unless the PLL is running and connected. Refer to Section 6.17.2 “PLL” for additional information.

6.17.2 PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up into the range of 10 MHz to 60 MHz with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32 (in practice, the multiplier value cannot be higher than 6 on this family of microcontrollers due to the upper frequency limit of the CPU). The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip Reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to Lock, then connect to the PLL as a clock source. The PLL settling time is 100 μs.

6.17.3 Reset and wake-up timer

Reset has two sources on the LPC2114/2124: the $\overline{\text{RESET}}$ pin and Watchdog Reset. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin with an additional glitch filter. Assertion of chip Reset by any source starts the Wake-up Timer (see Wake-up Timer description below), causing the internal chip reset to remain asserted until the external Reset is de-asserted, the oscillator is running, a fixed number of clocks have passed, and the on-chip flash controller has completed its initialization.

When the internal Reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The wake-up timer ensures that the oscillator and other analog functions required for chip operation are fully functional before the processor is allowed to execute instructions. This is important at power on, all types of Reset, and whenever any of the aforementioned functions are turned off for any reason. Since the oscillator and other functions are turned off during Power-down mode, any wake-up of the processor from Power-down mode makes use of the Wake-up Timer.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.17.4 Code security (Code Read Protection - CRP)

This feature of the LPC2114/2124/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user’s application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

Remark: Devices without the suffix /00 or /01 have only a security level equivalent to CRP2 available.

6.17.5 External interrupt inputs

The LPC2114/2124 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.17.6 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

6.17.7 Power control

The LPC2114/2124 support two reduced power modes: Idle mode and Power-down mode. In Idle mode, execution of instructions is suspended until either a Reset or interrupt occurs. Peripheral functions continue operation during Idle mode and may generate interrupts to cause the processor to resume execution. Idle mode eliminates power used by the processor itself, memory systems and related controllers, and internal buses.

In Power-down mode, the oscillator is shut down and the chip receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Power-down mode and the logic levels of chip output pins remain static. The Power-down mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Power-down mode reduces chip power consumption to nearly zero.

A Power Control for Peripherals feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings.

6.17.8 APB bus

The APB divider determines the relationship between the processor clock (CCLK) and the clock used by peripheral devices (PCLK). The APB divider serves two purposes. The first is to provide peripherals with the desired PCLK via APB bus so that they can operate at the speed chosen for the ARM processor. In order to achieve this, the APB bus may be slowed down to $\frac{1}{2}$ to $\frac{1}{4}$ of the processor clock rate. Because the APB bus must work properly at power-up (and its timing cannot be altered if it does not work since the APB divider control registers reside on the APB bus), the default condition at reset is for the APB bus to run at $\frac{1}{4}$ of the processor clock rate. The second purpose of the APB divider is to allow power savings when an application does not require any peripherals to run at the full processor rate. Because the APB divider is connected to the PLL output, the PLL remains active (if it was running) during Idle mode.

6.18 Emulation and debugging

The LPC2114/2124 support emulation and debugging via a JTAG serial port. A trace port allows tracing program execution. Debugging and trace functions are multiplexed only with GPIOs on Port 1. This means that all communication, timer and interface peripherals residing on Port 0 are available during the development and debugging phase as they are when the application is run in the embedded system itself.

6.18.1 EmbeddedICE

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol convertor. EmbeddedICE protocol convertor converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

The ARM core has a Debug Communication Channel function built-in. The debug communication channel allows a program running on the target to communicate with the host debugger or another separate host without stopping the program flow or even entering the debug state. The debug communication channel is accessed as a co-processor 14 by the program running on the ARM7TDMI-S core. The debug communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.18.2 Embedded trace

Since the LPC2114/2124 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The ETM provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.18.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2114/2124 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	–0.5	+2.5	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	–0.5	+3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			–0.5	+4.6	V
V_{IA}	analog input voltage			–0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins	[4][5]	–0.5	+6.0	V
		other I/O pins	[4][6]	–0.5	$V_{DD(3V3)}$ + 0.5	V
I_{DD}	supply current		[7][8]	-	100	mA
I_{SS}	ground current		[8][9]	-	100	mA
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature		[10]	–65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[11]			
		all pins		–2000	+2000	V
		machine model	[12]			
		all pins		–200	+200	V

[1] The following applies to Table 5:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] Only valid when the $V_{DD(3V3)}$ supply voltage is present.

[6] Not to exceed 4.6 V.

[7] Per supply pin.

[8] The peak current is limited to 25 times the corresponding maximum current.

[9] Per ground pin.

[10] Dependent on package type.

[11] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[12] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH coil and a 10 Ω series resistor.

8. Static characteristics

Table 6. Static characteristics

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)	[2]	1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	[3]	3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		2.5	3.3	3.6	V
Standard port pins, $\overline{\text{RESET}}$, RTCK						
I_{IL}	LOW-state input current	V_I = 0 V; no pull-up	-	-	3	μA
I_{IH}	HIGH-state input current	$V_I = V_{DD(3V3)}$; no pull-down	-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(3V3)}$; no pull-up/down	-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; T_j < 125 °C	100	-	-	mA
V_I	input voltage	[4][5][6]	0	-	5.5	V
V_O	output voltage	output active	0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-state output voltage	I_{OH} = −4 mA [7]	$V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 4 mA [7]	-	-	0.4	V
I_{OH}	HIGH-state output current	$V_{OH} = V_{DD(3V3)} - 0.4$ V [7]	−4	-	-	mA
I_{OL}	LOW-state output current	V_{OL} = 0.4 V [7]	4	-	-	mA
I_{OHS}	HIGH-state short-circuit output current	V_{OH} = 0 V [8]	-	-	−45	mA
I_{OLS}	LOW-state short-circuit output current	$V_{OL} = V_{DD(3V3)}$ [8]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V [9]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V [10]	−15	−50	−85	μA
		$V_{DD(3V3)} < V_I < 5$ V [9]	0	0	0	μA

Table 6. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Power consumption LPC2114, LPC2114/00, LPC2124, LPC2124/00						
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run	-	60	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C	-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C	-	110	500	µA
Power consumption LPC2114/01 and LPC2124/01						
$I_{DD(act)}$	active mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; code `while(1){}` executed from flash; all peripherals enabled via PCONP[11] register but not configured to run	-	40	-	mA
$I_{DD(idle)}$	Idle mode supply current	$V_{DD(1V8)}$ = 1.8 V; CCLK = 60 MHz; T_{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP[11] register but not configured to run	-	6.5	-	mA
$I_{DD(pd)}$	Power-down mode supply current	$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 25 °C	-	10	-	µA
		$V_{DD(1V8)}$ = 1.8 V; T_{amb} = 85 °C	-	110	500	µA
I^{2}C-bus pins						
V_{IH}	HIGH-state input voltage		$0.7V_{DD(3V3)}$	-	-	V
V_{IL}	LOW-state input voltage		-	-	$0.3V_{DD(3V3)}$	V
V_{hys}	hysteresis voltage		-	$0.05V_{DD(3V3)}$	-	V
V_{OL}	LOW-state output voltage	I_{OLS} = 3 mA [7]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD(3V3)}$ [12]	-	2	4	µA
		V_I = 5 V	-	10	22	µA

Table 7. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V unless otherwise specified; T_{amb} = −40 °C to +85 °C unless otherwise specified. ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	-	±2	LSB
E_O	offset error		[1][5]	-	-	±3	LSB
E_G	gain error		[1][6]	-	-	±0.5	%
E_T	absolute error		[1][7]	-	-	±4	LSB

[1] Conditions: V_{SSA} = 0 V, V_{DDA} = 3.3 V.

[2] The ADC is monotonic, there are no missing codes.

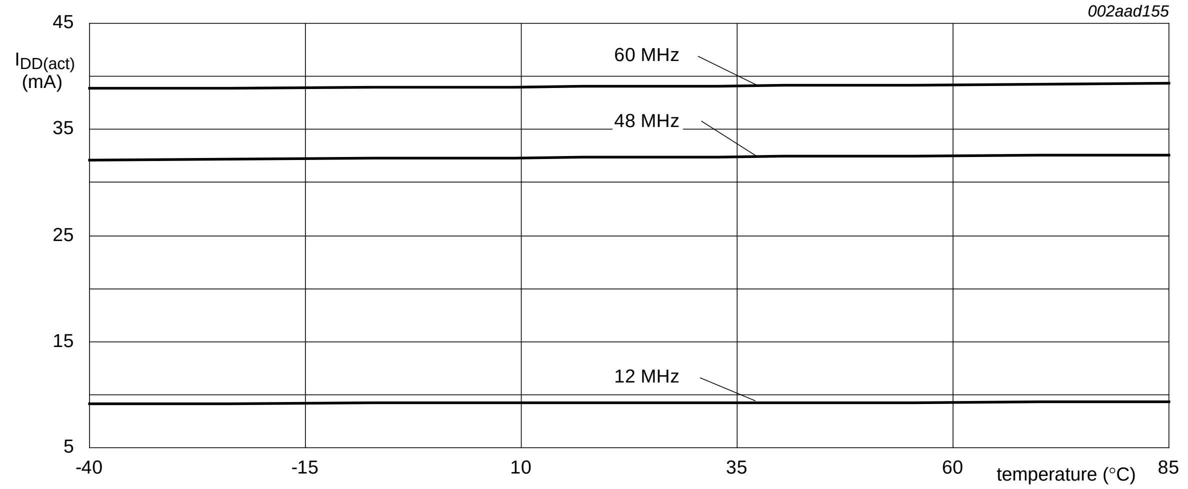
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 4.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 4.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 4.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 4.

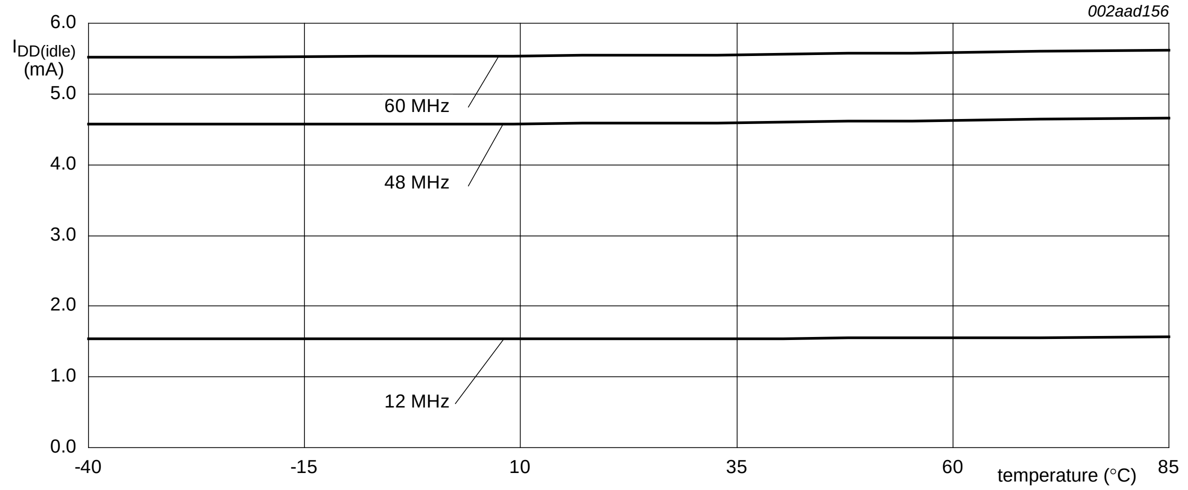
[7] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 4.



Test conditions: Active mode entered executing code from on-chip flash; PCLK = CCLK⁄4;

core voltage 1.8 V; all peripherals disabled.

Fig 11. Typical LPC2114/01 and LPC2124/01 $I_{DD(act)}$ measured at different temperatures



Test conditions: Idle mode entered executing code from on-chip flash; PCLK = CCLK⁄4;

core voltage 1.8 V; all peripherals disabled.

Fig 12. Typical LPC2114/01 and LPC2124/01 $I_{DD(idle)}$ measured at different temperatures

9.1 Timing

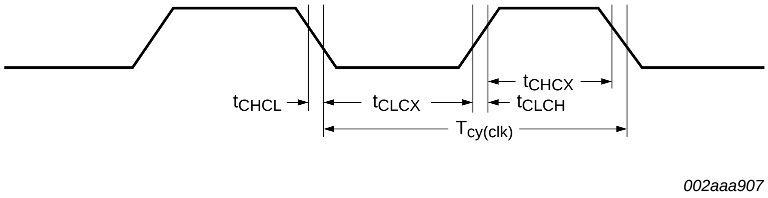


Fig 14. External clock timing (with an amplitude of at least $V_{i(RMS)}$ = 200 mV)

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DCC	Debug Communications Channel
FIFO	First In, First Out
GPIO	General Purpose Input/Output
I/O	Input/Output
JTAG	Joint Test Action Group
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SSI	Synchronous Serial Interface
SSP	Synchronous Serial Port
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receiver/Transmitter

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term ‘short data sheet’ is explained in section “Definitions”.

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15. Contents

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Date of release: 10 June 2011

Document identifier: LPC2114_2124