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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	46
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2124fbd64-151

- 128/256 kB on-chip flash program memory. 128-bit wide interface/accelerator enables high speed 60 MHz operation.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash programming takes 1 ms per 512 B line. Single sector or full chip erase takes 400 ms.
- EmbeddedICE-RT interface enables breakpoints and watch points. Interrupt service routines can continue to execute whilst the foreground task is debugged with the on-chip RealMonitor software.
- Embedded Trace Macrocell (ETM) enables non-intrusive high speed real-time tracing of instruction execution.
- Four-channel 10-bit ADC with conversion time as low as 2.44 μ s.
- Two 32-bit timers (with four capture and four compare channels), PWM unit (six outputs), Real-Time Clock (RTC) and watchdog.
- Multiple serial interfaces including two UARTs (16C550), Fast I²C-bus (400 kbit/s) and two SPIs.
- 60 MHz maximum CPU clock available from programmable on-chip Phase-Locked Loop with settling time of 100 μ s.
- Vectored Interrupt Controller with configurable priorities and vector addresses.
- Up to forty-six 5 V tolerant general purpose I/O pins. Up to nine edge or level sensitive external interrupt pins available.
- On-chip crystal oscillator with an operating range of 1 MHz to 30 MHz.
- Two low power modes, Idle and Power-down.
- Processor wake-up from Power-down mode via external interrupt.
- Individual enable/disable of peripheral functions for power optimization.
- Dual power supply:
 - ◆ CPU operating voltage range of 1.65 V to 1.95 V (1.8 V \pm 0.15 V).
 - ◆ I/O power supply range of 3.0 V to 3.6 V (3.3 V \pm 10 %) with 5 V tolerant I/O pads. 16/32-bit ARM7TDMI-S processor.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2114FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 \times 10 \times 1.4 mm	SOT314-2
LPC2124FBD64/01	LQFP64	plastic low profile quad flat package; 64 leads; body 10 \times 10 \times 1.4 mm	SOT314-2

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Fast GPIO/SSP/ Enhanced UART, ADC, Timer	Temperature range
LPC2114FBD64/01	128 kB	16 kB	yes	–40 °C to +85 °C
LPC2124FBD64/01	256 kB	16 kB	yes	–40 °C to +85 °C

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0[0] to P0[31]		I/O	Port 0 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 0 pins depends upon the pin function selected via the Pin Connect Block. Pins 26 and 31 of port 0 are not available.
P0[0]/TXD0/ PWM1	19	O	TXD0 — Transmitter output for UART0.
		O	PWM1 — Pulse Width Modulator output 1.
P0[1]/RXD0/ PWM3/EINT0	21	I	RXD0 — Receiver input for UART0.
		O	PWM3 — Pulse Width Modulator output 3.
		I	EINT0 — External interrupt 0 input
P0[2]/SCL/ CAP0[0]	22	I/O	SCL — I ² C-bus clock input/output. Open-drain output (for I ² C-bus compliance).
		I	CAP0[0] — Capture input for Timer 0, channel 0.
P0[3]/SDA/ MAT0[0]/EINT1	26	I/O	SDA — I ² C-bus data input/output. Open-drain output (for I ² C-bus compliance).
		O	MAT0[0] — Match output for Timer 0, channel 0.
		I	EINT1 — External interrupt 1 input.
P0[4]/SCK0/ CAP0[1]	27	I/O	SCK0 — Serial clock for SPI0. SPI clock output from master or input to slave.
		I	CAP0[1] — Capture input for Timer 0, channel 1.
P0[5]/MISO0/ MAT0[1]	29	I/O	MISO0 — Master In Slave OUT for SPI0. Data input to SPI master or data output from SPI slave.
		O	MAT0[1] — Match output for Timer 0, channel 1.
P0[6]/MOSI0/ CAP0[2]	30	I/O	MOSI0 — Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	CAP0[2] — Capture input for Timer 0, channel 2.
P0[7]/SSEL0/ PWM2/EINT2	31	I	SSEL0 — Slave Select for SPI0. Selects the SPI interface as a slave.
		O	PWM2 — Pulse Width Modulator output 2.
		I	EINT2 — External interrupt 2 input.
P0[8]/TXD1/ PWM4	33	O	TXD1 — Transmitter output for UART1.
		O	PWM4 — Pulse Width Modulator output 4.
P0[9]/RXD1/ PWM6/EINT3	34	I	RXD1 — Receiver input for UART1.
		O	PWM6 — Pulse Width Modulator output 6.
		I	EINT3 — External interrupt 3 input.
P0[10]/RTS1/ CAP1[0]	35	O	RTS1 — Request to Send output for UART1.
		I	CAP1[0] — Capture input for Timer 1, channel 0.
P0[11]/CTS1/ CAP1[1]	37	I	CTS1 — Clear to Send input for UART1.
		I	CAP1[1] — Capture input for Timer 1, channel 1.
P0[12]/DSR1/ MAT1[0]	38	I	DSR1 — Data Set Ready input for UART1.
		O	MAT1[0] — Match output for Timer 1, channel 0.
P0[13]/DTR1/ MAT1[1]	39	O	DTR1 — Data Terminal Ready output for UART1.
		O	MAT1[1] — Match output for Timer 1, channel 1.
P0[14]/DCD1/ EINT1	41	I	DCD1 — Data Carrier Detect input for UART1.
		I	EINT1 — External interrupt 1 input.

Note: LOW on this pin while **RESET** is LOW forces on-chip bootloader to take control of the part after reset.

However, the ISP flash erase command can be executed at any time (no matter whether the CRP is on or off). Removal of CRP is achieved by erasure of full on-chip user flash. With the CRP off, full access to the chip via the JTAG and/or ISP is restored.

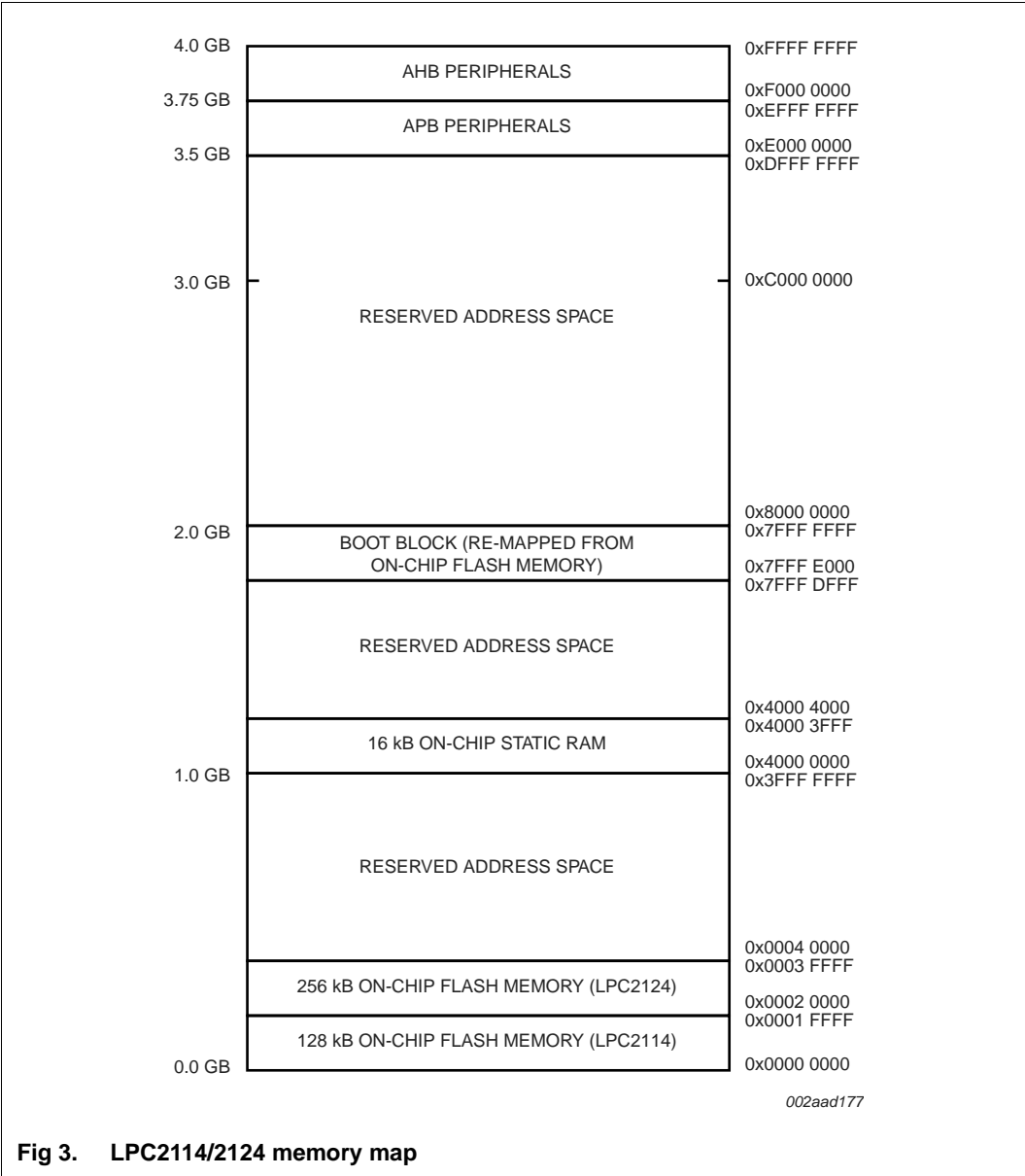
6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8 bit, 16 bit, and 32 bit. The LPC2114/2124 provide 16 kB of static RAM.

6.4 Memory map

The LPC2114/2124 memory maps incorporate several distinct regions, as shown in [Figure 3](#).

In addition, the CPU interrupt vectors may be re-mapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in [Section 6.17](#) [“System control”](#).



6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt reQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

Fast Interrupt reQuest (FIQ) has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine can simply start dealing with that device. But if more than one request is assigned to the FIQ class, the FIQ service routine can read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Table 4. Interrupt sources ...continued

Block	Flag(s)	VIC channel #
System Control	External Interrupt 0 (EINT0)	14
	External Interrupt 1 (EINT1)	15
	External Interrupt 2 (EINT2)	16
	External Interrupt 3 (EINT3)	17
ADC	ADC	18

[1] SSP interface available on LPC2114/01 and LPC2124/01 only.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

6.7 General purpose parallel I/O (GPIO) and Fast I/O

Device pins that are not connected to a specific peripheral function are controlled by the parallel I/O registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.7.2 Features added with the Fast GPIO set of registers available on LPC2114/2124/01 only

- Fast GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing, enabling port pin toggling up to 3.5 times faster than earlier LPC2000 devices.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All Fast GPIO registers are byte addressable.
- Entire port value can be written in one instruction.
- Ports are accessible via either the legacy group of registers (GPIOs) or the group of registers providing accelerated port access (Fast GPIOs).

6.8 10-bit ADC

The LPC2114/2124 each contain a single 10-bit successive approximation analog to digital converter with four multiplexed channels.

6.8.1 Features

- Measurement range of 0 V to 3 V.
- Capable of performing more than 400 000 10-bit samples per second.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or Timer Match signal.
- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.

6.8.2 ADC features available in LPC2114/2124/01 only

- Every analog input has a dedicated result register to reduce interrupt overhead.
- Every analog input can generate an interrupt once the conversion is completed.
- The ADC pads are 5 V tolerant when configured for digital I/O function(s).

6.9 UARTs

The LPC2114/2124 each contain two UARTs. In addition to standard transmit and receive data lines, the UART1 also provides a full modem control handshake interface.

6.9.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- UART1 is equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.9.2 UART features available in LPC2114/2124/01 only

Compared to previous LPC2000 microcontrollers, UARTs in LPC2114/2124/01 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 Bd with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware.

- Fractional baud rate generator enables standard baud rates such as 115200 Bd to be achieved with any crystal frequency above 2 MHz.
- Auto-bauding.
- Auto-CTS/RTS flow-control fully implemented in hardware.

6.10 I²C-bus serial I/O controller

The I²C-bus is a bidirectional bus for inter-IC control using only two wires: a serial clock line (SCL), and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g. an LCD driver or a transmitter with

the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C-bus is a multi-master bus; it can be controlled by more than one bus master connected to it.

The I²C-bus implemented in LPC2114/2124 supports a bit rate up to 400 kbit/s (Fast I²C-bus).

6.10.1 Features

- Standard I²C-bus compliant interface.
- Easy to configure as Master, Slave, or Master/Slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I²C-bus may be used for test and diagnostic purposes.

6.11 SPI serial I/O controller

The LPC2114/2124 each contain two SPIs. The SPI is a full duplex serial interface, designed to be able to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

6.11.1 Features

- Compliant with Serial Peripheral Interface (SPI) specification.
- Synchronous, Serial, Full Duplex communication.
- Combined SPI master and slave.
- Maximum data bit rate of $\frac{1}{8}$ of the input clock rate.

6.11.2 Features available in LPC2114/2124/01 only

- Eight to 16 bits per frame.
- When the SPI interface is used in Master mode, the SSELn pin is not needed (can be used for a different function).

6.12 SSP controller (LPC2114/2124/01 only)

Remark: This peripheral is available in LPC2114/2124/01 only.

The SSP is a controller capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of four to 16 bits of data flowing from the master to the slave and from the slave to the master.

While the SSP and SPI1 peripherals share the same physical pins, it is not possible to have both of these two peripherals active at the same time. The application can switch on the fly from SPI1 to SSP and back.

6.12.1 Features

- Compatible with Motorola's SPI, Texas Instrument's 4-wire SSI, and National Semiconductor's Microwire buses.
- Synchronous serial communication.
- Master or slave operation.
- 8-frame FIFOs for both transmit and receive.
- Four to 16 bits per frame.

6.13 General purpose timers

The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions at specified timer values, based on four match registers. It also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt. Multiple pins can be selected to perform a single capture or match function, providing an application with 'or' and 'and', as well as 'broadcast' functions among them.

6.13.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit Prescaler.
- Four 32-bit capture channels per timer that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Four external outputs per timer corresponding to match registers, with the following capabilities:
 - Set LOW on match.
 - Set HIGH on match.
 - Toggle on match.
 - Do nothing on match.

6.16 Pulse width modulator

The PWM is based on the standard Timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2114/2124. The Timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.16.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
 - Continuous operation with optional interrupt generation on match.
 - Stop timer on match with optional interrupt generation.
 - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

The Wake-up Timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution. When power is applied to the chip, or some event caused the chip to exit Power-down mode, some time is required for the oscillator to produce a signal of sufficient amplitude to drive the clock logic. The amount of time depends on many factors, including the rate of V_{DD} ramp (in the case of power on), the type of crystal and its electrical characteristics (if a quartz crystal is used), as well as any other external circuitry (e.g. capacitors), and the characteristics of the oscillator itself under the existing ambient conditions.

6.17.4 Code security (Code Read Protection - CRP)

This feature of the LPC2114/2124/01 allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the JTAG and ISP can be restricted. When needed, CRP is invoked by programming a specific pattern into a dedicated flash location. IAP commands are not affected by the CRP.

There are three levels of the Code Read Protection.

CRP1 disables access to chip via the JTAG and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors can not be erased.

CRP2 disables access to chip via the JTAG and only allows full flash erase and update using a reduced set of the ISP commands.

Running an application with level CRP3 selected fully disables any access to chip via the JTAG pins and the ISP. This mode effectively disables ISP override using P0[14] pin, too. It is up to the user's application to provide (if needed) flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via UART0.

CAUTION



If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

Remark: Devices without the suffix /00 or /01 have only a security level equivalent to CRP2 available.

6.17.5 External interrupt inputs

The LPC2114/2124 include up to nine edge or level sensitive External Interrupt Inputs as selectable pin functions. When the pins are combined, external events can be processed as four independent interrupt signals. The External Interrupt Inputs can optionally be used to wake up the processor from Power-down mode.

6.17.6 Memory mapping control

The Memory Mapping Control alters the mapping of the interrupt vectors that appear beginning at address 0x0000 0000. Vectors may be mapped to the bottom of the on-chip flash memory, or to the on-chip static RAM. This allows code running in different memory spaces to have control of the interrupts.

communication channel allows the JTAG port to be used for sending and receiving data without affecting the normal program flow. The debug communication channel data and control registers are mapped in to addresses in the EmbeddedICE logic.

The JTAG clock (TCK) must be slower than $\frac{1}{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.

6.18.2 Embedded trace

Since the LPC2114/2124 have significant amounts of on-chip memory, it is not possible to determine how the processor core is operating simply by observing the external pins. The ETM provides real-time trace capability for deeply embedded processor cores. It outputs information about processor execution to the trace port.

The ETM is connected directly to the ARM core and not to the main AMBA system bus. It compresses the trace information and exports it through a narrow trace port. An external trace port analyzer must capture the trace information under software debugger control. Instruction trace (or PC trace) shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. Trace information generation can be controlled by selecting the trigger resource. Trigger resources include address comparators, counters and sequencers. Since trace information is compressed the software debugger requires a static image of the code being executed. Self-modifying code can not be traced because of this restriction.

6.18.3 RealMonitor

RealMonitor is a configurable software module, developed by ARM Inc., which enables real time debug. It is a lightweight debug monitor that runs in the background while users debug their foreground application. It communicates with the host using the DCC (Debug Communications Channel), which is present in the EmbeddedICE logic. The LPC2114/2124 contain a specific configuration of RealMonitor software programmed into the on-chip flash memory.

8. Static characteristics

Table 6. Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2] 1.65	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3] 3.0	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		2.5	3.3	3.6	V
Standard port pins, RESET, RTCK						
I_{IL}	LOW-state input current	$V_I = 0\text{ V}$; no pull-up	-	-	3	μA
I_{IH}	HIGH-state input current	$V_I = V_{DD(3V3)}$; no pull-down	-	-	3	μA
I_{OZ}	OFF-state output current	$V_O = 0\text{ V}$; $V_O = V_{DD(3V3)}$; no pull-up/down	-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD(3V3)}) < V_I < (1.5V_{DD(3V3)})$; $T_J < 125\text{ }^{\circ}\text{C}$	100	-	-	mA
V_I	input voltage		[4][5][6] 0	-	5.5	V
V_O	output voltage	output active	0	-	$V_{DD(3V3)}$	V
V_{IH}	HIGH-state input voltage		2.0	-	-	V
V_{IL}	LOW-state input voltage		-	-	0.8	V
V_{hys}	hysteresis voltage		0.4	-	-	V
V_{OH}	HIGH-state output voltage	$I_{OH} = -4\text{ mA}$	[7] $V_{DD(3V3)} - 0.4$	-	-	V
V_{OL}	LOW-state output voltage	$I_{OL} = 4\text{ mA}$	[7] -	-	0.4	V
I_{OH}	HIGH-state output current	$V_{OH} = V_{DD(3V3)} - 0.4\text{ V}$	[7] -4	-	-	mA
I_{OL}	LOW-state output current	$V_{OL} = 0.4\text{ V}$	[7] 4	-	-	mA
I_{OHS}	HIGH-state short-circuit output current	$V_{OH} = 0\text{ V}$	[8] -	-	-45	mA
I_{OLS}	LOW-state short-circuit output current	$V_{OL} = V_{DD(3V3)}$	[8] -	-	50	mA
I_{pd}	pull-down current	$V_I = 5\text{ V}$	[9] 10	50	150	μA
I_{pu}	pull-up current	$V_I = 0\text{ V}$	[10] -15	-50	-85	μA
		$V_{DD(3V3)} < V_I < 5\text{ V}$	[9] 0	0	0	μA

Table 6. Static characteristics ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
Power consumption LPC2114, LPC2114/00, LPC2124, LPC2124/00						
I _{DD(act)}	active mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; code while(1){} executed from flash; all peripherals enabled via PCONP ^[11] register but not configured to run	-	60	-	mA
I _{DD(pd)}	Power-down mode supply current	V _{DD(1V8)} = 1.8 V; T _{amb} = 25 °C	-	10	-	μA
		V _{DD(1V8)} = 1.8 V; T _{amb} = 85 °C	-	110	500	μA
Power consumption LPC2114/01 and LPC2124/01						
I _{DD(act)}	active mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; code while(1){} executed from flash; all peripherals enabled via PCONP ^[11] register but not configured to run	-	40	-	mA
I _{DD(idle)}	Idle mode supply current	V _{DD(1V8)} = 1.8 V; CCLK = 60 MHz; T _{amb} = 25 °C; executed from flash; all peripherals enabled via PCONP ^[11] register but not configured to run	-	6.5	-	mA
I _{DD(pd)}	Power-down mode supply current	V _{DD(1V8)} = 1.8 V; T _{amb} = 25 °C	-	10	-	μA
		V _{DD(1V8)} = 1.8 V; T _{amb} = 85 °C	-	110	500	μA
I ² C-bus pins						
V _{IH}	HIGH-state input voltage		0.7V _{DD(3V3)}	-	-	V
V _{IL}	LOW-state input voltage		-	-	0.3V _{DD(3V3)}	V
V _{hys}	hysteresis voltage		-	0.05V _{DD(3V3)}	-	V
V _{OL}	LOW-state output voltage	I _{OLS} = 3 mA	^[7] -	-	0.4	V
I _{LI}	input leakage current	V _I = V _{DD(3V3)}	^[12] -	2	4	μA
		V _I = 5 V	-	10	22	μA

Table 6. Static characteristics ...continued*T_{amb} = -40 °C to +85 °C for industrial applications, unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
Oscillator pins						
V _{i(XTAL1)}	input voltage on pin XTAL1		0	-	1.8	V
V _{o(XTAL2)}	output voltage on pin XTAL2		0	-	1.8	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Internal rail.

[3] External rail.

[4] Including voltage on outputs in 3-state mode.

[5] V_{DD(3V3)} supply voltages must be present.

[6] 3-state outputs go into 3-state mode when V_{DD(3V3)} is grounded.

[7] Accounts for 100 mV voltage drop in all supply lines.

[8] Only allowed for a short time period.

[9] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[10] Applies to P1[25:16].

[11] See the *LPC2114/2124/2212/2214 User Manual*.

[12] To V_{SS}.

Table 7. ADC static characteristics

$V_{DDA} = 2.5\text{ V to }3.6\text{ V unless otherwise specified; }T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C unless otherwise specified. ADC frequency }4.5\text{ MHz.}$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		0	-	V_{DDA}	V
C_{ia}	analog input capacitance		-	-	1	pF
E_D	differential linearity error	[1][2][3]	-	-	± 1	LSB
$E_{L(adj)}$	integral non-linearity	[1][4]	-	-	± 2	LSB
E_O	offset error	[1][5]	-	-	± 3	LSB
E_G	gain error	[1][6]	-	-	± 0.5	%
E_T	absolute error	[1][7]	-	-	± 4	LSB

[1] Conditions: $V_{SSA} = 0\text{ V}$, $V_{DDA} = 3.3\text{ V}$.

[2] The ADC is monotonic, there are no missing codes.

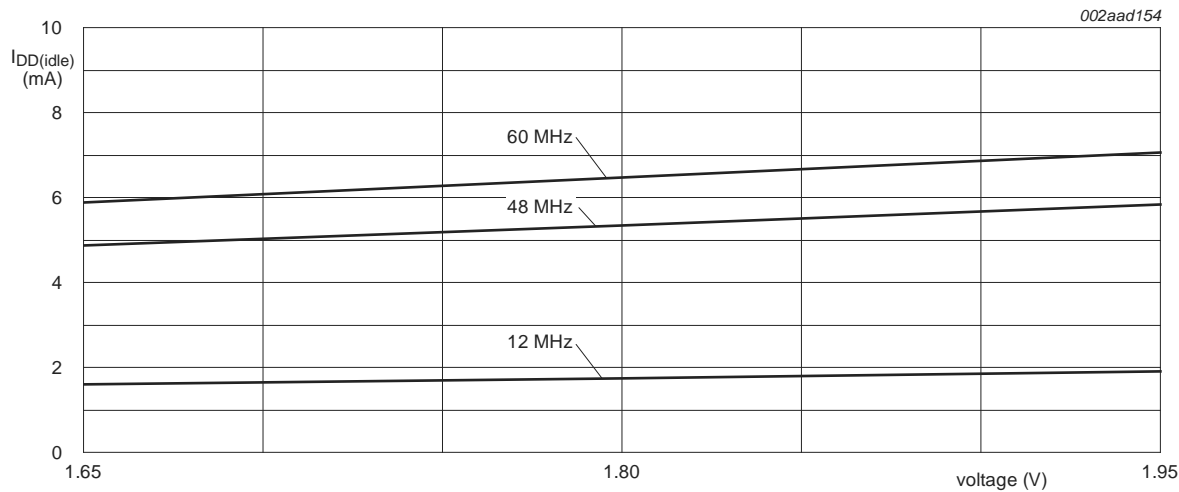
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See [Figure 4](#).

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See [Figure 4](#).

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See [Figure 4](#).

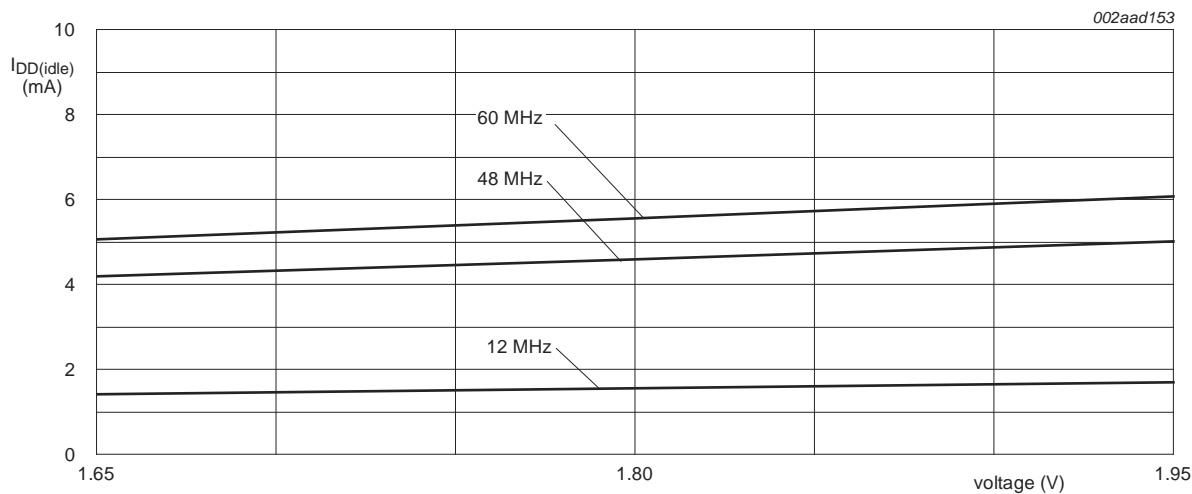
[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See [Figure 4](#).

[7] The absolute voltage error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See [Figure 4](#).



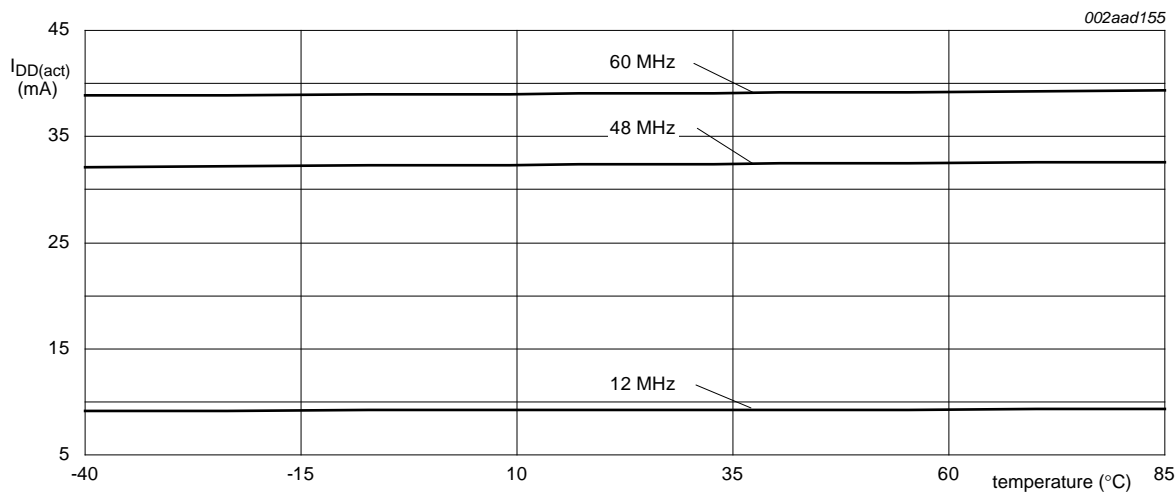
Test conditions: Idle mode entered executing code from on-chip flash; $PCLK = CCLK/4$;
 $T_{amb} = 25\text{ }^{\circ}\text{C}$; core voltage 1.8 V; all peripherals enabled.

Fig 9. Typical LPC2114/01 and LPC2124/01 $I_{DD(idle)}$ measured at different voltages



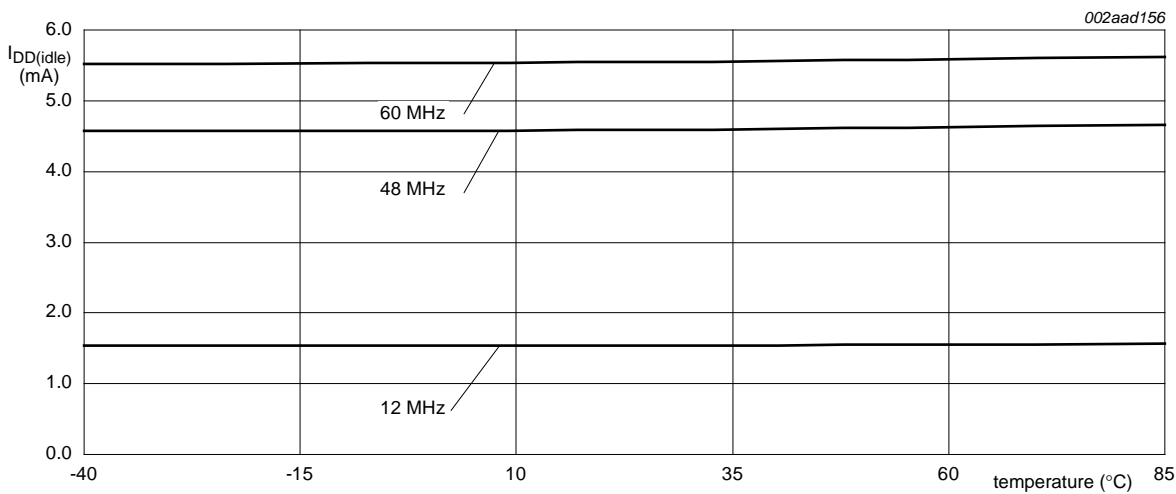
Test conditions: Idle mode entered executing code from on-chip flash; $PCLK = CCLK/4$;
Temp = 25 $^{\circ}\text{C}$; core voltage 1.8 V; all peripherals disabled.

Fig 10. Typical LPC2114/01 and LPC2124/01 $I_{DD(idle)}$ measured at different voltages



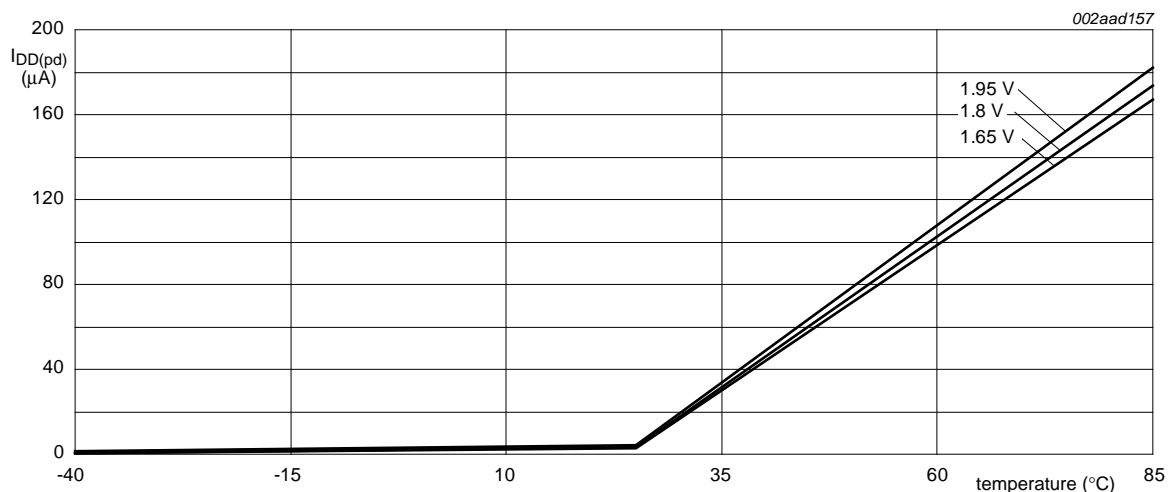
Test conditions: Active mode entered executing code from on-chip flash; $PCLK = CCLK/4$; core voltage 1.8 V; all peripherals disabled.

Fig 11. Typical LPC2114/01 and LPC2124/01 $I_{DD(act)}$ measured at different temperatures



Test conditions: Idle mode entered executing code from on-chip flash; $PCLK = CCLK/4$; core voltage 1.8 V; all peripherals disabled.

Fig 12. Typical LPC2114/01 and LPC2124/01 $I_{DD(idle)}$ measured at different temperatures



Test conditions: Power-down mode entered executing code from on-chip flash.

Fig 13. Typical LPC2114/01 and LPC2124/01 core power-down current $I_{DD(pd)}$ measured at different temperatures

Table 8. Typical LPC2114/01 and LPC2124/01 peripheral power consumption in active mode

Core voltage 1.8 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; all measurements in μA ; $PCLK = CCLK/4$.

Peripheral	CCLK = 12 MHz	CCLK = 48 MHz	CCLK = 60 MHz
Timer0	43	141	184
Timer1	46	150	180
UART0	98	320	398
UART1	103	351	421
PWM0	103	341	407
I ² C-bus	9	37	53
SPI0/1	6	27	29
RTC	16	55	78
ADC	33	128	167

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