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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	180MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, Microwire, MMC/SD, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, WDT
Number of I/O	83
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	136K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 8x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc18s37jbd144e

3.3 General description

The OTP memory contains four memory banks of 128 bits each. The first memory bank (OTP bank 0) is reserved. The other three OTP banks are programmable. In non-secure parts, OTP banks 1 and 2 are available for general-purpose data. In secure parts, OTP banks 1 and 2 are used for AES keys. OTP bank 3 contains up to two user programmable configuration words and two more words for general-purpose use.

The virgin OTP state is all zeros. A zero value can be overwritten by a one, but a one in any of the OTP bits cannot be changed.

Programming the OTP requires a higher voltage than reading. The read voltage is generated internally. The programming voltage is supplied via pin VPP. The OTP controller automatically selects the correct voltage. If the VPP pin is not connected, then the OTP cannot be programmed. An API is provided to program data into the OTP.

The AES keys in the OTP memory used by secure parts are not readable by software.

Table 8. OTP content for secure and non-secure parts

	Secure devices				Non-secure devices			
OTP bank	**Content**	**Encrypted**	**Software access**	**API**	**Content**	**Encrypted**	**Software access**	**API**
0	Reserved	-	-	-	-	-	-	-
1	AES key 1 for secure boot image	yes	no	aes_ProgramKey1	User-defined; general purpose 0	no	yes	otp_ProgGP0
2	AES key 2 for data	no	no	aes_ProgramKey2	User-defined; general purpose 1	no	yes	otp_ProgGP1
3	Word 0: Customer control data	no	yes	otp_ProgBootSrc, otp_ProgJTAGDis	Word 0: Customer control data	no	yes	otp_ProgBootSrc
3	Word 1; general purpose word 0 or USB ID	no	yes	otp_ProgGP2 or otp_ProgGP2_0 or otp_ProgUSBID	Same as for secure devices			
3	Words 2 to 3: General purpose data in words 1/2.	no	yes	otp_ProgGP2 or otp_ProgGP2_1, otp_ProgGP2_2	Same as for secure devices			

checks for the type of SPI flash device. For an SPI flash, the part boots with a 18 MHz clock. For a quad SPI flash device, the part boots with a 32 MHz clock. If the detected device is unknown, the SPIFI clock is reduced to 18 MHz.

If no header is present, it is assumed that the image is located on address 0x80000000 and is executed from there.

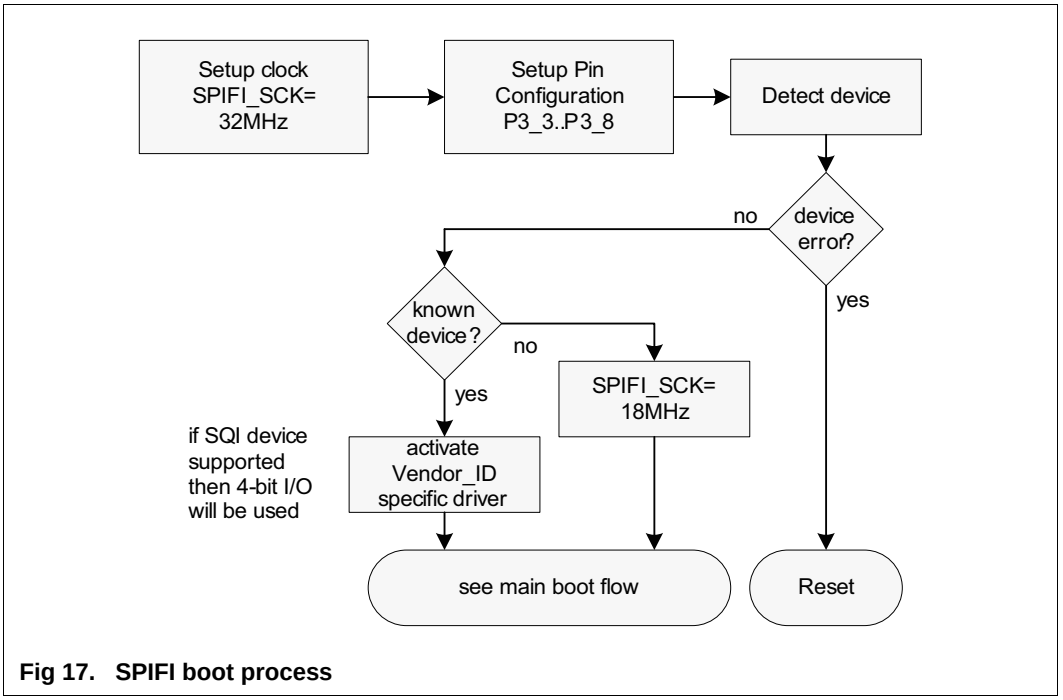


Fig 17. SPIFI boot process

4.3.6.4.1 Supported QSPI devices

Multiple QSPI devices from various vendors can be used with the SPIFI interface and the SPIFI API available on nxp.com.

LPC18xx devices support boot from flash. The boot code sets the SPIFI clock to 32 MHz at the beginning of the boot process and checks for the type of SPI flash device. If the detected device is not recognized by LPC18xx, the SPIFI clock is reduced to 18 MHz.

The devices listed in Table 19 are tested to work as boot devices for the LPC18xx and with the SPIFI API.

Remark: All QSPI devices have been tested at an operating voltage of 3.3 V.

Table 77. Level configuration register (HILO - address 0x4004 4000) bit description

Bit	Symbol	Value	Description	Reset value
13	TIM2_L		Level detect mode for combined timer output 2 event.	0
		0	Detect LOW level GIMA output 25 if bit 13 in the EDGE register is 0. Detect falling edge if bit 13 in the EDGE register is 1.	
		1	Detect HIGH level GIMA output 25 if bit 13 in the EDGE register is 0. Detect rising edge if bit 13 in the EDGE register is 1.	
14	TIM6_L		Level detect mode for combined timer output 6 event.	0
		0	Detect LOW level of GIMA output 26 if bit 14 in the EDGE register is 0. Detect falling edge if bit 14 in the EDGE register is 1.	
		1	Detect HIGH level of GIMA output 26 if bit 14 in the EDGE register is 0. Detect rising edge if bit 14 in the EDGE register is 1.	
15	QEI_L		Level detect mode for QEI event.	0
		0	Detect LOW level of the QEI interrupt if bit 15 in the EDGE register is 0. Detect falling edge if bit 15 in the EDGE register is 1.	
		1	Detect HIGH level of the QEI interrupt if bit 15 in the EDGE register is 0. Detect rising edge if bit 15 in the EDGE register is 1.	
16	TIM14_L		Level detect mode for combined timer output 14 event.	0
		0	Detect LOW level of GIMA output 27 if bit 16 in the EDGE register is 0. Detect falling edge if bit 16 in the EDGE register is 1.	
		1	Detect HIGH level of GIMA output 27 if bit 16 in the EDGE register is 0. Detect rising edge if bit 16 in the EDGE register is 1.	
18:17	-	-	Reserved.	
19	RESET_L		Level detect mode for Reset	0
		0	Detect LOW level if bit 19 in the EDGE register is 0. Detect falling edge if bit 19 in the EDGE register is 1.	
		1	Detect HIGH level if bit 19 in the EDGE register is 0. Detect rising edge if bit 19 in the EDGE register is 1.	
20	BODRESET_L		Level detect mode for BOD Reset	0
		0	Detect LOW level if bit 20 in the EDGE register is 0. Detect falling edge if bit 20 in the EDGE register is 1.	
		1	Detect HIGH level if bit 20 in the EDGE register is 0. Detect rising edge if bit 20 in the EDGE register is 1.	
21	DPDRESET_L		Level detect mode for Deep power-down Reset	0
		0	Detect LOW level if bit 21 in the EDGE register is 0. Detect falling edge if bit 21 in the EDGE register is 1.	
		1	Detect HIGH level if bit 21 in the EDGE register is 0. Detect rising edge if bit 21 in the EDGE register is 1.	
31:22	-	-	Reserved.	

Table 157. Reset control register 1 (RESET_CTRL1, address 0x4005 3104) bit description

…continued

Bit	Symbol	Description	Reset value	Access
6	MOTOCONPWM_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
7	QEI_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
8	ADC0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
9	ADC1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
10	DAC_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
11	-	Reserved	-	-
12	UART0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
13	UART1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
14	UART2_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
15	UART3_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
16	I2C0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
17	I2C1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
18	SSP0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
19	SSP1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
20	I2S_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
21	SPIFI_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
22	CAN1_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
23	CAN0_RST	Writing a one activates the reset. This bit is automatically cleared to 0 after one clock cycle.	0	W
24	-	Reserved	-	-
25	-	Reserved	-	-
26	-	Reserved	-	-
27	-	Reserved	-	-
28	-	Reserved	-	-
29	-	Reserved	-	-
30	-	Reserved	-	-
31	-	Reserved	-	-

Table 170. LPC18xx Pin description (flash-based parts) *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P9_3	M6	-	-	79	[2]	N; PU	I/O	**GPIO4[15] —** General purpose digital input/output pin.
							O	**MCOA0 —** Motor control PWM channel 0, output A.
							O	**USB1_IND1 —** USB1 Port indicator LED control output 1.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_RXD2 —** Ethernet receive data 2 (MII interface).
							-	**R —** Function reserved.
							O	**U3_TXD —** Transmitter output for USART3.
P9_4	N10	-	-	92	[2]	N; PU	-	**R —** Function reserved.
							O	**MCOB0 —** Motor control PWM channel 0, output B.
							O	**USB1_IND0 —** USB1 Port indicator LED control output 0.
							-	**R —** Function reserved.
							I/O	**GPIO5[17] —** General purpose digital input/output pin.
							O	**ENET_TXD2 —** Ethernet transmit data 2 (MII interface).
							-	**R —** Function reserved.
							I	**U3_RXD —** Receiver input for USART3.
P9_5	M9	-	69	98	[2]	N; PU	-	**R —** Function reserved.
							O	**MCOA1 —** Motor control PWM channel 1, output A.
							O	**USB1_PPWR —** VBUS drive signal (towards external charge pump or power management unit); indicates that VBUS must be driven (active HIGH). Add a pull-down resistor to disable the power switch at reset. This signal has opposite polarity compared to the $\overline{\text{USB\_PPWR}}$ used on other NXP LPC parts.
							-	**R —** Function reserved.
							I/O	**GPIO5[18] —** General purpose digital input/output pin.
							O	**ENET_TXD3 —** Ethernet transmit data 3 (MII interface).
							-	**R —** Function reserved.
							O	**U0_TXD —** Transmitter output for USART0.
P9_6	L11	-	72	103	[2]	N; PU	I/O	**GPIO4[11] —** General purpose digital input/output pin.
							O	**MCOB1 —** Motor control PWM channel 1, output B.
							I	**USB1_PWR_FAULT —** USB1 Port power fault signal indicating over-current condition; this signal monitors over-current on the USB1 bus (external circuitry required to detect over-current condition).
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**ENET_COL —** Ethernet Collision detect (MII interface).
							-	**R —** Function reserved.
							I	**U0_RXD —** Receiver input for USART0.

19.8.1.4 Disabling a DMA channel

A DMA channel can be disabled in three ways:

- By writing directly to the channel enable bit. Any outstanding data in the FIFO's is lost if this method is used.
- By using the active and halt bits in conjunction with the channel enable bit.
- By waiting until the transfer completes. This automatically clears the channel.

Disabling a DMA channel and losing data in the FIFO

Clear the relevant channel enable bit in the relevant channel configuration register. The current AHB transfer (if one is in progress) completes and the channel is disabled. Any data in the FIFO is lost.

Disabling the DMA channel without losing data in the FIFO

- Set the halt bit in the relevant channel configuration register. This causes any future DMA request to be ignored.
- Poll the active bit in the relevant channel configuration register until it reaches 0. This bit indicates whether there is any data in the channel that has to be transferred.
- Clear the channel enable bit in the relevant channel configuration register

19.8.1.5 Setting up a new DMA transfer

To set up a new DMA transfer:

If the channel is not set aside for the DMA transaction:

1. Read the ENBLDCHNS controller register and find out which channels are inactive.
2. Choose an inactive channel that has the required priority.
3. Program the DMA controller

19.8.1.6 Halting a DMA channel

Set the halt bit in the relevant DMA channel configuration register. The current source request is serviced. Any further source DMA request is ignored until the halt bit is cleared.

19.8.1.7 Programming a DMA channel

1. Choose a free DMA channel with the priority needed. DMA channel 0 has the highest priority and DMA channel 7 the lowest priority.
2. Clear any pending interrupts on the channel to be used by writing to the IntTCClear and INTERRCLEAR register. The previous channel operation might have left interrupt active.
3. Write the source address into the CSRCADDR register.
4. Write the destination address into the CDESTADDR register.
5. Write the address of the next LLI into the CLLI register. If the transfer comprises of a single packet of data then 0 must be written into this register.
6. Write the control information into the CCONTROL register.
7. Write the channel configuration information into the CCONFIG register. If the enable bit is set then the DMA channel is automatically enabled.

- Program the SDRAM Delay value for the EMC_CLKn lines in the EMCDELAYCLK register in the SCU block. (See Section 16.4.9.) Add the SDRAM delay for most SDRAM devices running at frequencies above 96 MHz under typical conditions. Add the SDRAM delay at any frequency to compensate for variations over temperature. For details, see the *LPC1850_30_20_10 data sheet.*

Table 344. EMC clocking and power control

	Base clock	Branch clock	Operating frequency	Notes
EMC registers and EMC clock EMC_CCLK	BASE_M3_CLK	CLK_M3_EMC	up to 180 MHz	The maximum operating frequency depends on temperature and voltage settings and is typically 120 MHz for SDRAM devices. For details, see the LPC18xx data sheets.
EMC clock EMC_CCLK (divided clock)	BASE_M3_CLK	CLK_M3_EMC_DIV	up to 180 MHz	This is an alternative clock option for EMC_CCLK. This clock can run at the same frequency as BASE_M3_CLK or at half the frequency of BASE_M3_CLK.

22.3 Features

- 8-bit, 16-bit, and 32-bit wide static memory support with up to four chip selects.
- Asynchronous static memory device support including RAM, ROM, and NOR Flash, with or without asynchronous page mode.
- Static memory features include:
  - Asynchronous page mode read
  - Programmable wait states
  - Bus turnaround delay
  - Output enable and write enable delays
  - Extended wait
- 16-bit and 32-bit wide chip select SDRAM memory support with up to four chip selects and up to 256 MB of data.
- Controller supports 2 kbit, 4 kbit, and 8 kbit row address synchronous memory parts. That is typical 512 MB, 256 MB, and 128 MB parts, with 4, 8, 16, or 32 data bits per device.
- Dynamic memory interface support including Single Data Rate SDRAM. SDRAM maximum frequency of up to 120 MHz.
- Dynamic memory self-refresh mode controlled by software.
- Power-saving modes dynamically control EMC_CKEOUT and EMC_CLK to SDRAMs.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- Separate reset domains allow the for auto-refresh through a chip reset if desired.
- Programmable delay elements allow to fine-tune the EMC timing.

Table 358. Dynamic Memory Data In to Active Command Time register (DYNAMICDAL - address 0x4000 5040) bit description

Bit	Symbol	Description	Reset value
3:0	TDAL	Data-in to active command. 0x0 - 0xE = n clock cycles. The delay is in EMC_CCLK cycles. 0xF = 15 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

22.6.12 Dynamic Memory Write Recovery Time register

This register enables you to program the write recovery time, tWR. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tWR, tDPL, tRWL, or tRDL. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 359. Dynamic Memory Write Recovery Time register (DYNAMICWR - address 0x4000 5044) bit description

Bit	Symbol	Description	Reset value
3:0	TWR	Write recovery time. 0x0 - 0xE = n + 1 clock cycles. The delay is in EMC_CCLK cycles. 0xF = 16 clock cycles (POR reset value).	0xF
31:4	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

22.6.13 Dynamic Memory Active to Active Command Period register

This register enables you to program the active to active command period, tRC. It is recommended that this register is modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. This value is normally found in SDRAM data sheets as tRC. This register is accessed with one wait state.

Note: This register is used for all four dynamic memory chip selects. Therefore the worst case value for all of the chip selects must be programmed.

Table 360. Dynamic Memory Active to Active Command Period register (DYNAMICRC - address 0x4000 5048) bit description

Bit	Symbol	Description	Reset value
4:0	TRC	Active to active command period. 0x0 - 0x1E = n + 1 clock cycles. The delay is in EMC_CCLK cycles. 0x1F = 32 clock cycles (POR reset value).	0x1F
31:5	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	-

22.7.6 External static memory interface

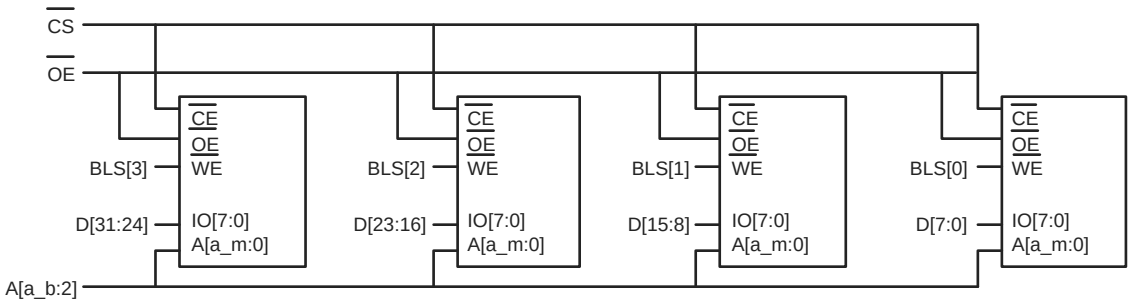
External memory interfacing depends on the bank width (32, 16 or 8 bit selected via MW bits in corresponding StaticConfig register).

If a memory bank is configured to be 32 bits wide, address lines A0 and A1 can be used as non-address lines. If a memory bank is configured to 16 bits wide, A0 is not required. However, 8 bit wide memory banks do require all address lines down to A0. Configuring A1 and/or A0 lines to provide address or non-address function is accomplished using the SYSCON registers.

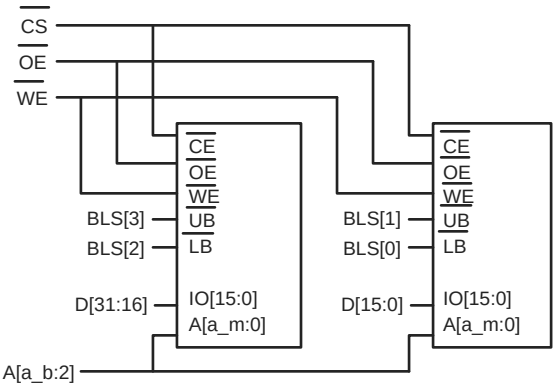
Symbol a_b in the following figures refers to the highest order address line in the data bus. Symbol a_m refers to the highest order address line of the memory chip used in the external memory interface.

If the external memory is used as external boot memory for flashless devices, refer to Section 4.2 on how to connect the EMC. The memory bank width for memory banks one and two is determined by the setting of the BOOT pins.

22.7.6.1 32 bit wide memory bank connection



a. 32 bit wide memory bank interfaced to four 8 bit memory chips



b. 32 bit wide memory bank interfaced to two 16 bit memory chips

Table 390. USB Command register in device mode (USBCMD_D - address 0x4000 6140) bit description *...continued*

Bit	Symbol	Value	Description	Access	Reset value
13	SUTW		Setup trip wire During handling a setup packet, this bit is used as a semaphore to ensure that the setup data payload of 8 bytes is extracted from a QH by the DCD without being corrupted. If the setup lockout mode is off (see USBMODE register) then there exists a hazard when new setup data arrives while the DCD is copying the setup data payload from the QH for a previous setup packet. This bit is set and cleared by software and will be cleared by hardware when a hazard exists. (See Section 23.10).	R/W	0
14	ATDTW		Add dTD trip wire This bit is used as a semaphore to ensure the to proper addition of a new dTD to an active (primed) endpoint's linked list. This bit is set and cleared by software during the process of adding a new dTD. See also Section 23.10. This bit shall also be cleared by hardware when its state machine is hazard region for which adding a dTD to a primed endpoint may go unrecognized.	R/W	0
15	-		Not used in device mode.	-	-
23:16	ITC		Interrupt threshold control. The system software uses this field to set the maximum rate at which the host/device controller will issue interrupts. ITC contains the maximum interrupt interval measured in micro-frames. Valid values are shown below. All other values are reserved. 0x0 = Immediate (no threshold) 0x1 = 1 micro frame. 0x2 = 2 micro frames. 0x8 = 8 micro frames. 0x10 = 16 micro frames. 0x20 = 32 micro frames. 0x40 = 64 micro frames.	R/W	0x8
31:24	-		Reserved		0

23.6.3.2 Host mode

Table 391. USB Command register in host mode (USBCMD_H - address 0x4000 6140) bit description - host mode

Bit	Symbol	Value	Description	Access	Reset value
0	RS		Run/Stop	R/W	0
		0	When this bit is set to 0, the Host Controller completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the Host Controller has finished the transaction and has entered the stopped state. Software should not write a one to this field unless the host controller is in the Halted state (i.e. HCHalted in the USBSTS register is a one).		
		1	When set to a 1, the Host Controller proceeds with the execution of the schedule. The Host Controller continues execution as long as this bit is set to a one.		

  - USB descriptors data structure (Table 500 “_USB_CORE_DESCS_T class structure”)
  - USB device stack initialization parameter data structure (Table 509 “USBD_API_INIT_PARAM class structure”).
  - USB device stack core API functions structure (Table 512 “USBD_CORE_API class structure”).
- Device Firmware Upgrade (DFU) class function driver
  - DFU descriptors data structure (Table 514 “USBD_DFU_INIT_PARAM class structure”).
  - DFU class API functions structure. This module exposes functions which interact directly with the USB device controller hardware (Table 513 “USBD_DFU_API class structure”).
- HID class function driver
  - struct (Table 493 “_HID_DESCRIPTOR class structure”).
  - struct (Table 495 “_HID_REPORT_T class structure”).
  - USB descriptors data structure (Table 516 “USBD_HID_INIT_PARAM class structure”).
  - HID class API functions structure. This structure contains pointers to all the functions exposed by the HID function driver module (Table 517 “USBD_HW_API class structure”).
- USB device controller driver
  - Hardware API functions structure. This module exposes functions which interact directly with the USB device controller hardware (Table 517 “USBD_HW_API class structure”).
- Mass Storage Class (MSC) function driver
  - Mass Storage Class function driver initialization parameter data structure (Table 519).
  - MSC class API functions structure. This module exposes functions which interact directly with the USB device controller hardware (Table 518).

25.4 Calling the USB device driver

A fixed location in ROM contains a pointer to the ROM driver table i.e. 0x1FFF 1FF8. The ROM driver table contains a pointer to the USB driver table. Pointers to the various USB driver functions are stored in this table. USB driver functions can be called by using a C structure. Figure 65 illustrates the pointer mechanism used to access the on-chip USB driver.

```
typedef struct USBD_API

{

const USBD_HW_API_T* hw;

const USBD_CORE_API_T* core;

const USBD_MSC_API_T* msc;
```

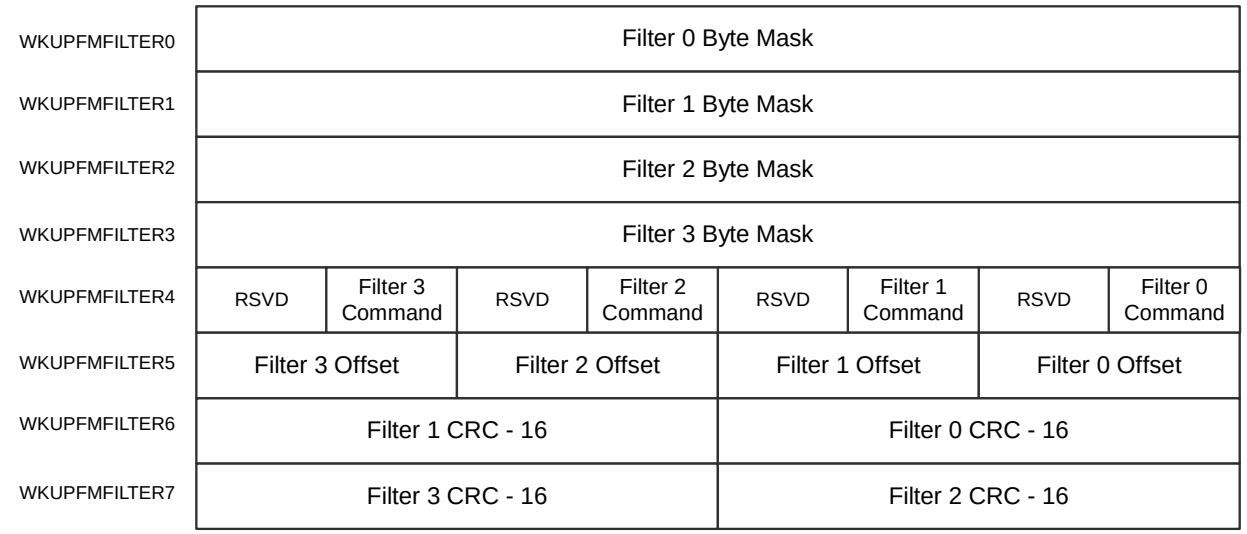


Fig 68. Wake-up frame filter register

Filter i byte mask

This register defines which bytes of the frame are examined by filter i (0, 1, 2, and 3) in order to determine whether or not the frame is a wake-up frame. The MSB (thirty-first bit) must be zero. Bit j [30:0] is the Byte Mask. If bit j (byte number) of the Byte Mask is set, then Filter i Offset + j of the incoming frame is processed by the CRC block; otherwise Filter i Offset + j is ignored.

Filter i command

This 4-bit command controls the filter i operation. Bit 3 specifies the address type, defining the pattern's destination address type. When the bit is set, the pattern applies to only multicast frames; when the bit is reset, the pattern applies only to unicast frame. Bit 2 and Bit 1 are reserved. Bit 0 is the enable for filter i; if Bit 0 is not set, filter i is disabled.

Filter i offset

This register defines the offset (within the frame) from which filter i examines the frames. This 8-bit pattern offset is the offset for the filter i first byte to be examined. The minimum allowed is 12, which refers to the 13th byte of the frame. The offset value 0 refers to the first byte of the frame.

Filter i CRC-16

This register contains the CRC_16 value calculated from the pattern, as well as the byte mask programmed to the wake-up filter register block.

26.7.2.2 Remote wake-up detection

When the MAC is in sleep mode and the remote wake-up bit is enabled in PMT Control and Status register (0x002C), normal operation is resumed after receiving a remote wake-up frame. The Application writes all eight wake-up filter registers by performing a sequential Write to address (0x0028). The Application enables remote wake-up by writing a 1 to Bit 2 of the PMT Control and Status register.

Table 739. MCPWM Count Control read address (CNTCON - 0x400A 005C) bit description

Bit	Symbol	Value	Description	Reset value
14	TC2MCI1_RE		Counter 2 rising edge mode, channel 1.	0
		0	A rising edge on MCI1 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a rising edge on MCI1.	
15	TC2MCI1_FE		Counter 2 falling edge mode, channel 1.	0
		0	A falling edge on MCI1 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a falling edge on MCI1.	
16	TC2MCI2_RE		Counter 2 rising edge mode, channel 2.	0
		0	A rising edge on MCI2 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a rising edge on MCI2.	
17	TC2MCI2_FE		Counter 2 falling edge mode, channel 2.	0
		0	A falling edge on MCI2 does not affect counter 2.	
		1	If MODE2 is 1, counter 2 advances on a falling edge on MCI2.	
28:18	-	-	Reserved.	-
29	CNTR0		Channel 0 counter/timer mode.	0
		0	Channel 0 is in timer mode.	
		1	Channel 0 is in counter mode.	
30	CNTR1		Channel 1 counter/timer mode.	0
		0	Channel 1 is in timer mode.	
		1	Channel 1 is in counter mode.	
31	CNTR2		Channel 2 counter/timer mode.	0
		0	Channel 2 is in timer mode.	
		1	Channel 2 is in counter mode.	

31.7.10.2 MCPWM Count Control set address

Writing one(s) to this write-only address sets the corresponding bit(s) in CNTCON.

Table 740. MCPWM Count Control set address (CNTCON_SET - 0x400A 0060) bit description

Bit	Symbol	Description	Reset value
0	TC0MCI0_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
1	TC0MCI0_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
2	TC0MCI1_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
3	TC0MCI1_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
4	TC0MCI2_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
5	TC0MCI2_FE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-
6	TC1MCI0_RE_SET	Writing a one sets the corresponding bit in the CNTCON register.	-

37.7.1 Event Monitor/Recorder Control Register

The Event Monitor/Recorder Control Register allows setup of the Event Monitor/Recorder and individual control over aspects of each channel's operation.

Table 838. Event Monitor/Recorder Control Register (ERCONTROL - address 0x4004 6084) bit description

Bit	Symbol	Value	Description	Reset value
0	INTWAKE_EN0		Interrupt and wakeup enable for channel 0.	0
		0	No interrupt or wakeup will be generated by event channel 0.	
		1	An event in channel 0 will trigger an (RTC) interrupt and a wake-up request.	
1	GPCLEAR_EN0		Enables automatically clearing the RTC general purpose registers when an event occurs on channel 0.	0
		0	Channel 0 has no influence on the general purpose registers.	
		1	An event in channel 0 will clear the general purpose registers asynchronously.	
2	POL0		Selects the polarity of an event on input pin WAKEUP0.	0
		0	A channel 0 event is defined as a negative edge on WAKEUP0.	
		1	A channel 0 event is defined as a positive edge on WAKEUP0.	
3	EV0_INPUT_EN		Event enable control for channel 0. Event Inputs should remain DISABLED when not being used for event detection, particularly if the associated pin is being used for some other function.	0
		0	Event 0 input is disabled and forced high internally.	
		1	Event 0 input is enabled.	
9:4	-		Reserved. Read value is undefined, only zero should be written.	NA
10	INTWAKE_EN1		Interrupt and wakeup enable for channel 1.	0
		0	No interrupt or wakeup will be generated by event channel 1.	
		1	An event in channel 1 will trigger an (RTC) interrupt and a wake-up request.	
11	GPCLEAR_EN1		Enables automatically clearing the RTC general purpose registers when an event occurs on channel 1.	0
		0	Channel 1 has no influence on the general purpose registers.	
		1	A n event in channel 1 will clear the general purpose registers asynchronously.	
12	POL1		Selects the polarity of an event on input pin WAKEUP1.	0
		0	A channel 1 event is defined as a negative edge on WAKEUP1.	
		1	A channel 1 event is defined as a positive edge on WAKEUP1.	
13	EV1_INPUT_EN		Event enable control for channel 1. Event Inputs should remain DISABLED when not being used for event detection, particularly if the associated pin is being used for some other function.	0
		0	Event 1 input is disabled and forced high internally.	
		1	Event 1 input is enabled.	
19:14	-		Reserved. Read value is undefined, only zero should be written.	NA
20	INTWAKE_EN2		Interrupt and wakeup enable for channel 2.	
		0	No interrupt or wakeup will be generated by event channel 2.	
		1	An event in channel 2 will trigger an (RTC) interrupt and a wake-up request.	

Table 838. Event Monitor/Recorder Control Register (ERCONTROL - address 0x4004 6084) bit description

Bit	Symbol	Value	Description	Reset value
21	GPCLEAR_EN2		Enables automatically clearing the RTC general purpose registers when an event occurs on channel 2.	0
		0	Channel 2 has no influence on the general purpose registers.	
		1	An event in channel 2 will clear the general purpose registers asynchronously.	
22	POL2		Selects the polarity of an event on input pin WAKEUP2.	0
		0	A channel 2 event is defined as a negative edge on WAKEUP2.	
		1	A channel 2 event is defined as a positive edge on WAKEUP2.	
23	EV2_INPUT_EN		Event enable control for channel 2. Event Inputs should remain DISABLED when not being used for event detection, particularly if the associated pin is being used for some other function.	0
		0	Event 2 input is disabled and forced high internally.	
		1	Event 2 input is enabled.	
29:24	-		Reserved. Read value is undefined, only zero should be written.	NA
31:30	ERMODE		Controls enabling the Event Monitor/Recorder and selecting its operating frequency. Event Monitor/Recorder registers can always be written to regardless of the state of these bits. Events occurring during the 1-sec interval immediately following enabling of the clocks may not be recognized.	0
		0x0	Disable Event Monitor/Recorder clocks. Operation of the Event Monitor/Recorder is disabled except for asynchronous clearing of GP registers if selected.	
		0x1	16 Hz sample clock. Enable Event Monitor/Recorder and select a 16 Hz sample clock for event input edge detection and glitch suppression. Pulses (in either direction) shorter than 62.5 ms to 125 ms will be filtered out.	
		0x2	64 Hz sample clock. Enable Event Monitor/Recorder and select a 64 Hz sample clock for event input edge detection and glitch suppression. Pulses (in either direction) shorter than 15.6 ms to 31.2 ms will be filtered out.	
		0x3	1 kHz sample clock. Enable Event Monitor/Recorder and select a 1 kHz sample clock for event input edge detection and glitch suppression. Pulses (in either direction) shorter than 1 ms to 2 ms will be filtered out.	

Table 867. USART Synchronous mode control registers (SYNCCTRL - address addresses 0x4008 1058 (USART0), 0x400C 1058 (USART2), 0x400C 2058 (USART3)) bit description

Bit	Symbol	Value	Description	Reset value
5	SSSDIS		Start/stop bits	0
		0	Send start and stop bits as in other modes.	
		1	Do not send start/stop bits.	
6	CCCLR		Continuous clock clear	0
		0	CSCEN is under software control.	
		1	Hardware clears CSCEN after each character is received.	
31:7	-		Reserved. The value read from a reserved bit is not defined.	NA

After reset, synchronous mode is disabled. Synchronous mode allows the user to send (synchronous master mode) or receive (synchronous slave mode) a clock with the serial input and output data. Synchronous mode is enabled by setting the SYNC bit. The CSRC bit can be used to switch between synchronous slave mode (logic 0) and synchronous master mode (logic 1). The serial data can either be sampled on the rising edge (default) or the falling edge of the serial clock. When the STARTSTOPDISABLE bit is set, the FES bit is hardware overwritten to sample on the falling edge.

A master clock is only required to generate a clock when transmitting data. In this case, data can only be received when data is transmitted. When the CSCEN bit is set, the clock will always be running (during synchronous master mode only), allowing data to be received continuously.

Note that this option should not be used in combination with STARTSTOPDISABLE (during full-duplex communication). The continuous clock can be automatically stopped by hardware after having received a complete character. This can be done by asserting the CCCLR bit. This is useful in half-duplex mode, where the clock cannot be generated by sending a character. After the reception of one character, the CSCEN bit is automatically cleared by hardware. When another character needs to be received, the CSCEN should be enabled again.

By default data transmission and reception performs the same in asynchronous mode and synchronous mode. When the STARTSTOPDISABLE bit is set, no start and stop bits are transmitted (nor are they received). This means that all bits that are send or received (a clock is running) are data bits.

Remark: The value of the SYNCCTRL register should not be modified while transmitting/receiving, data or data might get lost or corrupted.

Remark: The SYNCCTRL register should not be enabled in combination with the SCICTRL register, as only asynchronous smart card is supported.

The fractional baud rate generator must be disabled (DIVADDVAL = 0) during auto-baud. Also, when auto-baud is used, any write to DLM and DLL registers should be done before ACR register write. The minimum and the maximum baud rates supported by USART are function of USART_PCLK, number of data bits, stop bits and parity bits.

(7)

$$ratemin = \frac{2 \times PCLK}{16 \times 2^{15}} \leq UART_{baudrate} \leq \frac{PCLK}{16 \times (2 + databits + paritybits + stopbits)} = ratemax$$

38.7.2 Auto-baud modes

When the software is expecting an ”AT" command, it configures the USART with the expected character format and sets the ACR Start bit. The initial values in the divisor latches DLM and DLM don‘t care. Because of the ”A" or ”a" ASCII coding (”A" = 0x41, ”a" = 0x61), the USART Rx pin sensed start bit and the LSB of the expected character are delimited by two falling edges. When the ACR Start bit is set, the auto-baud protocol will execute the following phases:

1. On ACR Start bit setting, the baud rate measurement counter is reset and the USART RSR is reset. The RSR baud rate is switched to the highest rate.
2. A falling edge on USART Rx pin triggers the beginning of the start bit. The rate measuring counter will start counting USART_PCLK cycles.
3. During the receipt of the start bit, 16 pulses are generated on the RSR baud input with the frequency of the USART input clock, guaranteeing the start bit is stored in the RSR.
4. During the receipt of the start bit (and the character LSB for Mode = 0), the rate counter will continue incrementing with the pre-scaled USART input clock (USART_PCLK).
5. If Mode = 0, the rate counter will stop on next falling edge of the USART Rx pin. If Mode = 1, the rate counter will stop on the next rising edge of the USART Rx pin.
6. The rate counter is loaded into DLM/DLL and the baud rate will be switched to normal operation. After setting the DLM/DLL, the end of auto-baud interrupt IIR ABEOInt will be set, if enabled. The RSR will now continue receiving the remaining bits of the ”A/a" character.

Table 888: UART1 RS485 Control register (RS485CTRL - address 0x4008 204C) bit description

Bit	Symbol	Value	Description	Reset value
5	OINV		Polarity. This bit reverses the polarity of the direction control signal on the RTS (or DTR) pin.	0
		0	The direction control pin will be driven to logic ‘0’ when the transmitter has data to be sent. It will be driven to logic ‘1’ after the last bit of data has been transmitted.	
		1	The direction control pin will be driven to logic ‘1’ when the transmitter has data to be sent. It will be driven to logic ‘0’ after the last bit of data has been transmitted.	
31:6	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

39.6.15 UART1 RS-485 Address Match register

The RS485ADRMATCH register contains the address match value for RS-485/EIA-485 mode.

Table 889. UART1 RS485 Address Match register (RS485ADRMATCH - address 0x4008 2050) bit description

Bit	Symbol	Description	Reset value
7:0	ADRMATCH	Contains the address match value.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

39.6.16 UART1 RS-485 Delay value register

The user may program the 8-bit RS485DLY register with a delay between the last stop bit leaving the TXFIFO and the de-assertion of $\overline{\text{RTS}}$ (or $\overline{\text{DTR}}$). This delay time is in periods of the baud clock. Any delay time from 0 to 255 bit times may be programmed.

Table 890. UART1 RS485 Delay value register (RS485DLY - address 0x4008 2054) bit description

Bit	Symbol	Description	Reset value
7:0	DLY	Contains the direction control (RTS or DTR) delay value. This register works in conjunction with an 8-bit counter.	0x00
31:8	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

39.6.17 UART1 Transmit Enable Register

In addition to being equipped with full hardware flow control (auto-cts and auto-rts mechanisms described above), TER enables implementation of software flow control, too. When TXEN=1, UART1 transmitter will keep sending data as long as they are available. As soon as TXEN becomes 0, UART1 transmission will stop.

Table 1024.A/D Global Data register (GDR - address 0x400E 3004 (ADC0) and 0x400E 4004 (ADC1)) bit description

Bit	Symbol	Description	Reset value
29:27	-	Reserved. These bits always read as zeroes.	0
30	OVERRUN	This bit is 1 in burst mode if the results of one or more conversions was (were) lost and overwritten before the conversion that produced the result in the V_VREF bits.	0
31	DONE	This bit is set to 1 when an analog-to-digital conversion completes. It is cleared when this register is read and when the AD0/1CR register is written. If the AD0/1CR is written while a conversion is still in progress, this bit is set and a new conversion is started.	0

44.6.3 A/D Interrupt Enable register

This register allows control over which A/D channels generate an interrupt when a conversion is complete. For example, it may be desirable to use some A/D channels to monitor sensors by continuously performing conversions on them. The most recent results are read by the application program whenever they are needed. In this case, an interrupt is not desirable at the end of each conversion for some A/D channels.

Table 1025.A/D Interrupt Enable register (INTEN - address 0x400E 300C (ADC0) and 0x400E 400C (ADC1)) bit description

Bit	Symbol	Description	Reset value
7:0	ADINTEN	These bits allow control over which A/D channels generate interrupts for conversion completion. When bit 0 is one, completion of a conversion on A/D channel 0 will generate an interrupt, when bit 1 is one, completion of a conversion on A/D channel 1 will generate an interrupt, etc.	0x00
8	ADGINTEN	When 1, enables the global DONE flag in ADDR to generate an interrupt. When 0, only the individual A/D channels enabled by ADINTEN 7:0 will generate interrupts.	1
31:9	-	Reserved. Always 0.	0

44.6.4 A/D Data Registers

The A/D Data Register hold the result when an A/D conversion is complete, and also include the flags that indicate when a conversion has been completed and when a conversion overrun has occurred.

Table 1026.A/D Data registers (DR - addresses 0x400E 3010 (DR0) to 0x400E 302C (DR7) (ADC0); 0x400E 4010 (DR0) to 0x400E 402C (DR7) (ADC1)) bit description

Bit	Symbol	Description	Reset value
5:0	-	Reserved. Always 0.	0
15:6	V_VREF	When DONE is 1, this field contains a binary fraction representing the voltage on the ADCn input pin selected in Table 1023, divided by the voltage on the VDDA pin. Zero in the field indicates that the voltage on the ADCn input pin was less than, equal to, or close to that on VDDA, while 0x3FF indicates that the voltage on ADCn input pin was close to, equal to, or greater than that on VDDA.	-

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