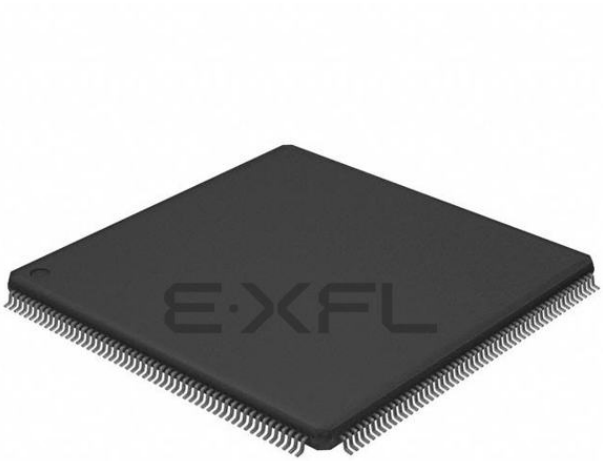

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Program Memory Type	FLASH
EEPROM Size	-
RAM Size	136K x 8
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Supplier Device Package	208-LQFP (28x28)
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Table 92. DMA mux control register (DMAMUX, address 0x4004 311C) bit description

Bit	Symbol	Value	Description	Reset value	Access
17:16	DMAMUXPER8		Select DMA to peripheral connection for DMA peripheral 8.	0	R/W
		0x0	Timer3 match 1		
		0x1	USART3 receive		
		0x2	SCT DMA request 1		
		0x3	Reserved		
19:18	DMAMUXPER9		Select DMA to peripheral connection for DMA peripheral 9.	0	R/W
		0x0	SSP0 receive		
		0x1	I2S0 DMA request 1		
		0x2	SCT DMA request 1		
		0x3	Reserved		
21:20	DMAMUXPER10		Select DMA to peripheral connection for DMA peripheral 10.	0	R/W
		0x0	SSP0 transmit		
		0x1	I2S0 DMA request 2		
		0x2	SCT DMA request 0		
		0x3	Reserved		
23:22	DMAMUXPER11		Selects DMA to peripheral connection for DMA peripheral 11.	0	R/W
		0x0	SSP1 receive		
		0x1	Reserved		
		0x2	USART0 transmit		
		0x3	Reserved		
25:24	DMAMUXPER12		Select DMA to peripheral connection for DMA peripheral 12.	0	R/W
		0x0	SSP1 transmit		
		0x1	Reserved		
		0x2	USART0 receive		
		0x3	Reserved		
27:26	DMAMUXPER13		Select DMA to peripheral connection for DMA peripheral 13.	0	R/W
		0x0	ADC0		
		0x1	AES in		
		0x2	SSP1 receive		
		0x3	USART3 receive		
29:28	DMAMUXPER14		Select DMA to peripheral connection for DMA peripheral 14.	0	R/W
		0x0	ADC1		
		0x1	AES out		
		0x2	SSP1 transmit		
		0x3	USART3 transmit		

Table 131. BASE_OUT_CLK control register (BASE_OUT_CLK, addresses 0x4005 00AC) bit description *…continued*

Bit	Symbol	Value	Description	Reset value	Access
28:24	CLK_SEL		Clock-source selection.	0x01	R/W
		0x00	32 kHz oscillator		
		0x01	IRC (default)		
		0x02	ENET_RX_CLK		
		0x03	ENET_TX_CLK		
		0x04	GP_CLKIN		
		0x05	Reserved		
		0x06	Crystal oscillator		
		0x07	PLL0USB		
		0x08	PLL0AUDIO		
		0x09	PLL1		
		0x0C	IDIVA		
		0x0D	IDIVB		
		0x0E	IDIVC		
		0x0F	IDIVD		
		0x10	IDIVE		
31:29	-		Reserved	-	-

12.6.14 BASE_AUDIO_CLK register

Table 132. BASE_AUDIO_CLK control register (BASE_AUDIO_CLK, addresses 0x4005 00C0) bit description

Bit	Symbol	Value	Description	Reset value	Access
0	PD		Output stage power down	0	R/W
		0	Output stage enabled (default)		
		1	power-down		
10:1	-		Reserved	-	-
11	AUTOBLOCK		Block clock automatically during frequency change	0	R/W
		0	Autoblocking disabled		
		1	Autoblocking enabled		
23:12	-		Reserved	-	-

Table 136. PLL0 (for USB) settings for 480 MHz output clock

Fclkin [MHz]	PLL0USB_MDIV Table 115	PLL0USB_NP_DIV Table 116
1	0x073E 56C9	0x0030 2062
2	0x073E 2DAD	0x0030 2062
3	0x0B3E 34B1	0x0030 2062
4	0x0E3E 7777	0x0030 2062
5	0x0D32 6667	0x0030 2062
6	0x0B2A 2A66	0x0030 2062
8	0x0820 6AAA	0x0030 2062
10	0x071A 7FAA	0x0030 2062
12	0x0616 7FFA	0x0030 2062
15	0x0512 3FFF	0x0030 2062
16	0x0410 1FFF	0x0030 2062
20	0x040E 03FF	0x0030 2062
24	0x030C 00FF	0x0030 2062

12.8.4 PLL0AUDIO settings for audio applications

12.8.4.1 Using the fractional divider

Table 137 shows typical divider settings for the audio PLL0 with the fractional divider active.

To use the fractional divider, follow these steps:

1. Set bit SEL_EXT = 0 and PLLFRACT_REQ = 1 in the PLL0AUDIO_CTRL register (Table 118).
2. Calculate NDEC, PDEC, and PLLFRACT_CTRL for the output frequency Fout.
3. Write the calculated NDEC and PDEC values to the PLL0AUDIO_NP_DIV register.
4. Write the calculated PLLFRACT_CTRL value to the PLL0AUDIOFRAC register.

Table 137. PLL0AUDIO divider settings for 12 MHz input

Fs [kHz]	Fout [MHz]	Fcco [MHz]	Error [Hz]	NDEC	PDEC	PLL0AUDIO_NP_DIV Table 120	PLLF0RACT_CTRL Table 121
128Fs							
192	24.576	540.672	1	514	29	0x0000201d	0x16872b
96	12.288	417.792	1	1	3	0x00001003	0x1a1cac
88.2	11.2896	338.688	1	0	24	0x00000018	0x070e56
64	8.192	344.064	1	0	30	0x0000001e	0x072b02
48	6.144	307.2	1	1	6	0x00001006	0x133333
44.1	5.6448	282.24	1	1	6	0x00001006	0x11a3d7
256Fs							
192	49.152	491.52	11	514	5	0x00002005	0x147ae1
96	24.576	540.672	1	514	29	0x0000201d	0x16872b

Table 159. Reset status register 1 (RESET_STATUS1, address 0x4005 3114) bit description

…continued

Bit	Symbol	Description	Reset value	Access
11:10	EMC_RST	Status of the EMC_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
13:12	ETHERNET_RST	Status of the ETHERNET_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
15:14	-	Reserved	01	-
17:16	-	Reserved	01	-
19:18	FLASHA_RST	Status of the FLASHA_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	-
21:20	-	Reserved	01	-
23:22	EEPROM_RST	Status of the EEPROM_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	-
25:24	GPIO_RST	Status of the GPIO_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	R/W
27:26	FLASHB_RST	Status of the FLASHB_RST reset generator output 00 = No reset activated 01 = Reset output activated by input to the reset generator 10 = Reserved 11 = Reset output activated by software write to RESET_CTRL register	01	-
29:28	-	Reserved	01	-
31:30	-	Reserved	01	-

Table 169. LPC1850/30/20/10 Pin description (flashless parts) *…continued*
LCD, Ethernet, USB0, and USB1 functions are not available on all parts.

Symbol	LBGA256	TFBGA180	TFBGA100	LQFP144		Reset state [1]	Type	Description
PE_11	D16	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_12 —** SCT output 12. Match output 3 of timer 3.
							O	**U1_TXD —** Transmitter output for UART1.
							I/O	**EMC_D30 —** External memory data line 30.
							I/O	**GPIO7[11] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_12	D15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_11 —** SCT output 11. Match output 3 of timer 2.
							I	**U1_RXD —** Receiver input for UART1.
							I/O	**EMC_D31 —** External memory data line 31.
							I/O	**GPIO7[12] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_13	G14	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							O	**CTOUT_14 —** SCT output 14. Match output 2 of timer 3.
							I/O	**I2C1_SDA —** I^2C1 data input/output (this pin does not use a specialized I^2C pad).
							O	**EMC_DQMOUT3 —** Data mask 3 used with SDRAM and static devices.
							I/O	**GPIO7[13] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
PE_14	C15	-	-	-	[2]	N; PU	-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							O	**$\overline{\text{EMC\_DYCS3}}$ —** SDRAM chip select 3.
							I/O	**GPIO7[14] —** General purpose digital input/output pin.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.

Table 170. LPC18xx Pin description (flash-based parts) *…continued*

Pin name	LBGA256	TFBGA100	LQFP144	LQFP208		Reset state [1]	Type	Description
P1_13	R10	H8	60	83	[2]	N; PU	I/O	**GPIO1[6] —** General purpose digital input/output pin.
							O	**U1_TXD —** Transmitter output for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D6 —** External memory data line 6.
							I	**T0_CAP0 —** Capture input 0 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							I	**SD_CD —** SD/MMC card detect input.
P1_14	R11	J8	61	85	[2]	N; PU	I/O	**GPIO1[7] —** General purpose digital input/output pin.
							I	**U1_RXD —** Receiver input for UART1.
							-	**R —** Function reserved.
							I/O	**EMC_D7 —** External memory data line 7.
							O	**T0_MAT2 —** Match output 2 of timer 0.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
							-	**R —** Function reserved.
P1_15	T12	K8	62	87	[2]	N; PU	I/O	**GPIO0[2] —** General purpose digital input/output pin.
							O	**U2_TXD —** Transmitter output for USART2.
							-	**R —** Function reserved.
							I	**ENET_RXD0 —** Ethernet receive data 0 (RMII/MII interface).
							O	**T0_MAT1 —** Match output 1 of timer 0.
							-	**R —** Function reserved.
							I/O	**EMC_D8 —** External memory data line 8.
							-	**R —** Function reserved.
P1_16	M7	H9	64	90	[2]	N; PU	I/O	**GPIO0[3] —** General purpose digital input/output pin.
							I	**U2_RXD —** Receiver input for USART2.
							-	**R —** Function reserved.
							I	**ENET_CRS —** Ethernet Carrier Sense (MII interface).
							O	**T0_MAT0 —** Match output 0 of timer 0.
							-	**R —** Function reserved.
							I/O	**EMC_D9 —** External memory data line 9.
							I	**ENET_RX_DV —** Ethernet Receive Data Valid (RMII/MII interface).

Table 236. Pin interrupt falling edge register (FALL, address 0x4008 7020) bit description

Bit	Symbol	Description	Reset value	Access
7:0	FDET	Falling edge detect. Bit n detects the falling edge of the pin selected in PINTSELn. Read 0: No falling edge has been detected on this pin since Reset or the last time a one was written to this bit. Write 0: no operation. Read 1: a falling edge has been detected since Reset or the last time a one was written to this bit. Write 1: clear falling edge detection for this pin.	0	R/W
31:8	-	Reserved.	-	-

18.5.1.10 Pin interrupt status register

Reading this register returns ones for pin interrupts that are currently requesting an interrupt. For pins identified as edge-sensitive in the Interrupt Select register, writing ones to this register clears both rising- and falling-edge detection for the pin. For level-sensitive pins, writing ones inverts the corresponding bit in the Active level register, thus switching the active level on the pin.

Table 237. Pin interrupt status register (IST address 0x4008 7024) bit description

Bit	Symbol	Description	Reset value	Access
7:0	PSTAT	Pin interrupt status. Bit n returns the status, clears the edge interrupt, or inverts the active level of the pin selected in PINTSELn. Read 0: interrupt is not being requested for this interrupt pin. Write 0: no operation. Read 1: interrupt is being requested for this interrupt pin. Write 1 (edge-sensitive): clear rising- and falling-edge detection for this pin. Write 1 (level-sensitive): switch the active level for this pin (in the IENF register).	0	R/W
31:8	-	Reserved.	-	-

18.5.2 GPIO GROUP0/GROUP1 interrupt register description

18.5.2.1 Grouped interrupt control register

Table 238. GPIO grouped interrupt control register (CTRL, addresses 0x4008 8000 (GROUP0 INT) and 0x4008 9000 (GROUP1 INT)) bit description

Bit	Symbol	Value	Description	Reset value
0	INT		Group interrupt status. This bit is cleared by writing a one to it. Writing zero has no effect.	0
		0	No interrupt request is pending.	
		1	Interrupt request is active.	

20.6.20 FIFO Threshold Watermark Register (FIFOTH)

Table 298. FIFO Threshold Watermark Register (FIFOTH, address 0x4000 404C) bit description

Bit	Symbol	Value	Description	Reset value
11:0	TX_WMARK		FIFO threshold watermark level when transmitting data to card. When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. If Interrupt is enabled, then interrupt occurs. During end of packet, request or interrupt is generated, regardless of threshold programming. In non-DMA mode, when transmit FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty). In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. 12 bits - 1 bit less than FIFO-count of status register, which is 13 bits. Limitation: TX_WMark >= 1; Recommended value: TX_WMARK = 16; (means less than or equal to FIFO_DEPTH/2).	0
15:12	-		Reserved.	0
27:16	RX_WMARK		FIFO threshold watermark level when receiving data to card. When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data. In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt. In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. 12 bits - 1 bit less than FIFO-count of status register, which is 13 bits. Limitation: RX_WMark less than FIFO_DEPTH-2 Recommended: RX_WMARK = 15; (means greater than (FIFO_DEPTH/2) - 1) NOTE: In DMA mode during CCS time-out, the DMA does not generate the request at the end of packet, even if remaining bytes are less than threshold. In this case, there will be some data left in the FIFO. It is the responsibility of the application to reset the FIFO after the CCS time-out.	0x1F

For static memory larger delays are defined by in steps of one EMC clock cycle by the STATICWAIT registers (see Section 22.6.22 to Section 22.6.27).

22.7.4 Data buffers

The AHB interface reads and writes via buffers to improve memory bandwidth and reduce transaction latency. The EMC contains four 16-word buffers. The buffers can be used as read buffers, write buffers, or a combination of both. The buffers are allocated automatically.

The buffers must be disabled during SDRAM initialization. The buffers must be enabled during normal operation.

The buffers can be enabled or disabled for static memory using the StaticConfig Registers.

22.7.4.1 Write buffers

Write buffers are used to:

- Merge write transactions so that the number of external transactions are minimized.

  Buffer data until the EMC can complete the write transaction, improving AHB write latency.

  Convert all dynamic memory write transactions into quadword bursts on the external memory interface. This enhances transfer efficiency for dynamic memory.
- Reduce external memory traffic. This improves memory bandwidth and reduces power consumption.

Write buffer operation:

- If the buffers are enabled, an AHB write operation writes into the Least Recently Used (LRU) buffer, if empty.

  If the LRU buffer is not empty, the contents of the buffer are flushed to memory to make space for the AHB write data.
- If a buffer contains write data it is marked as dirty, and its contents are written to memory before the buffer can be reallocated.

The write buffers are flushed whenever:

- The memory controller state machine is not busy performing accesses to external memory.

  The memory controller state machine is not busy performing accesses to external memory, and an AHB interface is writing to a different buffer.

Note: For dynamic memory, the smallest buffer flush is a quadword of data. For static memory, the smallest buffer flush is a byte of data.

22.7.4.2 Read buffers

Read buffers are used to:

- Buffer read requests from memory. Future read requests that hit the buffer read the data from the buffer rather than memory, reducing transaction latency.

Table 551. DMA Bus mode register (DMA_BUS_MODE, address 0x4001 1000) bit description *…continued*

Bit	Symbol	Description	Reset value	Access
13:8	PBL	Programmable burst length These bits indicate the maximum number of beats to be transferred in one DMA transaction. This will be the maximum value that is used in a single block Read/Write. The DMA will always attempt to burst as specified in PBL each time it starts a Burst transfer on the host bus. PBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value will result in undefined behavior. When USP is set high, this PBL value is applicable for TxDMA transactions only. The PBL values have the following limitations. The maximum number of beats (PBL) possible is limited by the size of the Tx FIFO and Rx FIFO in the MTL layer and the data bus width on the DMA. The FIFO has a constraint that the maximum beat supported is half the depth of the FIFO, except when specified (as given below). For different data bus widths and FIFO sizes, the valid PBL range (including x8 mode) is provided in the following table. If the PBL is common for both transmit and receive DMA, the minimum Rx FIFO and Tx FIFO depths must be considered. Do not program out-of-range PBL values, because the system may not behave properly.	1	R/W
15:14	PR	Rx-to-Tx priority ratio RxDMA requests given priority over TxDMA requests in the following ratio. This is valid only when the DA bit is reset. 00 = 1-to-1 01 = 2-to-1 10 = 3-to-1 11 = 4-to-1	00	R/W
16	FB	Fixed burst This bit controls whether the AHB Master interface performs fixed burst transfers or not. When set, the AHB will use only SINGLE, INCR4, INCR8 or INCR16 during start of normal burst transfers. When reset, the AHB will use SINGLE and INCR burst transfer operations.	0	R/W
22:17	RPBL	RxDMA PBL These bits indicate the maximum number of beats to be transferred in one RxDMA transaction. This will be the maximum value that is used in a single block Read/Write. The RxDMA will always attempt to burst as specified in RPBL each time it starts a Burst transfer on the host bus. RPBL can be programmed with permissible values of 1, 2, 4, 8, 16, and 32. Any other value will result in undefined behavior. These bits are valid and applicable only when USP is set high.	1	R/W
23	USP	Use separate PBL When set high, it configures the RxDMA to use the value configured in bits [22:17] as PBL while the PBL value in bits [13:8] is applicable to TxDMA operations only. When reset to low, the PBL value in bits [13:8] is applicable for both DMA engines.	0	R/W
24	PBL8X	8 x PBL mode When set high, this bit multiplies the PBL value programmed (bits [22:17] and bits [13:8]) eight times. Thus the DMA will transfer data in to a maximum of 8, 16, 32, 64, 128, and 256 beats depending on the PBL value. **Remark:** This bit function is not backward compatible. Before version 3.50a, this bit was 4xPBL.	0	R/W

Table 608. Cursor Image registers (CRSR_IMG, address 0x4000 8800 (CRSR_IMG0) to 0x4000 8BFC (CRSR_IMG255)) bit description

Bit	Symbol	Description	Reset value
31:0	CRSR_IMG	Cursor Image data. The 256 words of the cursor image registers define the appearance of either one 64x64 cursor or 4 32x32 cursors.	0x0

27.6.16 Cursor Control register

The CRSR_CTRL register provides access to frequently used cursor functions, such as the display on/off control for the cursor, and the cursor number.

If a 32x32 cursor is selected, one of four 32x32 cursors can be enabled. The images each occupy one quarter of the image memory, with Cursor0 from location 0, followed by Cursor1 from address 0x100, Cursor2 from 0x200 and Cursor3 from 0x300. If a 64x64 cursor is selected only one cursor fits in the image buffer, and no selection is possible.

Similar frame synchronization rules apply to the cursor number as apply to the cursor coordinates. If CrsrFramesync is 1, the displayed cursor image is only changed during the vertical frame blanking period. If CrsrFrameSync is 0, the cursor image index is changed immediately, even if the cursor is currently being scanned.

Table 609. Cursor Control register (CRSR_CTRL, address 0x4000 8C00) bit description

Bit	Symbol	Description	Reset value
0	CRSRON	Cursor enable. 0 = Cursor is not displayed. 1 = Cursor is displayed.	0x0
3:1	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0x0
5:4	CRSRNUM1_0	Cursor image number. If the selected cursor size is 6x64, this field has no effect. If the selected cursor size is 32x32: 00 = Cursor0. 01 = Cursor1. 10 = Cursor2. 11 = Cursor3.	0x0
31:6	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	0x0

27.6.17 Cursor Configuration register

The CRSR_CFG register provides overall configuration information for the hardware cursor.

27.7.1.2 AMBA AHB master interface

The AHB master interface transfers display data from a selected slave (memory) to the LCD controller DMA FIFOs. It can be configured to obtain data from any on-chip SRAM on AHB, various types of off-chip static memory, or off-chip SDRAM.

In dual panel mode, the DMA FIFOs are filled up in an alternating fashion via a single DMA request. In single panel mode, the DMA FIFOs are filled up in a sequential fashion from a single DMA request.

The inherent AHB master interface state machine performs the following functions:

- Loads the upper panel base address into the AHB address incrementer on recognition of a new frame.
- Monitors both the upper and lower DMA FIFO levels and asserts a DMA request to request display data from memory, filling them to above the programmed watermark. the DMA request is reasserted when there are at least four locations available in either FIFO (dual panel mode).
- Checks for 1 kB boundaries during fixed-length bursts, appropriately adjusting the address in such occurrences.
- Generates the address sequences for fixed-length and undefined bursts.
- Controls the handshaking between the memory and DMA FIFOs. It inserts busy cycles if the FIFOs have not completed their synchronization and updating sequence.
- Fills up the DMA FIFOs, in dual panel mode, in an alternating fashion from a single DMA request.
- Asserts the a bus error interrupt if an error occurs during an active burst.
- Responds to retry commands by restarting the failed access. This introduces some busy cycles while it re-synchronizes.

27.7.2 Dual DMA FIFOs and associated control logic

The pixel data accessed from memory is buffered by two DMA FIFOs that can be independently controlled to cover single and dual-panel LCD types. Each FIFO is 16 words deep by 64 bits wide and can be cascaded to form an effective 32-Dword deep FIFO in single panel mode.

Synchronization logic transfers the pixel data from the AHB clock domain to the LCD controller clock domain. The water level marks in each FIFO are set such that each FIFO requests data when at least four locations become available.

An interrupt signal is asserted if an attempt is made to read either of the two DMA FIFOs when they are empty (an underflow condition has occurred).

27.7.3 Pixel serializer

This block reads the 32-bit wide LCD data from the output port of the DMA FIFO and extracts 24, 16, 8, 4, 2, or 1 bpp data, depending on the current mode of operation. The LCD controller supports big-endian, little-endian, and Windows CE data formats.

Depending on the mode of operation, the extracted data can be used to point to a color or gray scale value in the palette RAM or can actually be a true color value that can be directly applied to an LCD panel input.

Table 622. RGB mode data formats

FIFO data	24-bit RGB	16-bit (1:5:5:5 RGB)	16-bit (5:6:5 RGB)	16-bit (4:4:4 RGB)
31	-	p1 intensity bit	p1, Blue 4	-
30	-	p1, Blue 4	p1, Blue 3	-
29	-	p1, Blue 3	p1, Blue 2	-
28	-	p1, Blue 2	p1, Blue 1	-
27	-	p1, Blue 1	p1, Blue 0	p1, Blue 3
26	-	p1, Blue 0	p1, Green 5	p1, Blue 2
25	-	p1, Green 4	p1, Green 4	p1, Blue 1
24	-	p1, Green 3	p1, Green 3	p1, Blue 0
23	p0, Blue 7	p1, Green 2	p1, Green 2	p1, Green 3
22	p0, Blue 6	p1, Green 1	p1, Green 1	p1, Green 2
21	p0, Blue 5	p1, Green 0	p1, Green 0	p1, Green 1
20	p0, Blue 4	p1, Red 4	p1, Red 4	p1, Green 0
19	p0, Blue 3	p1, Red 3	p1, Red 3	p1, Red 3
18	p0, Blue 2	p1, Red 2	p1, Red 2	p1, Red 2
17	p0, Blue 1	p1, Red 1	p1, Red 1	p1, Red 1
16	p0, Blue 0	p1, Red 0	p1, Red 0	p1, Red 0
15	p0, Green 7	p0 intensity bit	p0, Blue 4	-
14	p0, Green 6	p0, Blue 4	p0, Blue 3	-
13	p0, Green 5	p0, Blue 3	p0, Blue 2	-
12	p0, Green 4	p0, Blue 2	p0, Blue 1	-
11	p0, Green 3	p0, Blue 1	p0, Blue 0	p0, Blue 3
10	p0, Green 2	p0, Blue 0	p0, Green 5	p0, Blue 2
9	p0, Green 1	p0, Green 4	p0, Green 4	p0, Blue 1
8	p0, Green 0	p0, Green 3	p0, Green 3	p0, Blue 0
7	p0, Red 7	p0, Green 2	p0, Green 2	p0, Green 3
6	p0, Red 6	p0, Green 1	p0, Green 1	p0, Green 2
5	p0, Red 5	p0, Green 0	p0, Green 0	p0, Green 1
4	p0, Red 4	p0, Red 4	p0, Red 4	p0, Green 0
3	p0, Red 3	p0, Red 3	p0, Red 3	p0, Red 3
2	p0, Red 2	p0, Red 2	p0, Red 2	p0, Red 2
1	p0, Red 1	p0, Red 1	p0, Red 1	p0, Red 1
0	p0, Red 0	p0, Red 0	p0, Red 0	p0, Red 0

27.7.4 RAM palette

The RAM-based palette is a 256 x 16 bit dual-port RAM physically structured as 128 x 32 bits. Two entries can be written into the palette from a single word write access. The Least Significant Bit (LSB) of the serialized pixel data selects between upper and lower halves of the palette RAM. The half that is selected depends on the byte ordering mode. In little-endian mode, setting the LSB selects the upper half, but in big-endian mode, the lower half of the palette is selected.

Table 855. USART Line Status Register Read Only (LSR - addresses 0x4008 1014 (USART0), 0x400C 1014 (USART2), 0x400C 2014 (USART3)) bit description

Bit	Symbol	Value	Description	Reset Value
0	RDR		Receiver Data Ready. LSR[0] is set when the RBR holds an unread character and is cleared when the USART RBR FIFO is empty.	0
		0	RBR is empty.	
		1	RBR contains valid data.	
1	OE		Overrun Error. The overrun error condition is set as soon as it occurs. A LSR read clears LSR[1]. LSR[1] is set when USART RSR has a new character assembled and the USART RBR FIFO is full. In this case, the USART RBR FIFO will not be overwritten and the character in the USART RSR will be lost.	0
		0	Overrun error status is inactive.	
		1	Overrun error status is active.	
2	PE		Parity Error. When the parity bit of a received character is in the wrong state, a parity error occurs. A LSR read clears LSR[2]. Time of parity error detection is dependent on FCR[0]. **Note:** A parity error is associated with the character at the top of the USART RBR FIFO.	0
		0	Parity error status is inactive.	
		1	Parity error status is active.	
3	FE		Framing Error. When the stop bit of a received character is a logic 0, a framing error occurs. A LSR read clears LSR[3]. The time of the framing error detection is dependent on FCR0. Upon detection of a framing error, the RX will attempt to re-synchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error. **Note:** A framing error is associated with the character at the top of the USART RBR FIFO.	0
		0	Framing error status is inactive.	
		1	Framing error status is active.	
4	BI		Break Interrupt. When RXD1 is held in the spacing state (all zeros) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RXD1 goes to marking state (all ones). A LSR read clears this status bit. The time of break detection is dependent on FCR[0]. **Note:** The break interrupt is associated with the character at the top of the USART RBR FIFO.	0
		0	Break interrupt status is inactive.	
		1	Break interrupt status is active.	

Table 864. USART RS485 Control register (RS485CTRL - addresses 0x4008 104C (USART0), 0x400C 104C (USART2), 0x400C 204C (USART3)) bit description *…continued*

Bit	Symbol	Value	Description	Reset value
3	-	-	Reserved.	-
4	DCTRL		Direction control for DIR pin.	0
		0	Disable Auto Direction Control.	
		1	Enable Auto Direction Control.	
5	OINV		Direction control pin polarity. This bit reverses the polarity of the direction control signal on the DIR pin.	0
		0	The direction control pin will be driven to logic ‘0’ when the transmitter has data to be sent. It will be driven to logic ‘1’ after the last bit of data has been transmitted.	
		1	The direction control pin will be driven to logic ‘1’ when the transmitter has data to be sent. It will be driven to logic ‘0’ after the last bit of data has been transmitted.	
31:6	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

After reset RS485 mode will be disabled. The RS485 feature allows the USART to be configured as one of multiple addressable slave receivers controlled by a single USART. In RS485 mode the USART differentiates between an address character and a data character by means of a ninth bit. The parity bit is used to implement this bit, and when set to ‘1’ indicates an address and when set to ‘0’ indicates data. RS485 mode is enabled by setting the NMMEN bit. The USART slave receiver can be assigned a unique address and, manually or automatically, reject or accept data based on a received address. See section Section 38.7.4 for details.

38.6.17 USART RS485 Address Match register

The RS485ADRMATCH register contains the address match value for RS-485/EIA-485 mode.

Table 865. USART RS485 Address Match register (RS485ADRMATCH - addresses 0x4008 1050 (USART0), 0x400C 1050 (USART2), 0x400C 2050 (USART3)) bit description

Bit	Symbol	Description	Reset value
7:0	ADRMATCH	Contains the address match value.	0x00
31:8	-	Reserved	-

The ADRMATCH bit field contains the slave address match value that is used to compare a received address value to. During automatic address detection, this value is used to accept or reject serial input data.

41.6 Register description

Table 909 shows the registers associated with the I2S interface and a summary of their functions. Following the table are details for each register.

Reset value reflects the data stored in used bits only. It does not include reserved bits content.

Table 909. Register overview: I2S0 (base address 0x400A 2000)

Name	Access	Address offset	Description	Reset value	Reference
DAO	R/W	0x000	I2S Digital Audio Output Register. Contains control bits for the I2S transmit channel.	0x87E1	Table 911
DAI	R/W	0x004	I2S Digital Audio Input Register. Contains control bits for the I2S receive channel.	0x07E1	Table 912
TXFIFO	WO	0x008	I2S Transmit FIFO. Access register for the 8 x 32-bit transmitter FIFO.	0	Table 913
RXFIFO	RO	0x00C	I2S Receive FIFO. Access register for the 8 x 32-bit receiver FIFO.	0	Table 914
STATE	RO	0x010	I2S Status Feedback Register. Contains status information about the I2S interface.	0x7	Table 915
DMA1	R/W	0x014	I2S DMA Configuration Register 1. Contains control information for DMA request 1.	0	Table 916
DMA2	R/W	0x018	I2S DMA Configuration Register 2. Contains control information for DMA request 2.	0	Table 917
IRQ	R/W	0x01C	I2S Interrupt Request Control Register. Contains bits that control how the I2S interrupt request is generated.	0	Table 918
TXRATE	R/W	0x020	I2S Transmit MCLK divider. This register determines the I2S TX MCLK rate by specifying the value to divide PCLK by in order to produce MCLK.	0	Table 919
RXRATE	R/W	0x024	I2S Receive MCLK divider. This register determines the I2S RX MCLK rate by specifying the value to divide PCLK by in order to produce MCLK.	0	Table 920
TXBITRATE	R/W	0x028	I2S Transmit bit rate divider. This register determines the I2S transmit bit rate by specifying the value to divide TX_MCLK by in order to produce the transmit bit clock.	0	Table 921
RXBITRATE	R/W	0x02C	I2S Receive bit rate divider. This register determines the I2S receive bit rate by specifying the value to divide RX_MCLK by in order to produce the receive bit clock.	0	Table 922
TXMODE	R/W	0x030	I2S Transmit mode control.	0	Table 923
RXMODE	R/W	0x034	I2S Receive mode control.	0	Table 924

Table 966. Slave Receiver mode

Status Code (STAT)	Status of the I^2C-bus and hardware	Application software response					Next action taken by I^2C hardware
		To/From DAT	To CON				
			STA	STO	SI	AA	
0x60	Own SLA+W has been received; ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x68	Arbitration lost in SLA+R/W as master; Own SLA+W has been received, ACK returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x70	General call address (0x00) has been received; ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x78	Arbitration lost in SLA+R/W as master; General call address has been received, ACK has been returned.	No DAT action or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		No DAT action	X	0	0	1	Data byte will be received and ACK will be returned.
0x80	Previously addressed with own SLV address; DATA has been received; ACK has been returned.	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.
0x88	Previously addressed with own SLA; DATA byte has been received; NOT ACK has been returned.	Read data byte or	0	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address.
		Read data byte or	0	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1.
		Read data byte or	1	0	0	0	Switched to not addressed SLV mode; no recognition of own SLA or General call address. A START condition will be transmitted when the bus becomes free.
		Read data byte	1	0	0	1	Switched to not addressed SLV mode; Own SLA will be recognized; General call address will be recognized if ADR[0] = logic 1. A START condition will be transmitted when the bus becomes free.
0x90	Previously addressed with General Call; DATA byte has been received; ACK has been returned.	Read data byte or	X	0	0	0	Data byte will be received and NOT ACK will be returned.
		Read data byte	X	0	0	1	Data byte will be received and ACK will be returned.

Table 991. CAN message interface command mask 2 registers (IF2_MSK2, 0x400E 208C (C_CAN0) and 0x400A 408C (C_CAN1)) bit description

Bit	Symbol	Value	Description	Reset value	Access
12:0	MSK28_16		Identifier mask 0 = The corresponding bit in the identifier of the message can not inhibit the match in the acceptance filtering. 1 = The corresponding identifier bit is used for acceptance filtering.	0xFFF	R/W
13	-		Reserved	1	-
14	MDIR		Mask message direction	1	R/W
		0	The message direction bit (DIR) has no effect on acceptance filtering.		
		1	The message direction bit (DIR) is used for acceptance filtering.		
15	MXTD		Mask extend identifier	1	R/W
		0	The extended identifier bit (IDE) has no effect on acceptance filtering.		
		1	The extended identifier bit (IDE) is used for acceptance filtering.		
31:16	-	-	Reserved	0	-

43.6.2.4.3 CAN message interface command arbitration 1 registers

Table 992. CAN message interface command arbitration 1 registers (IF1_ARB1, address 0x400E 2030 (C_CAN0) and 0x400A 4030 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	ID15_0	Message identifier 29-bit identifier (“extended frame”) 11-bit identifier (“standard frame”)	0x00	R/W
31:16	-	Reserved	0	-

Table 993. CAN message interface command arbitration 1 registers (IF2_ARB1, address 0x400E 2090 (C_CAN0) and 0x400A 4090 (C_CAN1)) bit description

Bit	Symbol	Description	Reset value	Access
15:0	ID15_0	Message identifier 29-bit identifier (“extended frame”) 11-bit identifier (“standard frame”)	0x00	R/W
31:16	-	Reserved	0	-