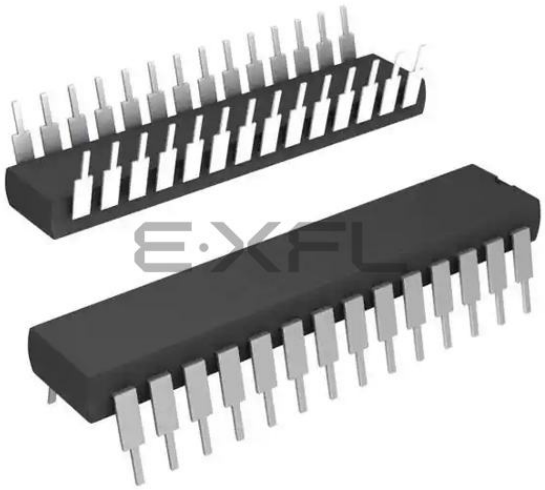

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0412pj020sg

Introduction

Zilog's Z8 Encore! XP® MCU product family is a line of Zilog microcontrollers based on the 8-bit eZ8 CPU. Z8 Encore! XP® F0822 Series of MCUs adds Flash memory to Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming allows faster development time and program changes in the field. The new eZ8 CPU is upward-compatible with the existing Z8® CPU instructions. The rich peripheral set of the Z8 Encore! XP® F0822 Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices and sensors.

Features

The Z8 Encore! XP® F0822 Series features:

- 20MHz eZ8 CPU core
- Up to 8KB Flash with in-circuit programming capability
- 1KB Register RAM
- Optional 2- to 5-channel, 10-bit Analog-to-Digital Converter (ADC)
- Full-duplex 9-bit Universal Asynchronous Receiver/Transmitter (UART) with bus transceiver Driver Enable Control
- Inter-Integrated Circuit (I^2C)
- Serial Peripheral Interface (SPI)
- Infrared Data Association (IrDA)-compliant infrared encoder/decoders
- Two 16-bit timers with Capture, Compare, and PWM capability
- Watchdog Timer (WDT) with internal RC oscillator
- 11 to 19 Input/Output pins depending upon package
- Up to 19 interrupts with configurable priority
- On-Chip Debugger (OCD)
- Voltage Brown-Out (VBO) protection
- Power-On Reset (POR)
- Crystal oscillator with three power settings and RC oscillator option
- 2.7V to 3.6V operating voltage with 5V-tolerant inputs
- 20-pin and 28-pin packages

Address Space

The eZ8 CPU accesses three distinct address spaces:

- The Register File contains addresses for the general-purpose registers and the eZ8 CPU, Peripheral, and GPIO Port Control registers
- The Program Memory contains addresses for all memory locations having executable code and/or data
- The Data Memory contains addresses for all memory locations that hold data only

These three address spaces are covered briefly in the following sections. For more information about the eZ8 CPU and its address space, refer to the eZ8 CPU Core User Manual (UM0128), which is available for download at www.zilog.com.

Register File

The Register File address space in the Z8 Encore! XP® F0822 Series is 4KB (4096 bytes). It is composed of two sections: Control registers and General-Purpose registers. When instructions are executed, registers are read from when defined as sources and written to when defined as destinations. The architecture of the eZ8 CPU allows all general-purpose registers to function as accumulators, address pointers, index registers, stack areas, or scratch pad memory.

The upper 256 bytes of the 1KB Register File address space is reserved for control of the eZ8 CPU, the on-chip peripherals, and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256-byte Control Register section is reserved (unavailable). Reading from the reserved Register File addresses returns an undefined value. Writing to reserved Register File addresses is not recommended by Zilog because it can produce unpredictable results.

The on-chip RAM always begins at address 000H in the Register File address space. Z8 Encore! XP® F0822 Series contains 1KB of on-chip RAM. Reading from Register File addresses outside the available RAM addresses (and not within the control register address space) returns an undefined value. Writing to these Register File addresses produces no effect.

voltage threshold (V_{POR}), the POR Counter is enabled and counts 66 cycles of the WDT oscillator. After the POR counter times out, the XTAL Counter is enabled to count a total of 16 system clock pulses. The device is held in the Reset state until both the POR Counter and XTAL counter have timed out. After the Z8 Encore! XP® F0822 Series device exits the POR state, the eZ8 CPU fetches the Reset vector. Following POR, the POR status bit in the Watchdog Timer Control Register (WDTCTL) is set to 1.

Figure 6 displays POR operation. See the Electrical Characteristics chapter on page 176 for the POR threshold voltage (V_{POR}).

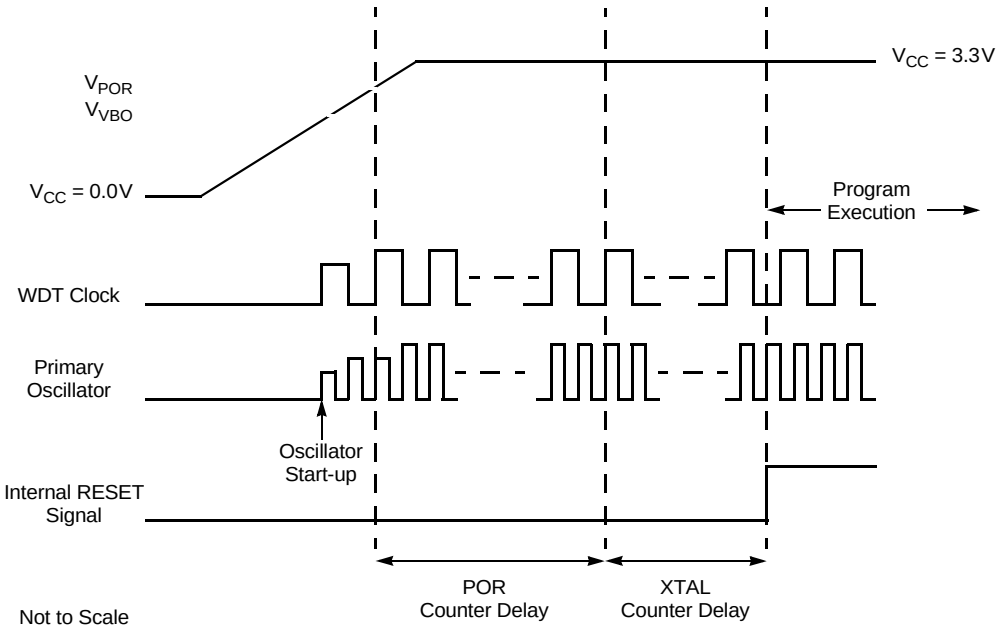

Figure 6. Power-On Reset Operation

Voltage Brown-Out Reset

The devices in Z8 Encore! XP® F0822 Series provides low-voltage brown-out protection. The VBO circuit senses when the supply voltage drops to an unsafe level (below the VBO threshold voltage) and forces the device into the Reset state. While the supply voltage remains below the POR voltage threshold (V_{POR}), the VBO block holds the device in the Reset state.

After the supply voltage again exceeds the POR voltage threshold, the device progresses through a full System Reset sequence as described in the POR section. Following POR,

the POR status bit in the Watchdog Timer Control Register (WDTCTL) is set to 1. Figure 7 displays the VBO operation. See the Electrical Characteristics chapter on page 176 for the VBO and POR threshold voltages (V_{VBO} and V_{POR}).

The VBO circuit can be either enabled or disabled during STOP Mode. Operation during STOP Mode is set by the VBO_AO option bit. For information about configuring VBO_AO, see the Option Bits chapter on page 155.

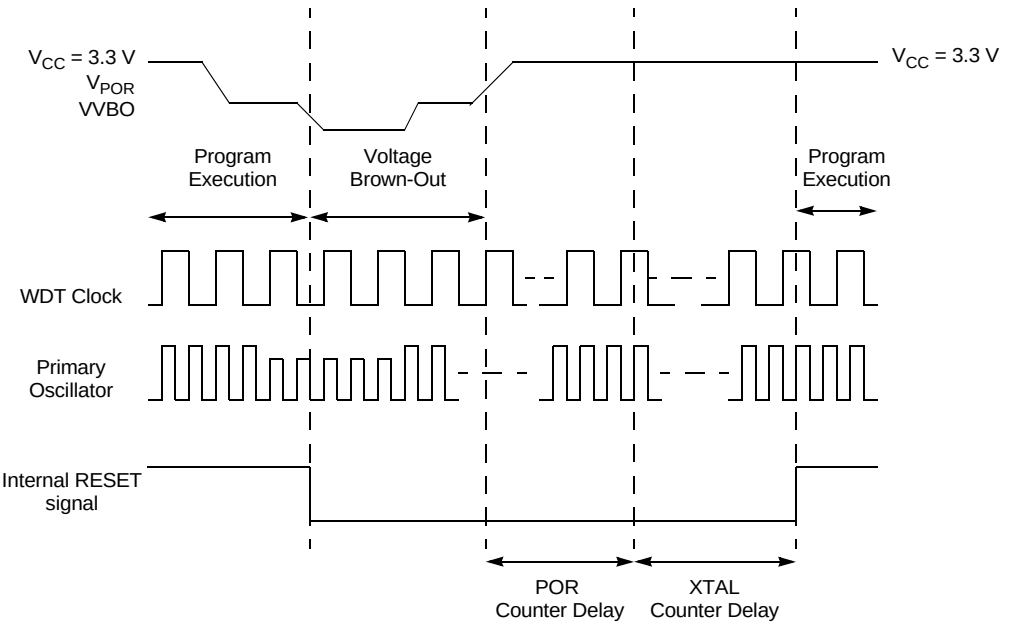

Figure 7. Voltage Brown-Out Reset Operation

Watchdog Timer Reset

If the device is in NORMAL or HALT Mode, WDT initiates a System Reset at time-out, if the WDT_RES option bit is set to 1. This setting is the default (unprogrammed) setting of the WDT_RES option bit. The WDT status bit in the WDT Control Register is set to signify that the reset was initiated by the WDT.

External Pin Reset

The $\overline{\text{RESET}}$ pin contains a Schmitt-triggered input, an internal pull-up, an analog filter, and a digital filter to reject noise. After the $\overline{\text{RESET}}$ pin is asserted for at least 4 system

Low-Power Modes

Z8 Encore! XP® F0822 Series products contain power-saving features. The highest level of power reduction is provided by STOP Mode. The next level of power reduction is provided by the HALT Mode.

STOP Mode

Execution of the eZ8 CPU's stop instruction places the device into STOP Mode. In STOP Mode, the operating characteristics are:

- Primary crystal oscillator is stopped; the X_{IN} pin is driven High and the X_{OUT} pin is driven Low
- System clock is stopped
- eZ8 CPU is stopped
- Program counter (PC) stops incrementing
- If enabled for operation in STOP Mode, the WDT and its internal RC oscillator continue to operate
- If enabled for operation in STOP Mode through the associated option bit, the VBO protection circuit continues to operate
- All other on-chip peripherals are idle

To minimize current in STOP Mode, WDT must be disabled and all GPIO pins configured as digital inputs must be driven to one of the supply rails (V_{CC} or GND). The device can be brought out of STOP Mode using Stop Mode Recovery. For more information about Stop Mode Recovery, see the Reset and Stop Mode Recovery chapter on page 21.

! **Caution:** STOP Mode must not be used when driving the Z8F082x family devices with an external clock driver source.

HALT Mode

Execution of the eZ8 CPU's HALT instruction places the device into HALT Mode. In HALT Mode, the operating characteristics are:

- Primary crystal oscillator is enabled and continues to operate

Table 24. Interrupt Vectors in Order of Priority

Priority	Program Memory Vector Address	Interrupt Source
Highest	0002H	Reset (not an interrupt)
	0004H	WDT (see the Watchdog Timer chapter on page 70)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	I^2C
	0014H	SPI
	0016H	ADC
	0018H	Port A7, rising or falling input edge
	001AH	Port A6, rising or falling input edge
	001CH	Port A5, rising or falling input edge
	001EH	Port A4, rising or falling input edge
	0020H	Port A3, rising or falling input edge
	0022H	Port A2, rising or falling input edge
	0024H	Port A1, rising or falling input edge
	0026H	Port A0, rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C3, both input edges
	0032H	Port C2, both input edges
	0034H	Port C1, both input edges
Lowest	0036H	Port C0, both input edges

- Writing a 1 to the IRQE bit in the Interrupt Control Register

Interrupts are globally disabled by any of the following actions:

- Execution of a Disable Interrupt (DI) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the interrupt controller
- Writing a 0 to the IRQE bit in the Interrupt Control Register
- Reset
- Execution of a trap instruction
- Illegal instruction trap

Interrupt Vectors and Priority

The interrupt controller supports three levels of interrupt priority. Level 3 is the highest priority, Level 2 is the second highest priority, and Level 1 is the lowest priority. If all of the interrupts were enabled with identical interrupt priority (all as Level 2 interrupts), then interrupt priority would be assigned from highest to lowest as specified in Table 24. Level 3 interrupts always have higher priority than Level 2 interrupts which in turn always have higher priority than Level 1 interrupts. Within each interrupt priority level (Level 1, Level 2, or Level 3), priority is assigned as specified in Table 24. A Reset, WDT interrupt (if enabled), and an Illegal Instruction Trap will always have the highest priority.

Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the Interrupt Request Register is cleared until the next interrupt occurs. Writing a 0 to the corresponding bit in the Interrupt Request Register likewise clears the interrupt request.

Caution: Zilog recommends not using a coding style that clears bits in the Interrupt Request registers. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost. See Example 1, which follows.

Example 1. A poor coding style that can result in lost interrupt requests:

```
LDX r0, IRQ0
AND r0, MASK
LDX IRQ0, r0
```

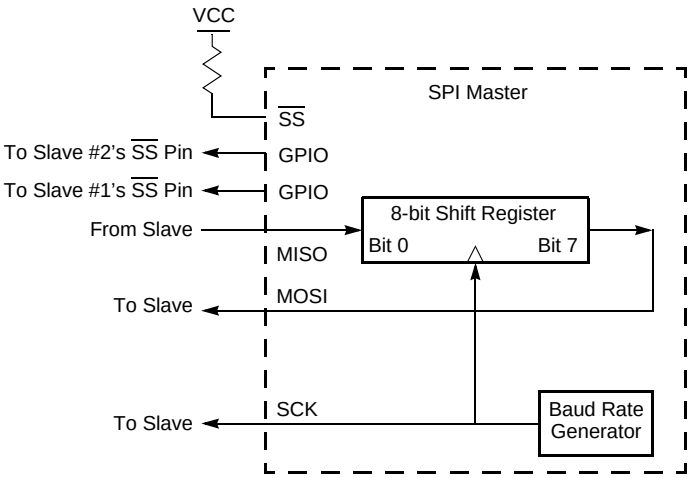

Figure 21. SPI Configured as a Master in a Single Master, Multiple Slave System

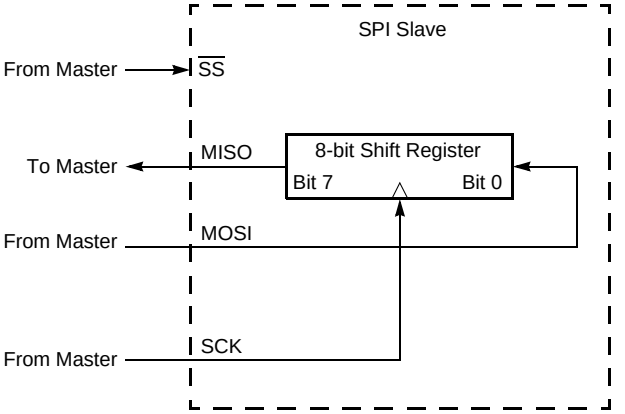

Figure 22. SPI Configured as a Slave

SPI Control Register

The SPI Control Register, shown in Table 65, configures the SPI for transmit and receive operations.

Table 65. SPI Control Register (SPICTL)

Bit	7	6	5	4	3	2	1	0
Field	IRQE	STR	BIRQ	PHASE	CLKPOL	WOR	MMEN	SPIEN
RESET	0							
R/W	R/W							
Address	F61H							

Bit	Description
[7] IRQE	**Interrupt Request Enable** 0 = SPI interrupts are disabled. No interrupt requests are sent to the Interrupt Controller. 1 = SPI interrupts are enabled. Interrupt requests are sent to the Interrupt Controller.
[6] STR	**Start an SPI Interrupt Request** 0 = No effect. 1 = Setting this bit to 1 also sets the IRQ bit in the SPI Status Register to 1. Setting this bit forces the SPI to send an interrupt request to the Interrupt Control. This bit can be used by software for a function similar to transmit buffer empty in a UART. Writing a 1 to the IRQ bit in the SPI Status Register clears this bit to 0.
[5] BIRQ	**BRG Timer Interrupt Request** If the SPI is enabled, this bit has no effect. If the SPI is disabled: 0 = BRG timer function is disabled. 1 = BRG timer function and time-out interrupt are enabled.
[4] PHASE	**Phase Select** Sets the phase relationship of the data to the clock. For more information about operation of the PHASE bit, see the SPI Clock Phase and Polarity Control section on page 104.
[3] CLKPOL	**Clock Polarity** 0 = SCK idles Low (0). 1 = SCK idle High (1).
[2] WOR	**Wire-OR (Open-Drain) Mode Enabled** 0 = SPI signal pins not configured for open-drain. 1 = All four SPI signal pins (SCK, $\overline{SS}$, MISO, MOSI) configured for open-drain function. This setting is typically used for multimaster and/or multislave configurations.
[1] MMEN	**SPI MASTER Mode Enable** 0 = SPI configured in SLAVE Mode. 1 = SPI configured in MASTER Mode.
[0] SPIEN	**SPI Enable** 0 = SPI disabled. 1 = SPI enabled.

Option Bits

Option bits allow user configuration of certain aspects of Z8 Encore! XP® F0822 Series operation. The feature configuration data is stored in Flash memory and read during Reset. Features available for control through the option bits are:

- Watchdog Timer time-out response selection–interrupt or Reset
- Watchdog Timer enabled at Reset
- The ability to prevent unwanted read access to user code in Flash memory
- The ability to prevent accidental programming and erasure of all or a portion of the user code in Flash memory
- Voltage Brown-Out configuration is always enabled or disabled during STOP Mode to reduce STOP Mode power consumption
- Oscillator Mode selection for high-, medium- and low-power crystal oscillators, or external RC oscillator

Operation

This section describes the type and configuration of the programmable Flash option bits.

Option Bit Configuration By Reset

During any reset operation (System Reset, Reset or Stop Mode Recovery), the option bits are automatically read from Flash memory and written to Option Configuration registers. The Option Configuration registers control operation of the devices within the Z8 Encore! XP® F0822 Series. Option bit control is established before the device exits Reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the Register File and are not accessible for read or write access. Each time the option bits are programmed or erased, the device must be Reset for the change to take place (Flash version only).

Option Bit Address Space

The first two bytes of Flash memory at addresses 0000H (shown in Table 90) and 0001H (shown in Table 91) are reserved for the user-programmable option bits. The byte at Program memory address 0000H configures user options. The byte at Flash memory address 0001H is reserved for future use and must remain in its unprogrammed state.

OCD Status Register

The OCD Status Register, shown in Table 95, reports status information about the current state of the debugger and the system.

Table 95. OCD Status Register (OCDSTAT)

Bit	7	6	5	4	3	2	1	0
Field	IDLE	HALT	RPEN	Reserved				
RESET	0							
R/W	R							

Bit	Description
[7] IDLE	**CPU Idling** This bit is set if the part is in DEBUG Mode (DBGMODE is 1), or if a BRK instruction occurred since the last time OCDCTL was written. This can be used to determine if the CPU is running or if it is idling. 0 = The eZ8 CPU is running. 1 = The eZ8 CPU is either stopped or looping on a BRK instruction.
[6] HALT	**HALT Mode** 0 = The device is not in HALT Mode. 1 = The device is in HALT Mode.
[5] RPEN	**Read Protect Option Bit Enabled** 0 = The Read Protect option bit is disabled (1). 1 = The Read Protect option bit is enabled (0), disabling many OCD commands.
[4:0]	**Reserved** These bits are reserved and must be programmed to 00000.

Figure 46 displays the maximum current consumption in STOP Mode with the VBO disabled and Watchdog Timer enabled plotted opposite the power supply voltage. All GPIO pins are configured as outputs and driven High. Disabling the Watchdog Timer and its internal RC oscillator in STOP Mode will provide some additional reduction in STOP Mode current consumption. This small current reduction is indistinquishable on the scale of Figure 46.

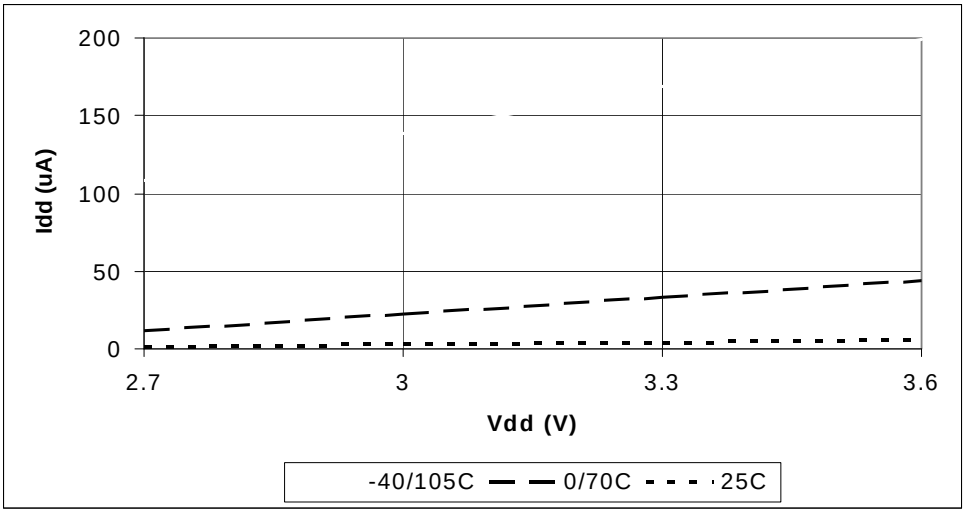

Figure 46. Maximum STOP Mode I_{DD} with VBO Disabled vs. Power Supply Voltage

Table 101 provides information about the external RC oscillator electrical characteristics and timing, and Table 102 provides information about the Flash memory electrical characteristics and timing.

Table 101. External RC Oscillator Electrical Characteristics and Timing

		T_A = –40°C to 105°C				
Symbol	**Parameter**	**Minimum**	**Typical***	**Maximum**	**Units**	**Conditions**
V_{DD}	Operating Voltage Range	2.70	–	–	V	
R_{EXT}	External Resistance from X_{IN} to V_{DD}	40	45	200	kΩ	
C_{EXT}	External Capacitance from X_{IN} to V_{SS}	0	20	1000	pF	
F_{OSC}	External RC Oscillation Frequency	–	–	4	MHz	

Note: *When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7V, but before the power supply drops to the voltage brown-out threshold. The oscillator will resume oscillation as soon as the supply voltage exceeds 2.7V.

Table 102. Flash Memory Electrical Characteristics and Timing

	V_{DD} = 2.7–3.6V T_A = –40°C to 105°C				
Parameter	**Minimum**	**Typical**	**Maximum**	**Units**	**Notes**
Flash Byte Read Time	50	–	–	µs	
Flash Byte Program Time	20	–	40	µs	
Flash Page Erase Time	10	–	–	ms	
Flash Mass Erase Time	200	–	–	ms	
Writes to Single Address Before Next Erase	–	–	2		
Flash Row Program Time	–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	–	–	years	25°C
Endurance	10,000	–	–	cycles	Program/erase cycles

Table 105 lists ADC electrical characteristics and timing data.

Table 105. Analog-to-Digital Converter Electrical Characteristics and Timing

		V_{DD} = 3.0–3.6 V T_A = –40°C to 105°C				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
	Resolution	10	–	–	bits	External V_{REF} = 3.0V
	Differential Nonlinearity (DNL)	–0.25	–	0.25	lsb	Guaranteed by design
	Integral Nonlinearity (INL)	–2.0	–	2.0	lsb	External V_{REF} = 3.0V
	DC Offset Error	–35	–	25	mV	80-pin QFP and 64-pin LQFP packages.
V_{REF}	Internal Reference Voltage	1.9	2.0	2.4	V	V_{DD} = 3.0–3.6V T_A = –40°C to 105°C
VC_{REF}	Voltage Coefficient of Internal Reference Voltage	–	78	–	mV/V	V_{REF} variation as a function of AV_{DD}.
TC_{REF}	Temperature Coefficient of Internal Reference Voltage	–	1	–	mV/°C	
	Single-Shot Conversion Period		5129		cycles	System clock cycles
	Continuous Conversion Period		256		cycles	System clock cycles
R_S	Analog Source Impedance	–	–	150	Ω	Recommended
Zin	Input Impedance		150		KΩ	20MHz system clock. Input impedance increases with lower system clock frequency.
V_{REF}	External Reference Voltage			AV_{DD}	V	AV_{DD} <= V_{DD}. When using an external reference voltage, decoupling capacitance should be placed from V_{REF} to AV_{SS}.
I_{REF}	Current draw into V_{REF} pin when driving with external source.		25.0	40.0	µA	

General Purpose I/O Port Input Data Sample Timing

Figure 48 displays timing of the GPIO Port input sampling. Table 106 lists the GPIO port input timing.

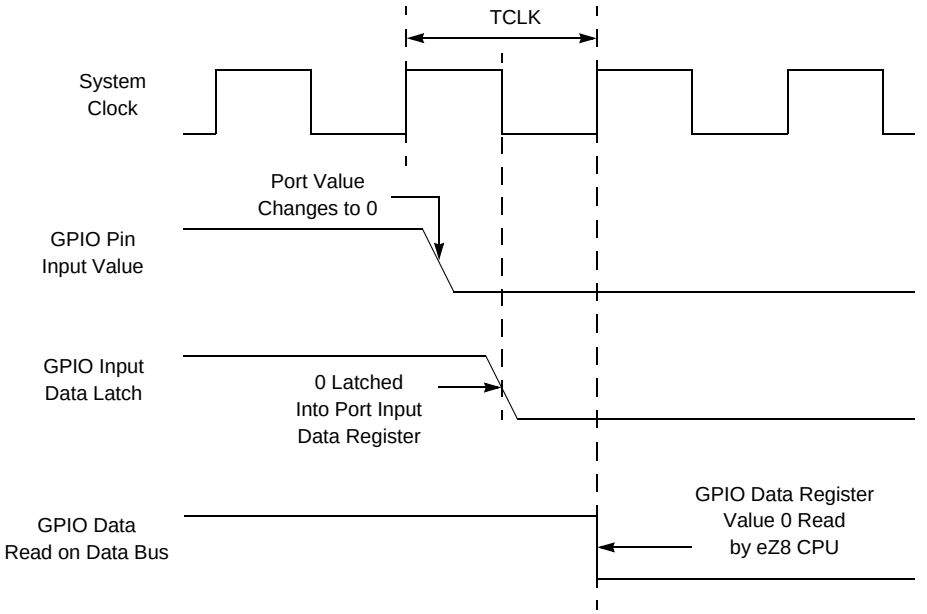

Figure 48. Port Input Sample Timing

Table 106. GPIO Port Input Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
T_{S_PORT}	Port Input Transition to X_{IN} Fall Setup Time (not pictured)	5	–
T_{H_PORT}	X_{IN} Fall to Port Input Transition Hold Time (not pictured)	5	–
T_{SMR}	GPIO Port Pin Pulse Width to Insure Stop Mode Recovery (for GPIO port pins enabled as SMR sources)	1µs	

SPI MASTER Mode Timing

Figure 51 and Table 109 provide timing information for SPI MASTER Mode pins. Timing is shown with SCK rising edge used to source MOSI output data, SCK falling edge used to sample MISO input data. Timing on the SS output pin(s) is controlled by software.

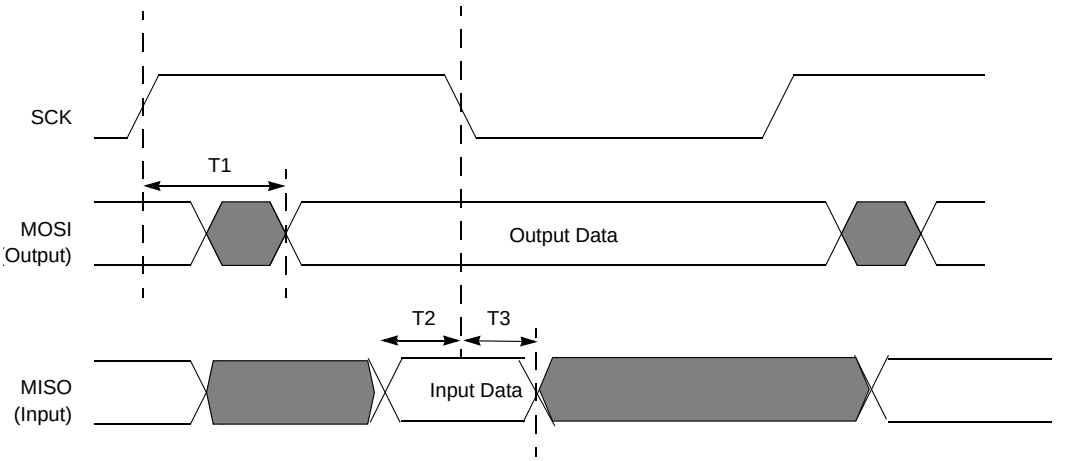

Figure 51. SPI MASTER Mode Timing

Table 109. SPI MASTER Mode Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
SPI MASTER			
T_1	SCK Rise to MOSI output Valid Delay	–5	+5
T_2	MISO input to SCK (receive edge) Setup Time	20	
T_3	MISO input to SCK (receive edge) Hold Time	0	

SPI SLAVE Mode Timing

Figure 52 and Table 110 provide timing information for the SPI SLAVE Mode pins. Timing is shown with SCK rising edge used to source MISO output data, SCK falling edge used to sample MOSI input data.

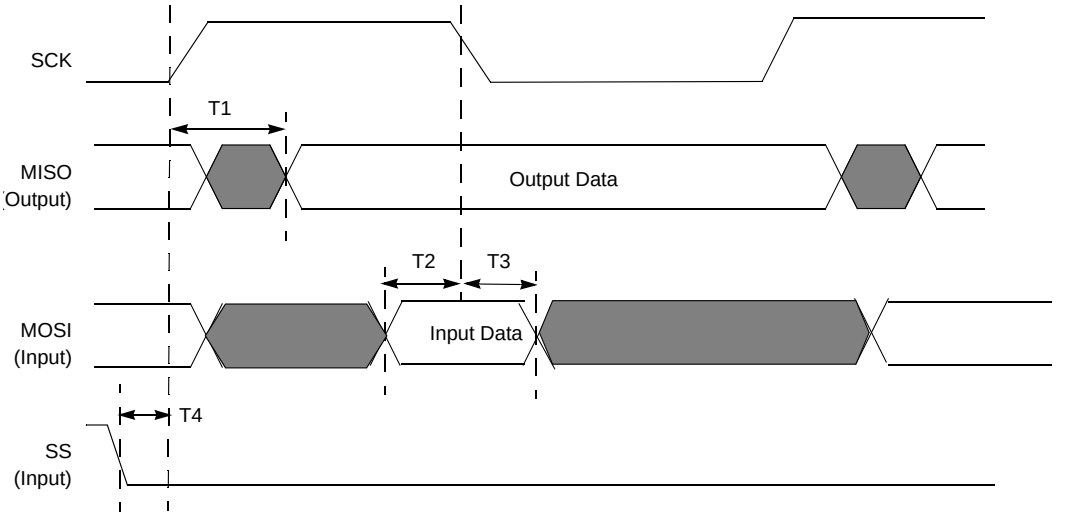

Figure 52. SPI SLAVE Mode Timing

Table 110. SPI SLAVE Mode Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
SPI SLAVE			
T_1	SCK (transmit edge) to MISO output Valid Delay	2 * X_{IN} period	3 * X_{IN} period + 20ns
T_2	MOSI input to SCK (receive edge) Setup Time	0	
T_3	MOSI input to SCK (receive edge) Hold Time	3 * X_{IN} period	
T_4	SS input assertion to SCK setup	1 * X_{IN} period	

I²C Timing

Figure 53 and Table 111 provide timing information for I²C pins.

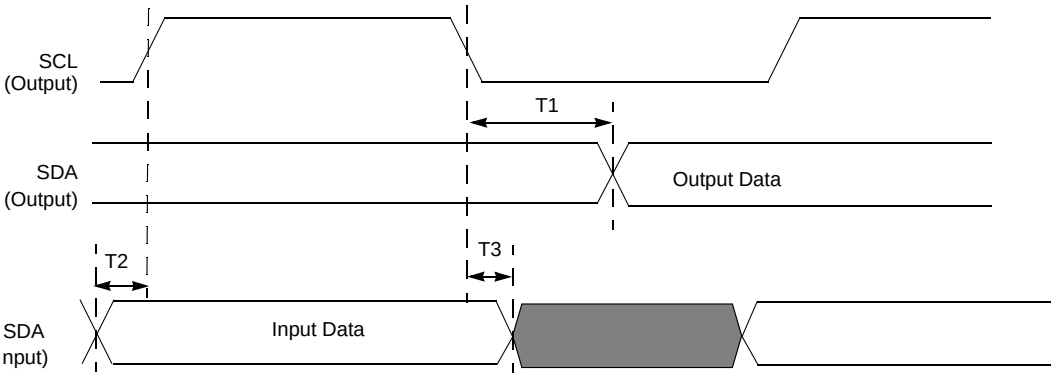

Figure 53. I²C Timing

Table 111. I²C Timing

		Delay (ns)	
Parameter	**Abbreviation**	**Minimum**	**Maximum**
I²C			
T_1	SCL Fall to SDA output delay	SCL period/4	
T_2	SDA Input to SCL rising edge Setup Time	0	
T_3	SDA Input to SCL falling edge Hold Time	0	

Hex Address: FC5

Table 177. IRQ1 Enable Low Bit Register (IRQ1ENL)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENL	PA6ENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0							
R/W	R/W							
Address	FC5H							

Hex Address: FC6

Table 178. Interrupt Request 2 Register (IRQ2)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				PC3I	PC2I	PC1I	PC0I
RESET	0							
R/W	R/W							
Address	FC6H							

Hex Address: FC7

Table 179. IRQ2 Enable High Bit Register (IRQ2ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENH	C2ENH	C1ENH	C0ENH
RESET	0							
R/W	R/W							
Address	FC7H							

Hex Address: FC8

Table 180. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENL	C2ENL	C1ENL	C0ENL
RESET	0							
R/W	R/W							
Address	FC8H							

G

H

I