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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 2x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0421hh020sg

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Table 7. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
UART 0				
F40	UART0 Transmit Data	U0TXD	XX	88
	UART0 Receive Data	U0RXD	XX	89
F41	UART0 Status 0	U0STAT0	0000011Xb	90
F42	UART0 Control 0	U0CTL0	00	92
F43	UART0 Control 1	U0CTL1	00	92
F44	UART0 Status 1	U0STAT1	00	90
F45	UART0 Address Compare Register	U0ADDR	00	94
F46	UART0 Baud Rate High Byte	U0BRH	FF	95
F47	UART0 Baud Rate Low Byte	U0BRL	FF	95
F48–F4F	Reserved	—	XX	
I^2C				
F50	I^2C Data	I2CDATA	00	129
F51	I^2C Status	I2CSTAT	80	129
F52	I^2C Control	I2CCTL	00	131
F53	I^2C Baud Rate High Byte	I2CBRH	FF	132
F54	I^2C Baud Rate Low Byte	I2CBRL	FF	132
F55	I^2C Diagnostic State	I2CDST	XX000000b	133
F56	I^2C Diagnostic Control	I2CDIAG	00	135
F57–F5F	Reserved	—	XX	
Serial Peripheral Interface (SPI) Unavailable in 20-Pin Package Devices				
F60	SPI Data	SPIDATA	01	109
F61	SPI Control	SPICTL	00	110
F62	SPI Status	SPISTAT	00	111
F63	SPI Mode	SPIMODE	00	112
F64	SPI Diagnostic State	SPIDST	00	113
F65	Reserved	—	XX	
F66	SPI Baud Rate High Byte	SPIBRH	FF	114
F67	SPI Baud Rate Low Byte	SPIBRL	FF	114
F68–F6F	Reserved	—	XX	

Note: XX = undefined.

Table 24. Interrupt Vectors in Order of Priority

Priority	Program Memory Vector Address	Interrupt Source
Highest	0002H	Reset (not an interrupt)
	0004H	WDT (see the Watchdog Timer chapter on page 70)
	0006H	Illegal Instruction Trap (not an interrupt)
	0008H	Reserved
	000AH	Timer 1
	000CH	Timer 0
	000EH	UART 0 receiver
	0010H	UART 0 transmitter
	0012H	I^2C
	0014H	SPI
	0016H	ADC
	0018H	Port A7, rising or falling input edge
	001AH	Port A6, rising or falling input edge
	001CH	Port A5, rising or falling input edge
	001EH	Port A4, rising or falling input edge
	0020H	Port A3, rising or falling input edge
	0022H	Port A2, rising or falling input edge
	0024H	Port A1, rising or falling input edge
	0026H	Port A0, rising or falling input edge
	0028H	Reserved
	002AH	Reserved
	002CH	Reserved
	002EH	Reserved
	0030H	Port C3, both input edges
	0032H	Port C2, both input edges
	0034H	Port C1, both input edges
Lowest	0036H	Port C0, both input edges

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, the ONE-SHOT Mode equation is used to determine the first PWM time-out period.

If TPOL is set to 0, the ratio of the PWM output High time to the total period is calculated using the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output High time to the total period is calculated using the following equation:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

CAPTURE Mode

In CAPTURE Mode, the current timer count value is recorded when the appropriate external Timer Input transition occurs. The capture count value is written to the Timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines if the Capture occurs on a rising edge or a falling edge of the Timer Input signal. When the capture event occurs, an interrupt is generated and the timer continues counting.

The timer continues counting up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt and continues counting.

Observe the following procedure for configuring a timer for CAPTURE Mode and initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for CAPTURE Mode
   - Set the prescale value
   - Set the Capture edge (rising or falling) for the Timer Input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Clear the Timer PWM High and Low Byte registers to 0000H. This allows user software to determine if interrupts were generated by either a capture event or a reload. If

Bit	Description (Continued)
[2] BRGCTL	**Baud Rate Control** This bit causes different UART behavior depending on whether the UART receiver is enabled (REN = 1 in the UART Control 0 Register). When the UART receiver is not enabled, this bit determines whether the BRG will issue interrupts. 0 = Reads from the Baud Rate High and Low Byte registers return the BRG reload value 1 = The BRG generates a receive interrupt when it counts down to zero. Reads from the Baud Rate High and Low Byte registers return the current BRG count value. When the UART receiver is enabled, this bit allows reads from the Baud Rate registers to return the BRG count value instead of the reload value. 0 = Reads from the Baud Rate High and Low Byte registers return the BRG reload value. 1 = Reads from the Baud Rate High and Low Byte registers return the current BRG count value. Unlike the Timers, there is no mechanism to latch the High Byte when the Low Byte is read.
[1] RDAIRQ	**Receive Data Interrupt Enable** 0 = Received data and receiver errors generates an interrupt request to the Interrupt Controller. 1 = Received data does not generate an interrupt request to the Interrupt Controller. Only receiver errors generate an interrupt request.
[0] IREN	**Infrared Encoder/Decoder Enable** 0 = Infrared Encoder/Decoder is disabled. UART operates normally operation. 1 = Infrared Encoder/Decoder is enabled. The UART transmits and receives data through the Infrared Encoder/Decoder.

UART Address Compare Register

The UART Address Compare Register, shown in Table 59, stores the multinode network address of the UART. When the MPMD[1] bit of UART Control Register 0 is set, all incoming address bytes will be compared to the value stored in the Address Compare Register. Receive interrupts and RDA assertions will only occur in the event of a match.

Table 59. UART Address Compare Register (U0ADDR)

Bit	7	6	5	4	3	2	1	0
Field	COMP_ADDR							
RESET	0							
R/W	R/W							
Address	F45H							

Bit	Description
[7:0] COMP_ADDR	**Compare Address** This 8-bit value is compared to the incoming address bytes.

For reliable communication, the UART baud rate error must never exceed 5 percent. Table 62 provides information about data rate errors for popular baud rates and commonly used crystal oscillator frequencies.

Table 62. UART Baud Rates

10.0 MHz System Clock				5.5296 MHz System Clock			
Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	1	625.0	0.00	625.0	N/A	N/A	N/A
250.0	3	208.33	–16.67	250.0	1	345.6	38.24
115.2	5	125.0	8.51	115.2	3	115.2	0.00
57.6	11	56.8	–1.36	57.6	6	57.6	0.00
38.4	16	39.1	1.73	38.4	9	38.4	0.00
19.2	33	18.9	0.16	19.2	18	19.2	0.00
9.60	65	9.62	0.16	9.60	36	9.60	0.00
4.80	130	4.81	0.16	4.80	72	4.80	0.00
2.40	260	2.40	–0.03	2.40	144	2.40	0.00
1.20	521	1.20	–0.03	1.20	288	1.20	0.00
0.60	1042	0.60	–0.03	0.60	576	0.60	0.00
0.30	2083	0.30	0.2	0.30	1152	0.30	0.00
3.579545 MHz System Clock				**1.8432 MHz System Clock**			
Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)	Desired Rate (kHz)	BRG Divisor (Decimal)	Actual Rate (kHz)	Error (%)
1250.0	N/A	N/A	N/A	1250.0	N/A	N/A	N/A
625.0	N/A	N/A	N/A	625.0	N/A	N/A	N/A
250.0	1	223.72	–10.51	250.0	N/A	N/A	N/A
115.2	2	111.9	–2.90	115.2	1	115.2	0.00
57.6	4	55.9	–2.90	57.6	2	57.6	0.00
38.4	6	37.3	–2.90	38.4	3	38.4	0.00
19.2	12	18.6	–2.90	19.2	6	19.2	0.00
9.60	23	9.73	1.32	9.60	12	9.60	0.00
4.80	47	4.76	–0.83	4.80	24	4.80	0.00
2.40	93	2.41	0.23	2.40	48	2.40	0.00
1.20	186	1.20	0.23	1.20	96	1.20	0.00
0.60	373	0.60	–0.04	0.60	192	0.60	0.00
0.30	746	0.30	–0.04	0.30	384	0.30	0.00

I²C Controller

The I²C Controller makes the F0822 Series products bus-compatible with the I²C protocol. The I²C Controller consists of two bidirectional bus lines: a serial data signal (SDA) and a serial clock signal (SCL). Features of the I²C Controller include:

- Transmit and Receive Operation in MASTER Mode
- Maximum data rate of 400 kbit/s
- 7-bit and 10-bit addressing modes for Slaves
- Unrestricted number of data bytes transmitted per transfer

The I²C Controller in the F0822 Series products does not operate in SLAVE Mode.

Architecture

Figure 25 displays the architecture of the I²C Controller.

Table 88. Flash Frequency High Byte Register (FFREQH)

Bit	7	6	5	4	3	2	1	0
Field	FFREQH							
RESET	0							
R/W	R/W							
Address	FFAH							

Table 89. Flash Frequency Low Byte Register (FFREQL)

Bit	7	6	5	4	3	2	1	0
Field	FFREQL							
RESET	0							
R/W	R/W							
Address	FFBH							

Bit	Description
[7:0] FFREQH, FFREQL	**Flash Frequency High and Low Bytes** These 2 bytes, {FFREQH[7:0], FFREQL[7:0]}, contain the 16-bit Flash Frequency value.

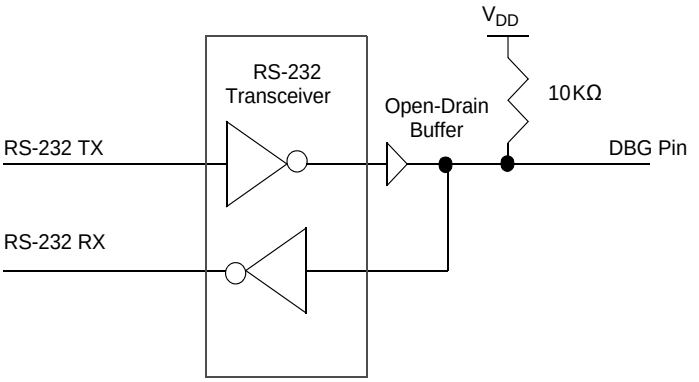

Figure 36. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #2 of 2

Debug Mode

The operating characteristics of the Z8 Encore! XP® F0822 Series devices in DEBUG Mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions
- The system clock operates unless in STOP Mode
- All enabled on-chip peripherals operate unless in STOP Mode
- Automatically exits HALT Mode
- Constantly refreshes the Watchdog Timer, if enabled

Entering Debug Mode

The device enters DEBUG Mode following any of the following operations:

- Writing the DBGMODE bit in the OCD Control Register to 1 using the OCD interface
- eZ8 CPU execution of a breakpoint (BRK) instruction
- Matching of the PC to the OCDCNTR Register (when enabled)
- The OCDCNTR Register decrements to 0000H (when enabled)
- If the DBG pin is Low when the device exits Reset, the OCD automatically places the device into DEBUG Mode

Figure 46 displays the maximum current consumption in STOP Mode with the VBO disabled and Watchdog Timer enabled plotted opposite the power supply voltage. All GPIO pins are configured as outputs and driven High. Disabling the Watchdog Timer and its internal RC oscillator in STOP Mode will provide some additional reduction in STOP Mode current consumption. This small current reduction is indistinquishable on the scale of Figure 46.

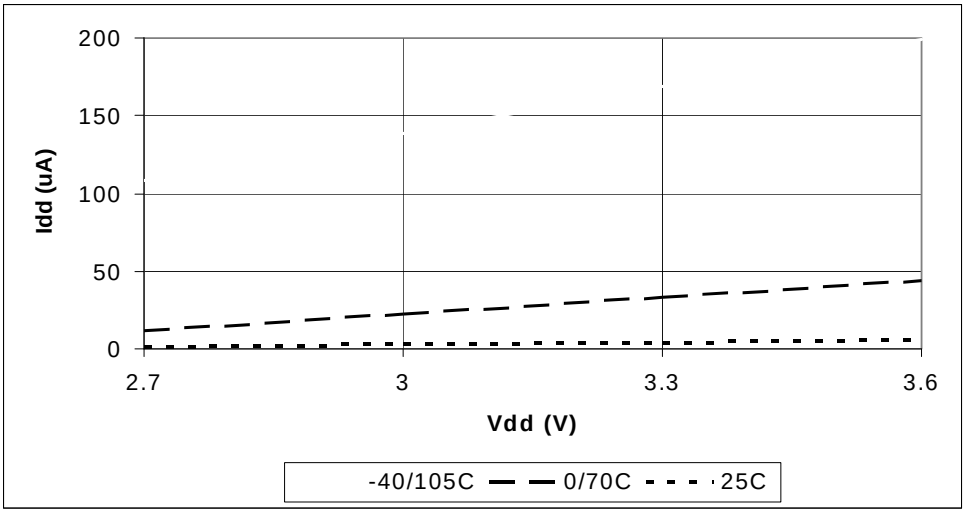

Figure 46. Maximum STOP Mode I_{DD} with VBO Disabled vs. Power Supply Voltage

Table 101 provides information about the external RC oscillator electrical characteristics and timing, and Table 102 provides information about the Flash memory electrical characteristics and timing.

Table 101. External RC Oscillator Electrical Characteristics and Timing

		T_A = –40°C to 105°C				
Symbol	**Parameter**	**Minimum**	**Typical***	**Maximum**	**Units**	**Conditions**
V_{DD}	Operating Voltage Range	2.70	–	–	V	
R_{EXT}	External Resistance from X_{IN} to V_{DD}	40	45	200	kΩ	
C_{EXT}	External Capacitance from X_{IN} to V_{SS}	0	20	1000	pF	
F_{OSC}	External RC Oscillation Frequency	–	–	4	MHz	

Note: *When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7V, but before the power supply drops to the voltage brown-out threshold. The oscillator will resume oscillation as soon as the supply voltage exceeds 2.7V.

Table 102. Flash Memory Electrical Characteristics and Timing

	V_{DD} = 2.7–3.6V T_A = –40°C to 105°C				
Parameter	**Minimum**	**Typical**	**Maximum**	**Units**	**Notes**
Flash Byte Read Time	50	–	–	µs	
Flash Byte Program Time	20	–	40	µs	
Flash Page Erase Time	10	–	–	ms	
Flash Mass Erase Time	200	–	–	ms	
Writes to Single Address Before Next Erase	–	–	2		
Flash Row Program Time	–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention	100	–	–	years	25°C
Endurance	10,000	–	–	cycles	Program/erase cycles

Table 105 lists ADC electrical characteristics and timing data.

Table 105. Analog-to-Digital Converter Electrical Characteristics and Timing

		V_{DD} = 3.0–3.6 V T_A = –40°C to 105°C				
Symbol	**Parameter**	**Minimum**	**Typical**	**Maximum**	**Units**	**Conditions**
	Resolution	10	–	–	bits	External V_{REF} = 3.0V
	Differential Nonlinearity (DNL)	–0.25	–	0.25	lsb	Guaranteed by design
	Integral Nonlinearity (INL)	–2.0	–	2.0	lsb	External V_{REF} = 3.0V
	DC Offset Error	–35	–	25	mV	80-pin QFP and 64-pin LQFP packages.
V_{REF}	Internal Reference Voltage	1.9	2.0	2.4	V	V_{DD} = 3.0–3.6V T_A = –40°C to 105°C
VC_{REF}	Voltage Coefficient of Internal Reference Voltage	–	78	–	mV/V	V_{REF} variation as a function of AV_{DD}.
TC_{REF}	Temperature Coefficient of Internal Reference Voltage	–	1	–	mV/°C	
	Single-Shot Conversion Period		5129		cycles	System clock cycles
	Continuous Conversion Period		256		cycles	System clock cycles
R_S	Analog Source Impedance	–	–	150	Ω	Recommended
Zin	Input Impedance		150		KΩ	20MHz system clock. Input impedance increases with lower system clock frequency.
V_{REF}	External Reference Voltage			AV_{DD}	V	AV_{DD} <= V_{DD}. When using an external reference voltage, decoupling capacitance should be placed from V_{REF} to AV_{SS}.
I_{REF}	Current draw into V_{REF} pin when driving with external source.		25.0	40.0	µA	

Table 122. CPU Control Instructions

Mnemonic	Operands	Instruction
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	HALT Mode
NOP	—	No Operation
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT	—	Watchdog Timer Refresh

Table 123. Load Instructions

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program memory
LDCI	dst, src	Load Constant to/from Program memory and Auto-Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Pop
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

Appendix A. Register Summary

For the reader's convenience, this appendix lists all Z8 Encore! XP® F0822 Series registers numerically by hexadecimal address.

General Purpose RAM

In the Z8 Encore! XP® F0822 Series, the 000–EFF hexadecimal address range is partitioned for general-purpose random access memory, as follows.

Hex Addresses: 000–1FF

This address range is reserved for general-purpose register file RAM. For more details, see the Register File Address Map chapter on page 17.

Hex Addresses: 200–EFF

This address range is reserved.

Timer 0 Control Registers

For more information about these Timer Control registers, see the Timer Control Register Definitions section on page 64.

Hex Address: F00

Table 130. Timer 0–1 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0							
R/W	R/W							
Address	F00H, F08H							

Hex Address: F72

Table 170. ADC Data High Byte Register (ADCD_H)

Bit	7	6	5	4	3	2	1	0
Field	ADCD_H							
RESET	X							
R/W	R							
Address	F72H							

Hex Address: F73

Table 171. ADC Data Low Bits Register (ADCD_L)

Bit	7	6	5	4	3	2	1	0
Field	ADCD_L		Reserved					
RESET	X							
R/W	R							
Address	F73H							

Hex Addresses: F74–FBF

This address range is reserved.

Interrupt Request Control Registers

For more information about the IRQ registers, see the Interrupt Control Register Definitions section on page 45.

Hex Address: FC0

Table 172. Interrupt Request 0 Register (IRQ0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1I	T0I	U0RXI	U0TXI	I2CI	SPII	ADCI
RESET	0							
R/W	R/W							
Address	FC0H							

Hex Addresses: FC9–FCE

This address range is reserved.

Hex Address: FCF

Table 181. Interrupt Control Register (IRQCTL)

Bit	7	6	5	4	3	2	1	0
Field	IRQE	Reserved						
RESET	0							
R/W	R/W	R						
Address	FCFH							

GPIO Control Registers

For more information about the GPIO control registers, see the GPIO Control Register Definitions section on page 31.

Hex Address: FD0

Table 182. Port A–C GPIO Address Registers (P*x*ADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W							
Address	FD0H, FD4H, FD8H							

Hex Address: FD1

Table 183. Port A–C Control Registers (P*x*CTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W							
Address	FD1H, FD5H, FD9H							

Hex Address: FF1

Table 195. Watchdog Timer Reload Upper Byte Register (WDTU)

Bit	7	6	5	4	3	2	1	0
Field	WDTU							
RESET	1							
R/W	R/W*							
Address	FF1H							
Note: *R/W = a read returns the current WDT count value; a write sets the appropriate reload value.								

Hex Address: FF2

Table 196. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	1							
R/W	R/W*							
Address	FF2H							
Note: *R/W = a read returns the current WDT count value; a write sets the appropriate reload value.								

Hex Address: FF3

Table 197. Watchdog Timer Reload Low Byte Register (WDTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	1							
R/W	R/W*							
Address	FF3H							
Note: *R/W = a read returns the current WDT count value; a write sets the appropriate reload value.								

Hex Addresses: FF4–FF7

This address range is reserved.

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