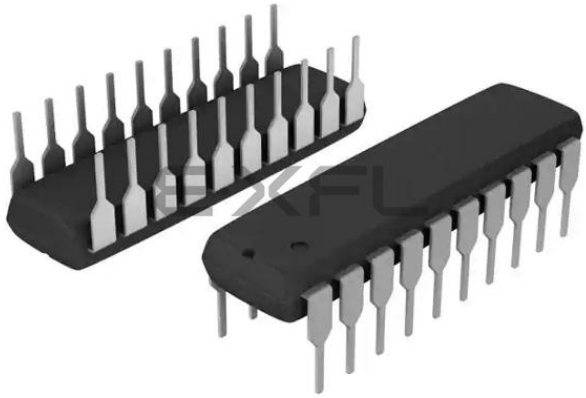

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | I²C, IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 11 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 20-DIP (0.300", 7.62mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0811ph020sg |

# Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

| Date | Revision Level | Description | Page |
|---|---|---|---|
| Oct 2011 | 18 | Added LDWX information to Load Instructions table, eZ8 CPU Instruction Summary table and to Second Op Code Map after 1FH figure; revised Flash Sector Protect Register description; revised Packaging chapter. | 206, 212, 220, 152, 221 |
| May 2008 | 17 | Removed *Flash Microcontrollers* from the title throughout the document. | All |
| Feb 2008 | 16 | Updated the flag status for BCLR, BIT, and BSET in eZ8 CPU Instruction Summary table. | 208 |
| Dec 2007 | 15 | Updated Zilog logo/text, Foreword section. Updated Z8 Encore! 8K Series to Z8 Encore! XP® F0822 Series Flash Microcontrollers throughout the document. | All |

## 10-Bit Analog-to-Digital Converter

The optional Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from 2 to 5 different analog input sources.

## UART

The Universal Asynchronous Receiver/Transmitter (UART) is full-duplex and capable of handling asynchronous data transfers. The UART supports 8-bit and 9-bit data modes and selectable parity.

## $I^2C$

The Inter-Integrated Circuit ($I^2C$) controller makes the Z8 Encore! XP compatible with the $I^2C$ protocol. The $I^2C$ Controller consists of two bidirectional bus lines, a serial data (SDA) line, and a serial clock (SCL) line.

## Serial Peripheral Interface

The Serial Peripheral Interface (SPI) allows the Z8 Encore! XP to exchange data between other peripheral devices such as EEPROMs, A/D converters, and ISDN devices. The SPI is a full-duplex, synchronous, and character-oriented channel that supports a four-wire interface.

## Timers

Two 16-bit reloadable timers are used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in One-Shot, Continuous, Gated, Capture, Compare, Capture and Compare, and PWM modes.

## Interrupt Controller

Z8 Encore! XP® F0822 Series products support up to 18 interrupts. These interrupts consist of 7 internal peripheral interrupts and 11 GPIO pin interrupt sources. The interrupts have 3 levels of programmable interrupt priority.

## Reset Controller

Z8 Encore! XP® F0822 Series products are reset using the $\overline{\text{RESET}}$ pin, POR, WDT, STOP Mode exit, or VBO warning signal.

**Table 7. Register File Address Map (Continued)**

| Address (Hex) | Register Description | Mnemonic | Reset (Hex) | Page No |
|---|---|---|---|---|
| **Analog-to-Digital Converter (ADC)** | | | | |
| F70 | ADC Control | ADCCTL | 20 | 139 |
| F71 | Reserved | — | XX | |
| F72 | ADC Data High Byte | ADCD_H | XX | 141 |
| F73 | ADC Data Low Bits | ADCD_L | XX | 142 |
| F74–FBF | Reserved | — | XX | |
| **Interrupt Controller** | | | | |
| FC0 | Interrupt Request 0 | IRQ0 | 00 | 45 |
| FC1 | IRQ0 Enable High Bit | IRQ0ENH | 00 | 48 |
| FC2 | IRQ0 Enable Low Bit | IRQ0ENL | 00 | 48 |
| FC3 | Interrupt Request 1 | IRQ1 | 00 | 46 |
| FC4 | IRQ1 Enable High Bit | IRQ1ENH | 00 | 49 |
| FC5 | IRQ1 Enable Low Bit | IRQ1ENL | 00 | 49 |
| FC6 | Interrupt Request 2 | IRQ2 | 00 | 47 |
| FC7 | IRQ2 Enable High Bit | IRQ2ENH | 00 | 51 |
| FC8 | IRQ2 Enable Low Bit | IRQ2ENL | 00 | 51 |
| FC9–FCC | Reserved | — | XX | |
| FCD | Interrupt Edge Select | IRQES | 00 | 52 |
| FCE | Reserved | — | 00 | |
| FCF | Interrupt Control | IRQCTL | 00 | 53 |
| **GPIO Port A** | | | | |
| FD0 | Port A Address | PAADDR | 00 | 32 |
| FD1 | Port A Control | PACTL | 00 | 33 |
| FD2 | Port A Input Data | PAIN | XX | 38 |
| FD3 | Port A Output Data | PAOUT | 00 | 39 |
| **GPIO Port B** | | | | |
| FD4 | Port B Address | PBADDR | 00 | 32 |
| FD5 | Port B Control | PBCTL | 00 | 33 |
| FD6 | Port B Input Data | PBIN | XX | 38 |
| FD7 | Port B Output Data | PBOUT | 00 | 39 |

Note: XX = undefined.

# Reset and Stop Mode Recovery

The Reset Controller within the Z8 Encore! XP® F0822 Series controls Reset and Stop Mode Recovery operation. In typical operation, the following events cause a Reset to occur:

- Power-On Reset (POR)
- Voltage Brown-Out
- WDT time-out (when configured through the WDT_RES option bit to initiate a Reset)
- External $\overline{\text{RESET}}$ pin assertion
- On-Chip Debugger initiated Reset (OCDCTL[0] set to 1)

When the Z8 Encore! XP® F0822 Series device is in STOP Mode, a Stop Mode Recovery is initiated by any of the following events:

- WDT time-out
- GPIO Port input pin transition on an enabled Stop Mode Recovery source
- DBG pin driven Low

## Reset Types

Z8 Encore! XP® F0822 Series provides two types of reset operation (System Reset and Stop Mode Recovery). The type of reset is a function of both the current operating mode of the Z8 Encore! XP® F0822 Series device and the source of the Reset. Table 8 lists the types of Resets and their operating characteristics.

**Table 8. Reset and Stop Mode Recovery Characteristics and Latency**

| | Reset Characteristics and Latency | | |
|---|---|---|---|
| **Reset Type** | **Control Registers** | **eZ8 CPU** | **Reset Latency (Delay)** |
| System Reset | Reset (as applicable) | Reset | 66 WDT Oscillator cycles + 16 System Clock cycles |
| Stop Mode Recovery | Unaffected, except for the WDT_CTL Register | Reset | 66 WDT Oscillator cycles + 16 System Clock cycles |

### System Reset

During a System Reset, a Z8 Encore! XP® F0822 Series device is held in Reset for 66 cycles of the WDT oscillator followed by 16 cycles of the system clock. At the beginning

In COMPARE Mode, the system clock always provides the timer input. The Compare time is calculated by the following equation:

$$\text{Compare Mode Time (s)} = \frac{(\text{Compare Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## GATED Mode

In GATED Mode, the timer counts only when the Timer Input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control Register. When the Timer Input signal is asserted, counting begins. A timer interrupt is generated when the Timer Input signal is deasserted or a timer reload occurs. To determine if a Timer Input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. When reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the Timer Input signal is still asserted). Also, if the Timer Output alternate function is enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reset.

Observe the following procedure for configuring a timer for GATED Mode and initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for GATED Mode
   - Set the prescale value
2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in GATED Mode. After the first timer reset in GATED Mode, counting always begins at the reset value of 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin for the Timer Input alternate function.
6. Write to the Timer Control Register to enable the timer.
7. Assert the Timer Input signal to initiate the counting.

# Universal Asynchronous Receiver/ Transmitter

The Universal Asynchronous Receiver/Transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. Features of the UART include:

- 8-bit asynchronous data transfer
- Selectable even- and odd-parity generation and checking
- Option of one or two stop bits
- Separate transmit and receive interrupts
- Framing, parity, overrun, and break detection
- Separate transmit and receive enables
- 16-bit Baud Rate Generator
- Selectable MULTIPROCESSOR (9-Bit) Mode with three configurable interrupt schemes
- BRG timer mode
- Driver Enable output for external bus transceivers

## Architecture

The UART consists of three primary functional blocks: Transmitter, Receiver, and Baud Rate Generator. The UART's transmitter and receiver functions independently, but use the same baud rate and data format. Figure 11 displays the UART architecture.

6. Read data from the UART Receive Data Register. If operating in MULTIPROCESSOR (9-Bit) Mode, further actions may be required depending on the Multiprocessor Mode bits MPMD[1:0].
7. Return to Step 5 to receive additional data.

## Receiving Data Using Interrupt-Driven Method

The UART Receiver interrupt indicates the availability of new data (as well as error conditions). Observe the following procedure to configure the UART receiver for interrupt-driven operation:

1. Write to the UART Baud Rate High and Low Byte registers to set the required baud rate.
2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
3. Execute a DI instruction to disable interrupts.
4. Write to the Interrupt Control registers to enable the UART Receiver interrupt and set the required priority.
5. Clear the UART Receiver interrupt in the applicable Interrupt Request Register.
6. Write to the UART Control 1 Register to enable MULTIPROCESSOR (9-Bit) Mode functions, if appropriate.
   - Set the Multiprocessor Mode Select (MPEN) to enable MULTIPROCESSOR Mode.
   - Set the Multiprocessor Mode bits, MPMD[1:0], to select the required address matching scheme.
   - Configure the UART to interrupt on received data and errors or errors only (interrupt on errors only is unlikely to be useful for Z8 Encore! XP devices without a DMA block)
7. Write the device address to the Address Compare Register (automatic multiprocessor modes only).
8. Write to the UART Control 0 Register to:
   - Set the receive enable bit (REN) to enable the UART for data reception
   - Enable parity, if required, and if MULTIPROCESSOR Mode is not enabled, and select either even or odd parity.
9. Execute an EI instruction to enable interrupts.

**Table 53. UART Transmit Data Register (U0TXD)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TXD | | | | | | | |
| RESET | X | X | X | X | X | X | X | X |
| R/W | W | W | W | W | W | W | W | W |
| Address | F40H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>TXD | **Transmit Data**<br>UART transmitter data byte to be shifted out through the TXD*x* pin. |

## UART Receive Data Register

Data bytes received through the RXD*x* pin are stored in the UART Receive Data Register, which is shown in Table 54. The read-only UART Receive Data Register shares a Register File address with the write-only UART Transmit Data Register.

**Table 54. UART Receive Data Register (U0RXD)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RXD | | | | | | | |
| RESET | X | | | | | | | |
| R/W | R | | | | | | | |
| Address | F40H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>RXD | **Receive Data**<br>UART receiver data byte from the RXD*x* pin. |

## UART Control 0 and Control 1 Registers

The UART Control 0 and Control 1 registers, shown in Tables 57 and 58, configure the properties of the UART's transmit and receive operations. The UART Control registers must not been written while the UART is enabled.

**Table 57. UART Control 0 Register (U0CTL0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TEN | REN | CTSE | PEN | PSEL | SBRK | STOP | LBEN |
| RESET | 0 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F42H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>TEN | **Transmit Enable**<br>This bit enables or disables the transmitter. The enable is also controlled by the $\overline{CTS}$ signal and the CTSE bit. If the $\overline{CTS}$ signal is Low and the CTSE bit is 1, the transmitter is enabled.<br>0 = Transmitter disabled.<br>1 = Transmitter enabled. |
| [6]<br>REN | **Receive Enable**<br>This bit enables or disables the receiver.<br>0 = Receiver disabled.<br>1 = Receiver enabled. |
| [5]<br>CTSE | **CTS Enable**<br>0 = The $\overline{CTS}$ signal has no effect on the transmitter.<br>1 = The UART recognizes the $\overline{CTS}$ signal as an enable control from the transmitter. |
| [4]<br>PEN | **Parity Enable**<br>This bit enables or disables parity. Even or odd is determined by the PSEL bit. This bit is overridden by the MPEN bit.<br>0 = Parity is disabled.<br>1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit. |
| [3]<br>PSEL | **Parity Select**<br>0 = Even parity is transmitted and expected on all received data.<br>1 = Odd parity is transmitted and expected on all received data. |
| [2]<br>SBRK | **Send Break**<br>This bit pauses or breaks data transmission by forcing the Transmit data output to 0. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit. The UART does not automatically generate a stop bit when SBRK is deasserted. Software must time the duration of the break and the duration of any appropriate stop bit time following the break.<br>0 = No break is sent.<br>1 = The output of the transmitter is zero. |

| Bit | Description (Continued) |
|---|---|
| [1]<br>STOP | **Stop Bit Select**<br>0 = The transmitter sends one stop bit.<br>1 = The transmitter sends two stop bits. |
| [0]<br>LBEN | **Loop Back Enable**<br>0 = Normal operation.<br>1 = All transmitted data is looped back to the receiver. |

**Table 58. UART Control 1 Register (U0CTL1)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | MPMD[1] | MPEN | MPMD[0] | MPBT | DEPOL | BRGCTL | RDAIRQ | IREN |
| RESET | 0 | | | | | | | |
| R/W | R/W | | | | | | | |
| Address | F43H | | | | | | | |

| Bit | Description |
|---|---|
| [7,5]<br>MPMD[1,0] | **Multiprocessor Mode**<br>If MULTIPROCESSOR (9-Bit) Mode is enabled,<br>00 = The UART generates an interrupt request on all received bytes (data and address).<br>01 = The UART generates an interrupt request only on received address bytes.<br>10 = The UART generates an interrupt request when a received address byte matches the value stored in the Address Compare Register and on all successive data bytes until an address mismatch occurs.<br>11 = The UART generates an interrupt request on all received data bytes for which the most recent address byte matched the value in the Address Compare Register. |
| [6]<br>MPEN | **Multiprocessor (9-Bit) Enable**<br>This bit is used to enable MULTIPROCESSOR (9-Bit) Mode.<br>0 = Disable MULTIPROCESSOR (9-Bit) Mode.<br>1 = Enable MULTIPROCESSOR (9-Bit) Mode. |
| [4]<br>MPBT | **Multiprocessor Bit Transmit**<br>This bit is applicable only when MULTIPROCESSOR (9-Bit) Mode is enabled.<br>0 = Send a 0 in the multiprocessor bit location of the data stream (9th bit).<br>1 = Send a 1 in the multiprocessor bit location of the data stream (9th bit). |
| [3]<br>DEPOL | **Driver Enable Polarity**<br>0 = DE signal is Active High.<br>1 = DE signal is Active Low. |

## Start and Stop Conditions

The Master ($I^2C$) drives all Start and Stop signals and initiates all transactions. To start a transaction, the $I^2C$ Controller generates a start condition by pulling the SDA signal Low while SCL is High. To complete a transaction, the $I^2C$ Controller generates a Stop condition by creating a Low-to-High transition of the SDA signal while the SCL signal is High. The start and stop bits in the $I^2C$ Control Register control the sending of start and stop conditions. A Master is also allowed to end one transaction and begin a new one by issuing a restart. This restart issuance is accomplished by setting the start bit at the end of a transaction rather than setting the stop bit.

**Note:** The start condition is not sent until the start bit is set and data has been written to the $I^2C$ Data Register.

## Master Write and Read Transactions

The following sections provide Zilog's recommended procedure for performing $I^2C$ write and read transactions from the $I^2C$ Controller (Master) to slave $I^2C$ devices. In general, software should rely on the TDRE, RDRF and NCKI bits of the status register (these bits generate interrupts) to initiate software actions. When using interrupts or DMA, the TXI bit is set to start each transaction and cleared at the end of each transaction to eliminate a *trailing* transmit interrupt.

**Caution:** Caution should be used in using the ACK status bit within a transaction because it is difficult for software to tell when it is updated by hardware.

When writing data to a slave, the $I^2C$ pauses at the beginning of the Acknowledge cycle if the data register has not been written with the next value to be sent (TDRE bit in the $I^2C$ Status Register equal to 1). In this scenario where software is not keeping up with the $I^2C$ bus (TDRE asserted longer than one byte time), the Acknowledge clock cycle for byte *n* is delayed until the data register is written with byte *n+1*, and appears to be grouped with the data clock cycles for byte *n+1*. If either the start or stop bit is set, the $I^2C$ does not pause prior to the Acknowledge cycle because no additional data is sent.

When a Not Acknowledge condition is received during a write (either during the address or data phases), the $I^2C$ Controller generates the Not Acknowledge interrupt (NCKI = 1) and pause until either the stop or start bit is set. Unless the Not Acknowledge was received on the last byte, the data register will already have been written with the next address or data byte to send. In this case the FLUSH bit of the control register should be set at the same time the stop or start bit is set to remove the stale transmit data and enable subsequent transmit interrupts.

# Oscillator Operation with an External RC Network

The External RC oscillator mode is applicable to timing insensitive applications. Figure 39 displays a recommended configuration for connection with an external resistor-capacitor (RC) network.

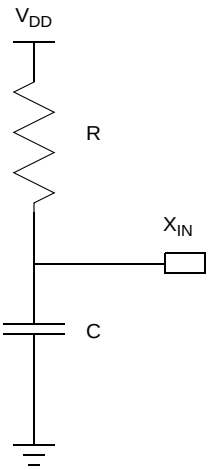


**Figure 39. Connecting the On-Chip Oscillator to an External RC Network**

An external resistance value of 45 kΩ is recommended for oscillator operation with an external RC network. The minimum resistance value to ensure operation is 40 kΩ. The typical oscillator frequency can be estimated from the values of the resistor (*R* in kΩ) and capacitor (*C* in pF) elements using the below equation:

$$\text{Oscillator Frequency (kHz)} = \frac{1\times10^{6}}{(0.4 \times R \times C) + (4 \times C)}$$

Figure 40 displays the typical (3.3V and 25°C) oscillator frequency as a function of the capacitor (*C* in pF) employed in the RC network assuming a 45 kΩ external resistor. For very small values of C, the parasitic capacitance of the oscillator $X_{IN}$ pin and the printed circuit board should be included in the estimation of the oscillator frequency.

It is possible to operate the RC oscillator using only the parasitic capacitance of the package and printed circuit board. To minimize sensitivity to external parasites, external capacitance values in excess of 20pF are recommended.

# On-Chip Peripheral AC and DC Electrical Characteristics

Table 100 provides information about the Power-On Reset and Voltage Brown-Out electrical characteristics.

**Table 100. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing**

| | | $T_A$ = –40°C to 105°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical*** | **Maximum** | **Units** | **Conditions** |
| $V_{POR}$ | Power-On Reset Voltage Threshold | 2.15 | 2.40 | 2.60 | V | $V_{DD} = V_{POR}$ |
| $V_{VBO}$ | Voltage Brown-Out Reset Voltage Threshold | 2.05 | 2.30 | 2.55 | V | $V_{DD} = V_{VBO}$ |
| | $V_{POR}$ to $V_{VBO}$ hysteresis | 50 | 100 | – | mV | |
| | Starting $V_{DD}$ voltage to ensure valid POR | – | $V_{SS}$ | – | V | |
| $T_{ANA}$ | POR Analog Delay | – | 50 | – | µs | $V_{DD} > V_{POR}$; $T_{POR}$ Digital Reset delay follows $T_{ANA}$ |
| $T_{POR}$ | POR Digital Delay | – | 5.0 | – | ms | 50 WDT Oscillator cycles (10kHz) + 16 System Clock cycles (20MHz) |
| $T_{VBO}$ | Voltage Brown-Out Pulse Rejection Period | – | 10 | – | µs | $V_{DD} < V_{VBO}$ to generate a Reset. |
| $T_{RAMP}$ | Time for VDD to transition from $V_{SS}$ to $V_{POR}$ to ensure valid Reset | 0.10 | – | 100 | ms | |

Note: *Data in the typical column is from characterization at 3.3 V and 25°C. These values are provided for design guidance only and are not tested in production.

Table 103 lists Reset and Stop Mode Recovery pin timing data; Table 104 lists Watchdog Timer Electrical Characteristics and Timing data.

**Table 103. Reset and Stop Mode Recovery Pin Timing**

| | | $T_A$ = –40°C to 105°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical*** | **Maximum** | **Units** | **Conditions** |
| $T_{RESET}$ | $\overline{\text{Reset}}$ pin assertion to initiate a System Reset | 4 | – | – | $T_{CLK}$ | Not in STOP Mode. $T_{CLK}$ = System Clock period. |
| $T_{SMR}$ | Stop Mode Recovery pin Pulse Rejection Period | 10 | 20 | 40 | ns | $\overline{\text{RESET}}$, DBG and GPIO pins configured as SMR sources. |

Note: *When using the external RC oscillator mode, the oscillator can stop oscillating if the power supply drops below 2.7V, but before the power supply drops to the voltage brown-out threshold. The oscillator will resume oscillation as soon as the supply voltage exceeds 2.7V.

**Table 104. Watchdog Timer Electrical Characteristics and Timing**

| | | $V_{DD}$ = 2.7–3.6 V<br>$T_A$ = –40°C to 105°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| $F_{WDT}$ | WDT Oscillator Frequency | 5 | 10 | 20 | kHz | |
| $I_{WDT}$ | WDT Oscillator Current including internal RC oscillator | – | < 1 | 5 | µA | |

Table 105 lists ADC electrical characteristics and timing data.

**Table 105. Analog-to-Digital Converter Electrical Characteristics and Timing**

| | | $V_{DD}$ = 3.0–3.6 V<br>$T_A$ = –40°C to 105°C | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| | Resolution | 10 | – | – | bits | External $V_{REF}$ = 3.0V |
| | Differential Nonlinearity (DNL) | –0.25 | – | 0.25 | lsb | Guaranteed by design |
| | Integral Nonlinearity (INL) | –2.0 | – | 2.0 | lsb | External $V_{REF}$ = 3.0V |
| | DC Offset Error | –35 | – | 25 | mV | 80-pin QFP and 64-pin LQFP packages. |
| $V_{REF}$ | Internal Reference Voltage | 1.9 | 2.0 | 2.4 | V | $V_{DD}$ = 3.0–3.6V<br>$T_A$ = –40°C to 105°C |
| $VC_{REF}$ | Voltage Coefficient of Internal Reference Voltage | – | 78 | – | mV/V | $V_{REF}$ variation as a function of $AV_{DD}$. |
| $TC_{REF}$ | Temperature Coefficient of Internal Reference Voltage | – | 1 | – | mV/°C | |
| | Single-Shot Conversion Period | | 5129 | | cycles | System clock cycles |
| | Continuous Conversion Period | | 256 | | cycles | System clock cycles |
| $R_S$ | Analog Source Impedance | – | – | 150 | Ω | Recommended |
| Zin | Input Impedance | | 150 | | KΩ | 20MHz system clock. Input impedance increases with lower system clock frequency. |
| $V_{REF}$ | External Reference Voltage | | | $AV_{DD}$ | V | $AV_{DD}$ <= $V_{DD}$. When using an external reference voltage, decoupling capacitance should be placed from $V_{REF}$ to $AV_{SS}$. |
| $I_{REF}$ | Current draw into $V_{REF}$ pin when driving with external source. | | 25.0 | 40.0 | µA | |

**Table 124. Logical Instructions**

| Mnemonic | Operands | Instruction |
|---|---|---|
| AND | dst, src | Logical AND |
| ANDX | dst, src | Logical AND using Extended Addressing |
| COM | dst | Complement |
| OR | dst, src | Logical OR |
| ORX | dst, src | Logical OR using Extended Addressing |
| XOR | dst, src | Logical Exclusive OR |
| XORX | dst, src | Logical Exclusive OR using Extended Addressing |

**Table 125. Program Control Instructions**

| Mnemonic | Operands | Instruction |
|---|---|---|
| BRK | — | On-Chip Debugger Break |
| BTJ | p, bit, src, DA | Bit Test and Jump |
| BTJNZ | bit, src, DA | Bit Test and Jump if Non-Zero |
| BTJZ | bit, src, DA | Bit Test and Jump if Zero |
| CALL | dst | Call Procedure |
| DJNZ | dst, src, RA | Decrement and Jump Non-Zero |
| IRET | — | Interrupt Return |
| JP | dst | Jump |
| JP cc | dst | Jump Conditional |
| JR | DA | Jump Relative |
| JR cc | DA | Jump Relative Conditional |
| RET | — | Return |
| TRAP | vector | Software Trap |

| Upper Nibble (Hex) \ Lower Nibble (Hex) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1.2 **BRK** | 2.2 **SRP** IM | 2.3 **ADD** r1,r2 | 2.4 **ADD** r1,Ir2 | 3.3 **ADD** R2,R1 | 3.4 **ADD** IR2,R1 | 3.3 **ADD** R1,IM | 3.4 **ADD** IR1,IM | 4.3 **ADDX** ER2,ER1 | 4.3 **ADDX** IM,ER1 | 2.3 **DJNZ** r1,X | 2.2 **JR** cc,X | 2.2 **LD** r1,IM | 3.2 **JP** cc,DA | 1.2 **INC** r1 | 1.2 **NOP** |
| 1 | 2.2 **RLC** R1 | 2.3 **RLC** IR1 | 2.3 **ADC** r1,r2 | 2.4 **ADC** r1,Ir2 | 3.3 **ADC** R2,R1 | 3.4 **ADC** IR2,R1 | 3.3 **ADC** R1,IM | 3.4 **ADC** IR1,IM | 4.3 **ADCX** ER2,ER1 | 4.3 **ADCX** IM,ER1 | | | | | | See 2nd Op Code Map |
| 2 | 2.2 **INC** R1 | 2.3 **INC** IR1 | 2.3 **SUB** r1,r2 | 2.4 **SUB** r1,Ir2 | 3.3 **SUB** R2,R1 | 3.4 **SUB** IR2,R1 | 3.3 **SUB** R1,IM | 3.4 **SUB** IR1,IM | 4.3 **SUBX** ER2,ER1 | 4.3 **SUBX** IM,ER1 | | | | | | |
| 3 | 2.2 **DEC** R1 | 2.3 **DEC** IR1 | 2.3 **SBC** r1,r2 | 2.4 **SBC** r1,Ir2 | 3.3 **SBC** R2,R1 | 3.4 **SBC** IR2,R1 | 3.3 **SBC** R1,IM | 3.4 **SBC** IR1,IM | 4.3 **SBCX** ER2,ER1 | 4.3 **SBCX** IM,ER1 | | | | | | |
| 4 | 2.2 **DA** R1 | 2.3 **DA** IR1 | 2.3 **OR** r1,r2 | 2.4 **OR** r1,Ir2 | 3.3 **OR** R2,R1 | 3.4 **OR** IR2,R1 | 3.3 **OR** R1,IM | 3.4 **OR** IR1,IM | 4.3 **ORX** ER2,ER1 | 4.3 **ORX** IM,ER1 | | | | | | |
| 5 | 2.2 **POP** R1 | 2.3 **POP** IR1 | 2.3 **AND** r1,r2 | 2.4 **AND** r1,Ir2 | 3.3 **AND** R2,R1 | 3.4 **AND** IR2,R1 | 3.3 **AND** R1,IM | 3.4 **AND** IR1,IM | 4.3 **ANDX** ER2,ER1 | 4.3 **ANDX** IM,ER1 | | | | | | 1.2 **WDT** |
| 6 | 2.2 **COM** R1 | 2.3 **COM** IR1 | 2.3 **TCM** r1,r2 | 2.4 **TCM** r1,Ir2 | 3.3 **TCM** R2,R1 | 3.4 **TCM** IR2,R1 | 3.3 **TCM** R1,IM | 3.4 **TCM** IR1,IM | 4.3 **TCMX** ER2,ER1 | 4.3 **TCMX** IM,ER1 | | | | | | 1.2 **STOP** |
| 7 | 2.2 **PUSH** R2 | 2.3 **PUSH** IR2 | 2.3 **TM** r1,r2 | 2.4 **TM** r1,Ir2 | 3.3 **TM** R2,R1 | 3.4 **TM** IR2,R1 | 3.3 **TM** R1,IM | 3.4 **TM** IR1,IM | 4.3 **TMX** ER2,ER1 | 4.3 **TMX** IM,ER1 | | | | | | 1.2 **HALT** |
| 8 | 2.5 **DECW** RR1 | 2.6 **DECW** IRR1 | 2.5 **LDE** r1,Irr2 | 2.9 **LDEI** Ir1,Irr2 | 3.2 **LDX** r1,ER2 | 3.3 **LDX** Ir1,ER2 | 3.4 **LDX** IRR2,R1 | 3.5 **LDX** IRR2,IR1 | 3.4 **LDX** r1,rr2,X | 3.4 **LDX** rr1,r2,X | | | | | | 1.2 **DI** |
| 9 | 2.2 **RL** R1 | 2.3 **RL** IR1 | 2.5 **LDE** r2,Irr1 | 2.9 **LDEI** Ir2,Irr1 | 3.2 **LDX** r2,ER1 | 3.3 **LDX** Ir2,ER1 | 3.4 **LDX** R2,IRR1 | 3.5 **LDX** IR2,IRR1 | 3.3 **LEA** r1,r2,X | 3.5 **LEA** rr1,rr2,X | | | | | | 1.2 **EI** |
| A | 2.5 **INCW** RR1 | 2.6 **INCW** IRR1 | 2.3 **CP** r1,r2 | 2.4 **CP** r1,Ir2 | 3.3 **CP** R2,R1 | 3.4 **CP** IR2,R1 | 3.3 **CP** R1,IM | 3.4 **CP** IR1,IM | 4.3 **CPX** ER2,ER1 | 4.3 **CPX** IM,ER1 | | | | | | 1.4 **RET** |
| B | 2.2 **CLR** R1 | 2.3 **CLR** IR1 | 2.3 **XOR** r1,r2 | 2.4 **XOR** r1,Ir2 | 3.3 **XOR** R2,R1 | 3.4 **XOR** IR2,R1 | 3.3 **XOR** R1,IM | 3.4 **XOR** IR1,IM | 4.3 **XORX** ER2,ER1 | 4.3 **XORX** IM,ER1 | | | | | | 1.5 **IRET** |
| C | 2.2 **RRC** R1 | 2.3 **RRC** IR1 | 2.5 **LDC** r1,Irr2 | 2.9 **LDCI** Ir1,Irr2 | 2.3 **JP** IRR1 | 2.9 **LDC** Ir1,Irr2 | | 3.4 **LD** r1,r2,X | 3.2 **PUSHX** ER2 | | | | | | | 1.2 **RCF** |
| D | 2.2 **SRA** R1 | 2.3 **SRA** IR1 | 2.5 **LDC** r2,Irr1 | 2.9 **LDCI** Ir2,Irr1 | 2.6 **CALL** IRR1 | 2.2 **BSWAP** R1 | 3.3 **CALL** DA | 3.4 **LD** r2,r1,X | 3.2 **POPX** ER1 | | | | | | | 1.2 **SCF** |
| E | 2.2 **RR** R1 | 2.3 **RR** IR1 | 2.2 **BIT** p,b,r1 | 2.3 **LD** r1,Ir2 | 3.2 **LD** R2,R1 | 3.3 **LD** IR2,R1 | 3.2 **LD** R1,IM | 3.3 **LD** IR1,IM | 4.2 **LDX** ER2,ER1 | 4.2 **LDX** IM,ER1 | | | | | | 1.2 **CCF** |
| F | 2.2 **SWAP** R1 | 2.3 **SWAP** IR1 | 2.6 **TRAP** Vector | 2.3 **LD** Ir1,r2 | 2.8 **MULT** RR1 | 3.3 **LD** R2,IR1 | 3.3 **BTJ** p,b,r1,X | 3.4 **BTJ** p,b,Ir1,X | | | | | | | | |

**Figure 58. First Op Code Map**

# Ordering Information

Order your Z8 Encore! XP® F0822 Series products from Zilog using the part numbers shown in Table 129. For more information about ordering, please consult your local Zilog sales office. The Sales Location page on the Zilog website lists all regional offices.

**Table 129. Z8 Encore! XP F0830 Series Ordering Matrix**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | $I^2C$ | SPI | UARTs with IrDA | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| **Z8F08xx with 8KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | | | |
| Z8F0821HH020SG | 8KB | 1KB | 11 | 16 | 2 | 2 | 1 | 0 | 1 | SSOP 20-pin package |
| Z8F0821PH020SG | 8KB | 1KB | 11 | 16 | 2 | 2 | 1 | 0 | 1 | PDIP 20-pin package |
| Z8F0822SJ020SG | 8KB | 1KB | 19 | 19 | 2 | 5 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F0822PJ020SG | 8KB | 1KB | 19 | 19 | 2 | 5 | 1 | 1 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40° to +105°C** | | | | | | | | | | |
| Z8F0821HH020EG | 8KB | 1KB | 11 | 16 | 2 | 2 | 1 | 0 | 1 | SSOP 20-pin package |
| Z8F0821PH020EG | 8KB | 1KB | 11 | 16 | 2 | 2 | 1 | 0 | 1 | PDIP 20-pin package |
| Z8F0822SJ020EG | 8KB | 1KB | 19 | 19 | 2 | 5 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F0822PJ020EG | 8KB | 1KB | 19 | 19 | 2 | 5 | 1 | 1 | 1 | PDIP 28-pin package |
| **Z8F08xx with 8KB Flash** | | | | | | | | | | |
| Standard Temperature: 0°C to 70°C | | | | | | | | | | |
| Z8F0811HH020SG | 8KB | 1KB | 11 | 16 | 2 | 0 | 1 | 0 | 1 | SSOP 20-pin package |
| Z8F0811PH020SG | 8KB | 1KB | 11 | 16 | 2 | 0 | 1 | 0 | 1 | PDIP 20-pin package |
| Z8F0812SJ020SG | 8KB | 1KB | 19 | 19 | 2 | 0 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F0812PJ020SG | 8KB | 1KB | 19 | 19 | 2 | 0 | 1 | 1 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to +105°C** | | | | | | | | | | |
| Z8F0811HH020EG | 8KB | 1KB | 11 | 16 | 2 | 0 | 1 | 0 | 1 | SSOP 20-pin package |
| Z8F0811PH020EG | 8KB | 1KB | 11 | 16 | 2 | 0 | 1 | 0 | 1 | PDIP 20-pin package |
| Z8F0812SJ020EG | 8KB | 1KB | 19 | 19 | 2 | 0 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F0812PJ020EG | 8KB | 1KB | 19 | 19 | 2 | 0 | 1 | 1 | 1 | PDIP 28-pin package |

**Table 129. Z8 Encore! XP F0830 Series Ordering Matrix**

| Part Number | Flash | RAM | I/O Lines | Interrupts | 16-Bit Timers w/PWM | 10-Bit A/D Channels | $I^2C$ | SPI | UARTs with IrDA | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| **Z8F04xx with 4KB Flash, 10-Bit Analog-to-Digital Converter** | | | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | | | |
| Z8F0421HH020SG | 4KB | 1KB | 11 | 16 | 2 | 2 | 1 | 0 | 1 | SSOP 20-pin package |
| Z8F0421PH020SG | 4KB | 1KB | 11 | 16 | 2 | 2 | 1 | 0 | 1 | PDIP 20-pin package |
| Z8F0422SJ020SG | 4KB | 1KB | 19 | 19 | 2 | 5 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F0422PJ020SG | 4KB | 1KB | 19 | 19 | 2 | 5 | 1 | 1 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | | | |
| Z8F0421HH020EG | 4KB | 1KB | 11 | 16 | 2 | 2 | 1 | 0 | 1 | SSOP 20-pin package |
| Z8F0421PH020EG | 4KB | 1KB | 11 | 16 | 2 | 2 | 1 | 0 | 1 | PDIP 20-pin package |
| Z8F0422SJ020EG | 4KB | 1KB | 19 | 19 | 2 | 5 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F0422PJ020EG | 4KB | 1KB | 19 | 19 | 2 | 5 | 1 | 1 | 1 | PDIP 28-pin package |
| **Z8F04xx with 4KB Flash** | | | | | | | | | | |
| **Standard Temperature: 0°C to 70°C** | | | | | | | | | | |
| Z8F0411HH020SG | 4KB | 1KB | 11 | 16 | 2 | 0 | 1 | 0 | 1 | SSOP 20-pin package |
| Z8F0411PH020SG | 4KB | 1KB | 11 | 16 | 2 | 0 | 1 | 0 | 1 | PDIP 20-pin package |
| Z8F0412SJ020SG | 4KB | 1KB | 19 | 19 | 2 | 0 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F0412PJ020SG | 4KB | 1KB | 19 | 19 | 2 | 0 | 1 | 1 | 1 | PDIP 28-pin package |
| **Extended Temperature: –40°C to 105°C** | | | | | | | | | | |
| Z8F0411HH020EG | 4KB | 1KB | 11 | 16 | 2 | 0 | 1 | 0 | 1 | SSOP 20-pin package |
| Z8F0411PH020EG | 4KB | 1KB | 11 | 16 | 2 | 0 | 1 | 0 | 1 | PDIP 20-pin package |
| Z8F0412SJ020EG | 4KB | 1KB | 19 | 19 | 2 | 0 | 1 | 1 | 1 | SOIC 28-pin package |
| Z8F0412PJ020EG | 4KB | 1KB | 19 | 19 | 2 | 0 | 1 | 1 | 1 | PDIP 28-pin package |
| Z8F08200100KITG | Development Kit (20- and 28-pin) | | | | | | | | | |
| ZUSBSC00100ZACG | USB Smart Cable Accessory Kit | | | | | | | | | |
| ZUSBOPTSC01ZACG | Opto-Isolated USB Smart Cable Accessory Kit | | | | | | | | | |

Visit the Zilog website at http://www.zilog.com for ordering information about Z8 Encore! XP® F0822 Series development tools and accessories.

## D



## E



## F