

Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	19
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0822pj020eg

Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page
Oct 2011	18	Added LDWX information to Load Instructions table, eZ8 CPU Instruction Summary table and to Second Op Code Map after 1FH figure; revised Flash Sector Protect Register description; revised Packaging chapter.	206 , 212 , 220 , 152 , 221
May 2008	17	Removed <i>Flash Microcontrollers</i> from the title throughout the document.	All
Feb 2008	16	Updated the flag status for BCLR, BIT, and BSET in eZ8 CPU Instruction Summary table.	208
Dec 2007	15	Updated Zilog logo/text, Foreword section. Updated Z8 Encore! 8K Series to Z8 Encore! XP [®] F0822 Series Flash Microcontrollers throughout the document.	All

Interrupt Request Control Registers	238
GPIO Control Registers	241
Watchdog Timer Control Registers	244
Flash Control Registers	246
Index	248
Customer Support	258

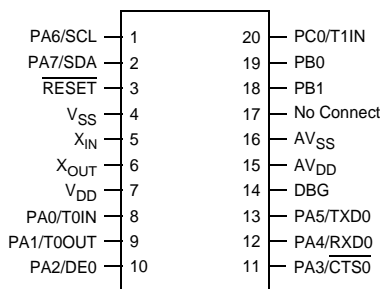


Figure 4. The Z8F0811 and Z8F0411 MCUs in 20-Pin SSOP and PDIP Packages

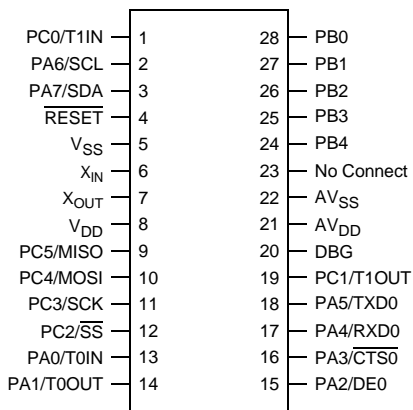


Figure 5. The Z8F0812 and Z8F0412 MCUs in 28-Pin SOIC and PDIP Packages

Port A–C Address Registers

The Port A–C Address registers, shown in Table 14, select the GPIO port functionality accessible through the Port A–C Control registers. The Port A–C Address and Control registers combine to provide access to all GPIO port control.

Table 14. Port A–C GPIO Address Registers (PxADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W							
Address	FD0H, FD4H, FD8H							

Bit	Description
[7:0]	Port Address
PADDR	The Port Address selects one of the subregisters accessible through the Port Control Register. 00H = No function. Provides some protection against accidental port reconfiguration. 01H = Data Direction. 02H = Alternate Function. 03H = Output Control (Open-Drain). 04H = High Drive Enable. 05H = Stop Mode Recovery Source Enable. 06H = Pull-up Enable. 07H–FFH = no function.

Architecture

Figure 10 displays the architecture of the timers.

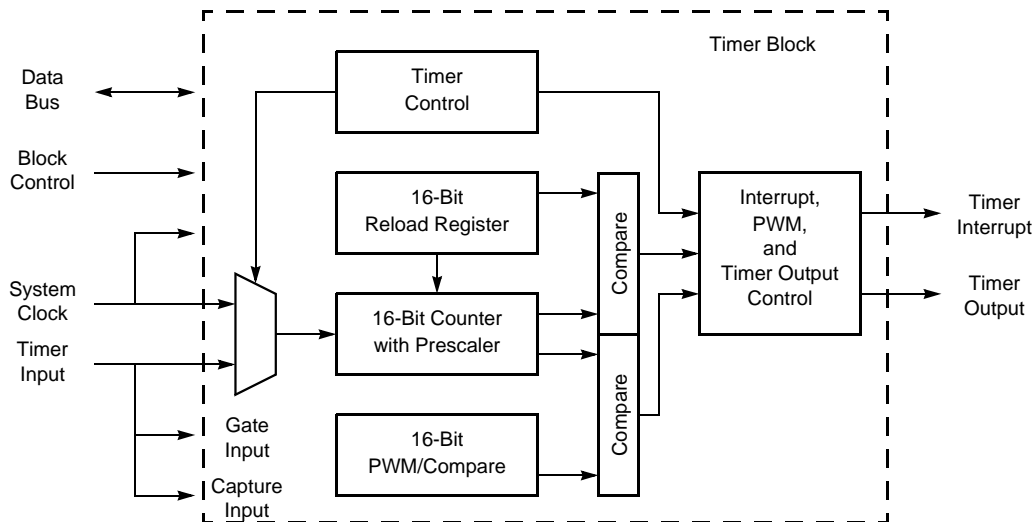


Figure 10. Timer Block Diagram

Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer rolls over to 0000H and continues counting.

Timer Operating Modes

The timers are configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt and the count value in the Timer High

Table 42. Timer 0–1 Reload Low Byte Register (TxRL)

Bit	7	6	5	4	3	2	1	0
Field	TRL							
RESET	1							
R/W	R/W							
Address	F03H, F0BH							

Bit	Description
[7] TRH, TRL	Timer Reload Register High and Low These two bytes form the 16-bit reload value, {TRH[7:0], TRL[7:0]}. This value sets the maximum count value which initiates a timer reload to 0001H. In COMPARE Mode, these two bytes form the 16-bit Compare value.

Timer 0–1 PWM High and Low Byte Registers

The Timer 0–1 PWM High and Low Byte (TxPWMH and TxPWML) registers, shown in Tables 43 and 44, are used for Pulse-Width Modulator (PWM) operations. These registers also store the Capture values for the CAPTURE and CAPTURE/COMPARE modes.

Table 43. Timer 0–1 PWM High Byte Register (TxPWMH)

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0							
R/W	R/W							
Address	F04H, F0CH							

Table 44. Timer 0–1 PWM Low Byte Register (TxPWML)

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0							
R/W	R/W							
Address	F05H, F0DH							

Bit	Description
[7:0] PWMH, PWML	Pulse-Width Modulator High and Low Bytes These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control (TxCTL) Register. The TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in CAPTURE or CAPTURE/COMPARE modes.

Timer 0–3 Control 0 Registers

The Timer 0–3 Control 0 (TxCTL0) registers, shown in Table 45, allow cascading of the Timers.

Table 45. Timer 0–3 Control 0 Registers (TxCTL0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved			CSC	Reserved			
RESET	0							
R/W	R/W							
Address	F06H, F0EH, F16H, F1EH							

Bit	Description
[7:5]	Reserved These bits are reserved and must be programmed to 000.
[4] CSC	Cascade Timers 0 = Timer Input signal comes from the pin. 1 = For Timer 0, input signal is connected to Timer 1 output. For Timer 1, the input signal is connected to the Timer 0 output.
[3:0]	Reserved These bits are reserved and must be programmed to 0000.

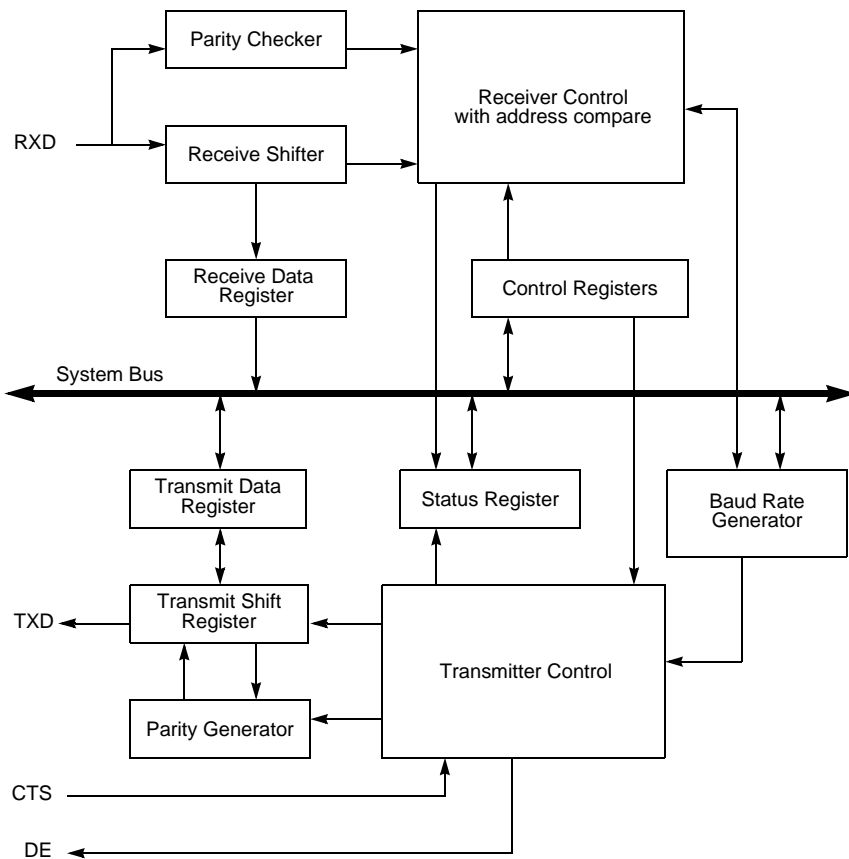


Figure 11. UART Block Diagram

Operation

The UART always transmits and receives data in an 8-bit data format, least-significant bit first. An even or odd parity bit is optionally added to the data stream. Each character begins with an active Low start bit and ends with either 1 or 2 active High stop bits. Figures 12 and 13 display the asynchronous data format used by the UART without parity and with parity, respectively.

Table 75. I²C Baud Rate Low Byte Register (I2CBRL)

Bit	7	6	5	4	3	2	1	0
Field	BRL							
RESET	FFH							
R/W	R/W							
Address	F54H							

Bit	Description
-----	-------------

[7:0] BRL	I²C Baud Rate Low Byte Least significant byte, BRG[7:0], of the I ² C Baud Rate Generator's reload value.
--------------	---

Note: If the DIAG bit in the I²C Diagnostic Control Register is set to 1, a read of the I2CBRL Register returns the current value of the I²C Baud Rate Counter [7:0].

I²C Diagnostic State Register

The I²C Diagnostic State Register, shown in Table 76, provides observability into the internal state. This register is read-only; it is used for I²C diagnostics and manufacturing test purposes.

Table 76. I²C Diagnostic State Register (I2CDST)

Bit	7	6	5	4	3	2	1	0
Field	SCLIN	SDAIN	STPCNT	TXRXSTATE				
RESET	X		0					
R/W	R							
Address	F55H							

Bit	Description
-----	-------------

[7] SCLIN	Serial Clock Input Value of the Serial Clock input signal.
[6] SDAIN	Serial Data Input Value of the Serial Data input signal.
[5] STPCNT	Stop Count Value of the internal Stop Count control signal.

Page Select Register

The Page Select (FPS) Register, shown in Table 86, selects the Flash memory page to be erased or programmed. Each Flash page contains 512 bytes of Flash memory. During a Page Erase operation, all Flash memory locations with the 7 most significant bits of the address provided by the PAGE field are erased to FFH.

The Page Select Register shares its Register File address with the Flash Sector Protect Register. The Page Select Register cannot be accessed when the Flash Sector Protect Register is enabled.

Table 86. Page Select Register (FPS)

Bit	7	6	5	4	3	2	1	0
Field	INFO_EN	PAGE						
RESET	0							
R/W	R/W							
Address	FF9H							

Bit	Description
[7] INFO_EN	Information Area Enable 0 = Information Area is not selected. 1 = Information Area is selected. The Information area is mapped into the Flash memory address space at addresses FE00H through FFFFH.
[6:0] PAGE	Page Select This 7-bit field selects the Flash memory page for Programming and Page Erase operations. Flash memory address[15:9] = PAGE[6:0].

Flash Sector Protect Register

The Flash Sector Protect Register, shown in Table 87, protects Flash memory sectors from being programmed or erased from user code. The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register can be accessed only after writing the Flash Control Register with 5EH.

User code can only write bits in this register to 1 (bits cannot be cleared to 0 by user code). To determine the appropriate Flash memory sector address range and sector number for your F0822 Series product, please refer to [Table 82](#) on page 143.

Electrical Characteristics

The data in this chapter represents all known data prior to qualification and characterization of the Z8 Encore! XP® F0822 Series of products, and is therefore subject to change. Additional electrical characteristics may be found in the individual chapters of this document.

Absolute Maximum Ratings

These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

! **Caution:** Stresses greater than those listed in Table 97 can cause permanent damage to the device.

Table 97. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	-40	+105	°C	1
Storage temperature	-65	+150	°C	
Voltage on any pin with respect to V_{SS}	-0.3	+5.5	V	2
Voltage on AV_{SS} pin with respect to V_{SS}	-0.3	+0.3	V	2
Voltage on V_{DD} pin with respect to V_{SS}	-0.3	+3.6	V	
Voltage on AV_{DD} pin with respect to V_{DD}	-0.3	+0.3	V	
Maximum current on input and/or inactive output pin	-5	+5	μA	
Maximum output current from active output pin	-25	+25	mA	
20-pin SSOP Package Maximum Ratings at -40°C to 70°C				
Total power dissipation		430	mW	
Maximum current into V_{DD} or out of V_{SS}		120	mA	

Note: This voltage applies to all pins except the following: V_{DD} , AV_{DD} , V_{REF} , pins that support analog input (Port B), and where otherwise noted.

Table 97. Absolute Maximum Ratings (Continued)

Parameter	Minimum	Maximum	Units	Notes
20-pin SSOP Package Maximum Ratings at 70°C to 105°C				
Total power dissipation		250	mW	
Maximum current into V_{DD} or out of V_{SS}		69	mA	
20-pin PDIP Package Maximum Ratings at -40°C to 70°C				
Total power dissipation		775	mW	
Maximum current into V_{DD} or out of V_{SS}		215	mA	
20-pin PDIP Package Maximum Ratings at 70°C to 105°C				
Total power dissipation		285	mW	
Maximum current into V_{DD} or out of V_{SS}		79	mA	
28-pin SOIC Package Maximum Ratings at -40°C to 70°C				
Total power dissipation		450	mW	
Maximum current into V_{DD} or out of V_{SS}		125	mA	
28-pin SOIC Package Maximum Ratings at 70°C to 105°C				
Total power dissipation		260	mW	
Maximum current into V_{DD} or out of V_{SS}		73	mA	
28-pin PDIP Package Maximum Ratings at -40°C to 70°C				
Total power dissipation		1100	mW	
Maximum current into V_{DD} or out of V_{SS}		305	mA	
28-pin PDIP Package Maximum Ratings at 70°C to 105°C				
Total power dissipation		400	mW	
Maximum current into V_{DD} or out of V_{SS}		110	mA	
Note: This voltage applies to all pins except the following: V_{DD} , AV_{DD} , V_{REF} , pins that support analog input (Port B), and where otherwise noted.				

AC Characteristics

Table 99 provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50pF on all outputs.

Table 99. AC Characteristics

Symbol	Parameter	$V_{DD} = 2.7-3.6V$ $T_A = -40^{\circ}C$ to $105^{\circ}C$		Units	Conditions
		Minimum	Maximum		
F_{SYSCLK}	System Clock Frequency (ROM)	–	20.0	MHz	
F_{SYSCLK}	System Clock Frequency (Flash)	–	20.0	MHz	Read-only from Flash memory.
		0.032768	20.0	MHz	Program or erasure of Flash memory.
F_{XTAL}	Crystal Oscillator Frequency	0.032768	20.0	MHz	System clock frequencies below the crystal oscillator minimum require an external clock driver.
T_{XIN}	System Clock Period	50	–	ns	$T_{CLK} = 1/F_{SYSCLK}$
T_{XINH}	System Clock High Time	20	30	ns	$T_{CLK} = 50ns$
T_{XINL}	System Clock Low Time	20	30	ns	$T_{CLK} = 50ns$

Figure 47 displays the input frequency response of the ADC.

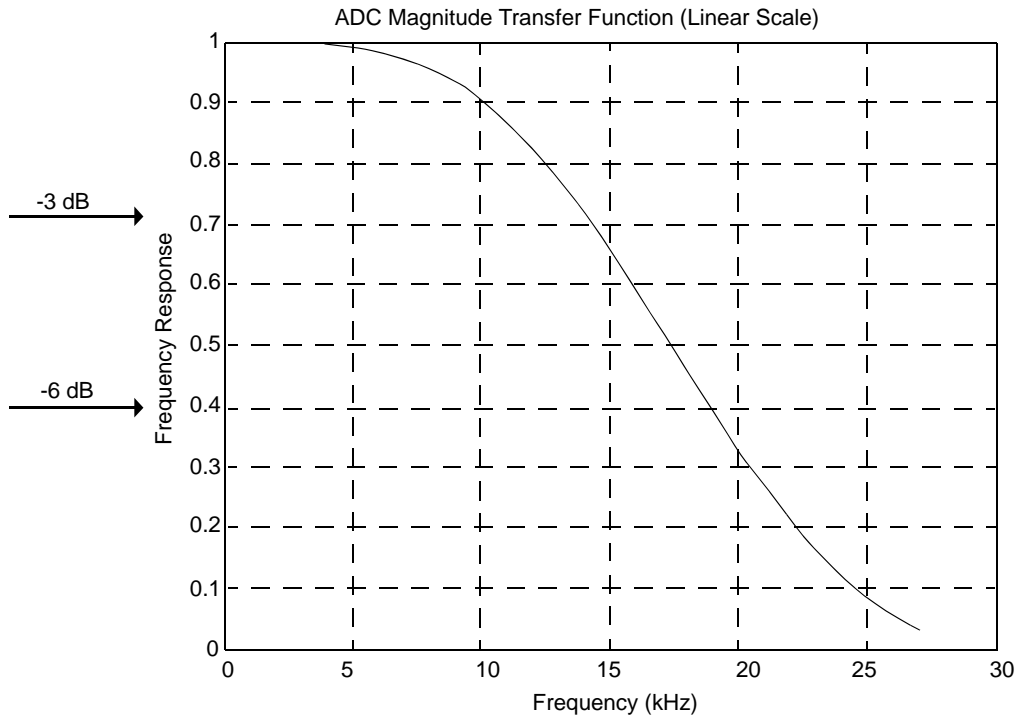


Figure 47. Analog-to-Digital Converter Frequency Response

On-Chip Debugger Timing

Figure 50 and Table 108 provide timing information for the DBG pin. The DBG pin timing specifications assume a 4µs maximum rise and fall time.

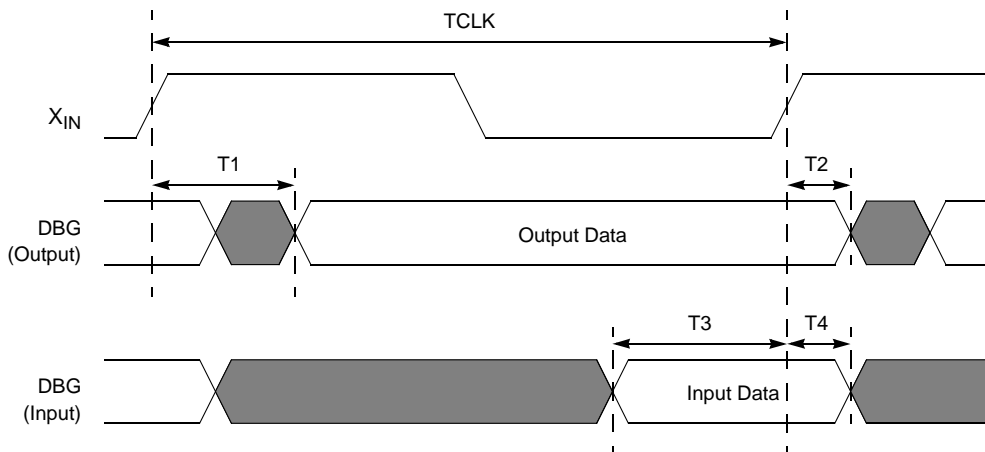


Figure 50. On-Chip Debugger Timing

Table 108. On-Chip Debugger Timing

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
DBG			
T ₁	X _{IN} Rise to DBG Valid Delay	–	15
T ₂	X _{IN} Rise to DBG Output Hold Time	2	–
T ₃	DBG to X _{IN} Rise Input Setup Time	10	–
T ₄	DBG to X _{IN} Rise Input Hold Time	5	–
	DBG frequency		System Clock/4

Table 127. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
ADD dst, src	dst ← dst + src	r	r	02	*	*	*	*	0	*	2	3
		r	lr	03							2	4
		R	R	04							3	3
		R	IR	05							3	4
		R	IM	06							3	3
		IR	IM	07							3	4
ADDX dst, src	dst ← dst + src	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09							4	3
AND dst, src	dst ← dst AND src	r	r	52	-	*	*	0	-	-	2	3
		r	lr	53							2	4
		R	R	54							3	3
		R	IR	55							3	4
		R	IM	56							3	3
		IR	IM	57							3	4
ANDX dst, src	dst ← dst AND src	ER	ER	58	-	*	*	0	-	-	4	3
		ER	IM	59							4	3
BCLR bit, dst	dst[bit] ← 0	r		E2	-	-	-	-	-	-	2	2
BIT p, bit, dst	dst[bit] ← p	r		E2	-	-	-	-	-	-	2	2
BRK	Debugger Break			00	-	-	-	-	-	-	1	1
BSET bit, dst	dst[bit] ← 1	r		E2	-	-	-	-	-	-	2	2
BSWAP dst	dst[7:0] ← dst[0:7]	R		D5	X	*	*	0	-	-	2	2
BTJ p, bit, src, dst	if src[bit] = p PC ← PC + X	r		F6	-	-	-	-	-	-	3	3
		lr		F7							3	4
BTJNZ bit, src, dst	if src[bit] = 1 PC ← PC + X	r		F6	-	-	-	-	-	-	3	3
		lr		F7							3	4
BTJZ bit, src, dst	if src[bit] = 0 PC ← PC + X	r		F6	-	-	-	-	-	-	3	3
		lr		F7							3	4

Note: Flags Notation:

* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 127. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
DECW dst	dst ← dst – 1	RR		80	-	*	*	*	-	-	2	5
		IRR		81							2	6
DI	IRQCTL[7] ← 0			8F	-	-	-	-	-	-	1	2
DJNZ dst, RA	dst ← dst – 1 if dst ≠ 0 PC ← PC + X	r		0A-FA	-	-	-	-	-	-	2	3
EI	IRQCTL[7] ← 1			9F	-	-	-	-	-	-	1	2
HALT	HALT Mode			7F	-	-	-	-	-	-	1	2
INC dst	dst ← dst + 1	R		20	-	*	*	*	-	-	2	2
		IR		21							2	3
		r		0E-FE							1	2
INCW dst	dst ← dst + 1	RR		A0	-	*	*	*	-	-	2	5
		IRR		A1							2	6
IRET	FLAGS ← @SP SP ← SP + 1 PC ← @SP SP ← SP + 2 IRQCTL[7] ← 1			BF	*	*	*	*	*	*	1	5
JP dst	PC ← dst	DA		8D	-	-	-	-	-	-	3	2
		IRR		C4							2	3
JP cc, dst	if cc is true PC ← dst	DA		0D-FD	-	-	-	-	-	-	3	2
JR dst	PC ← PC + X	DA		8B	-	-	-	-	-	-	2	2
JR cc, dst	if cc is true PC ← PC + X	DA		0B-FB	-	-	-	-	-	-	2	2

Note: Flags Notation:

* = Value is a function of the result of the operation.


- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 127. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
SRL dst		R		1F C0	*	*	0	*	-	-	3	2
		IR		1F C1								3
SRP src	RP ← src		IM	01	-	-	-	-	-	-	2	2
STOP	STOP Mode			6F	-	-	-	-	-	-	1	2
SUB dst, src	dst ← dst – src	r	r	22	*	*	*	*	1	*	2	3
		r	lr	23							2	4
		R	R	24							3	3
		R	IR	25							3	4
		R	IM	26							3	3
		IR	IM	27							3	4
SUBX dst, src	dst ← dst – src	ER	ER	28	*	*	*	*	1	*	4	3
		ER	IM	29							4	3
SWAP dst	dst[7:4] ↔ dst[3:0]	R		F0	X	*	*	X	-	-	2	2
		IR		F1							2	3
TCM dst, src	(NOT dst) AND src	r	r	62	-	*	*	0	-	-	2	3
		r	lr	63							2	4
		R	R	64							3	3
		R	IR	65							3	4
		R	IM	66							3	3
		IR	IM	67							3	4
TCMX dst, src	(NOT dst) AND src	ER	ER	68	-	*	*	0	-	-	4	3
		ER	IM	69							4	3

Note: Flags Notation:

* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Index

Numerics

10-bit ADC 4

A

absolute maximum ratings 176
AC characteristics 185
ADC 204
 architecture 136
 automatic power-down 137
 block diagram 137
 continuous conversion 138
 control register 139
 control register definitions 139
 data high byte register 141
 data low bits register 142
 electrical characteristics and timing 190
 operation 137
 single-shot conversion 137
ADCCCTL register 139
ADCDH register 141
ADCDL register 142
ADCX 204
ADD 204
additional symbols 202
address space 14
ADDX 204
analog signals 11
analog-to-digital converter (ADC) 136
AND 207
ANDX 207
arithmetic instructions 204
assembly language programming 199
assembly language syntax 200

B

B 202
b 201
baud rate generator, UART 88

BCLR 205
binary number suffix 202
BIT 205
bit 201
 clear 205
 manipulation instructions 205
 set 205
 set or clear 205
 swap 205, 208
 test and jump 207
 test and jump if non-zero 207
 test and jump if zero 207
block diagram 3
block transfer instructions 205
BRK 207
BSET 205
BSWAP 205, 208
BTJ 207
BTJNZ 207
BTJZ 207

C

CALL procedure 207
capture mode 68
capture/compare mode 69
cc 201
CCF 206
characteristics, electrical 176
clear 206
clock phase (SPI) 104
CLR 206
COM 207
compare 68
compare - extended addressing 204
compare mode 68
compare with carry 204
compare with carry - extended addressing 204
complement 207
complement carry flag 205, 206

PWM mode 68
PxADDR register 32, 241, 242, 243
PxCTL register 33, 241, 242, 243

R

R 201
r 201
RCF 205, 206
receive
 10-bit data format (I2C) 126
 7-bit data transfer format (I2C) 125
 IrDA data 99
receive interrupt 117
receiving UART data-interrupt-driven method 82
receiving UART data-pollled method 81
register 112, 201, 236
 ADC control (ADCCTL) 139
 ADC data high byte (ADCDH) 141
 ADC data low bits (ADC DL) 142
 baud low and high byte (I2C) 132, 133, 135
 baud rate high and low byte (SPI) 114
 control (SPI) 110
 control, I2C 131
 data, SPI 109
 flash control (FCTL) 150, 246
 flash high and low byte (FFREQH and FRE-
 EQL) 153
 flash page select (FPS) 152
 flash status (FSTAT) 151
 GPIO port A-H address (PxADDR) 32, 241,
 242, 243
 GPIO port A-H alternate function sub-registers
 34
 GPIO port A-H control address (PxCTL) 33,
 241, 242, 243
 GPIO port A-H data direction sub-registers 33
 I2C baud rate high (I2CBRH) 132, 133, 135,
 234
 I2C control (I2CCTL) 131, 233
 I2C data (I2CDATA) 129, 233
 I2C status 129, 233
 I2C status (I2CSTAT) 129, 233
 I2Cbaud rate low (I2CBRL) 133, 234

mode, SPI 112
OCD control 169
OCD status 171
SPI baud rate high byte (SPIBRH) 114, 236
SPI baud rate low byte (SPIBRL) 114, 237
SPI control (SPICTL) 110, 235
SPI data (SPIDATA) 109, 235
SPI status (SPISTAT) 111, 235
status, I2C 129
status, SPI 111
UARTx baud rate high byte (UxBRH) 95, 232
UARTx baud rate low byte (UxBRL) 95, 232
UARTx Control 0 (UxCTL0) 92, 94, 231, 232
UARTx control 1 (UxCTL1) 93, 231
UARTx receive data (UxRXD) 89, 230
UARTx status 0 (UxSTAT0) 90, 231
UARTx status 1 (UxSTAT1) 91, 231
UARTx transmit data (UxTXD) 89, 230
watch-dog timer control (WDTCTL) 74, 244
watch-dog timer reload high byte (WDTH) 75,
245
watch-dog timer reload low byte (WDTL) 76,
245
watch-dog timer reload upper byte (WDTU)
75, 245
register address (RA) 202
register file 14
register file address map 17
register pair 202
register pointer 202
reset
 and stop mode characteristics 21
 and stop mode recovery 21
 carry flag 205
 controller 5
 sources 22
RET 207
return 207
RL 208
RLC 208
rotate and shift instructions 208
rotate left 208
rotate left through carry 208
rotate right 208