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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "[Embedded - Microcontrollers](#)"

##### Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	41
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/atmega3209-afr">https://www.e-xfl.com/product-detail/microchip-technology/atmega3209-afr</a>

# ATmega3209/4809 – 48-pin Data Sheet

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- SleepWalking peripherals
- Power Down with limited wake-up functionality
- Peripherals
  - One 16-bit Timer/Counter type A with dedicated period register, three compare channels (TCA)
  - Four 16-bit Timer/Counter type B with input capture (TCB)
  - One 16-bit Real Time Counter (RTC) running from external crystal or internal RC oscillator
  - Four USART with fractional baud rate generator, autobaud, and start-of-frame detection
  - Master/slave Serial Peripheral Interface (SPI)
  - Dual mode Master/Slave TWI with dual address match
    - Standard mode (Sm, 100 kHz)
    - Fast mode (Fm, 400 kHz)
    - Fast mode plus (Fm+, 1 MHz)
  - Event System for CPU independent and predictable inter-peripheral signaling
  - Configurable Custom Logic (CCL) with up to four programmable Lookup Tables (LUT)
  - One Analog Comparator (AC) with scalable reference input
  - One 10-bit 150 ksps Analog to Digital Converter (ADC)
  - Five selectable internal voltage references: 0.55V, 1.1V, 1.5V, 2.5V, and 4.3V
  - CRC code memory scan hardware
    - Optional automatic scan after reset
  - Watchdog Timer (WDT) with Window Mode, with separate on-chip oscillator
  - External interrupt on all general purpose pins
- I/O and Packages:
  - 41 programmable I/O lines
  - 48-pin UQFN 6x6 and TQFP 7x7
- Temperature Range: -40°C to 125°C
- Speed Grades:
  - 0-5 MHz @ 1.8V – 5.5V
  - 0-10 MHz @ 2.7V – 5.5V
  - 0-20 MHz @ 4.5V – 5.5V, -40°C to 105°C

# ATmega3209/4809 – 48-pin Data Sheet

## Ordering Information

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### 1. Ordering Information

Find available ordering options online at [microchipdirect.com](http://microchipdirect.com), or contact your local sales representative.

## 4. I/O Multiplexing and Considerations

### 4.1 Multiplexed Signals

QFN48/ TQFP48	Pin name <sup>(1,2)</sup>	Special	ADC0	AC0	USARTn	SPI0	TWI0	TCA0	TCBn	Other	CCL-LUTn
44	PA0	EXTCLK			0,TxD			0-WO0			0-IN0
45	PA1				0,RxD			0-WO1			0-IN1
46	PA2	TWI			0,XCK		SDA(MS)	0-WO2	0-WO	EVOUTA	0-IN2
47	PA3	TWI			0,XDIR		SCL(MS)	0-WO3	1-WO		0-OUT
48	PA4				0,TxD <sup>(3)</sup>	MOSI		0-WO4			
1	PA5				0,RxD <sup>(3)</sup>	MISO		0-WO5			
2	PA6				0,XCK <sup>(3)</sup>	SCK					0-OUT <sup>(3)</sup>
3	PA7	CLKOUT		OUT	0,XDIR <sup>(3)</sup>	SS				EVOUTA <sup>(3)</sup>	
4	PB0				3,TxD			0-WO0 <sup>(3)</sup>			
5	PB1				3,RxD			0-WO1 <sup>(3)</sup>			
6	PB2				3,XCK			0-WO2 <sup>(3)</sup>		EVOUTB	
7	PB3				3,XDIR			0-WO3 <sup>(3)</sup>			
8	PB4				3,TxD <sup>(3)</sup>			0-WO4 <sup>(3)</sup>	2-WO <sup>(3)</sup>		
9	PB5				3,RxD <sup>(3)</sup>			0-WO5 <sup>(3)</sup>	3-WO		
10	PC0				1,TxD	MOSI <sup>(3)</sup>		0-WO0 <sup>(3)</sup>	2-WO		1-IN0
11	PC1				1,RxD	MISO <sup>(3)</sup>		0-WO1 <sup>(3)</sup>	3-WO <sup>(3)</sup>		1-IN1
12	PC2	TWI			1,XCK	SCK <sup>(3)</sup>	SDA(MS) <sup>(3)</sup>	0-WO2 <sup>(3)</sup>		EVOUTC	1-IN2
13	PC3	TWI			1,XDIR	SS <sup>(3)</sup>	SCL(MS) <sup>(3)</sup>	0-WO3 <sup>(3)</sup>			1-OUT
14	VDD										
15	GND										
16	PC4				1,TxD <sup>(3)</sup>			0-WO4 <sup>(3)</sup>			
17	PC5				1,RxD <sup>(3)</sup>			0-WO5 <sup>(3)</sup>			
18	PC6				1,XCK <sup>(3)</sup>						1-OUT <sup>(3)</sup>
19	PC7				1,XDIR <sup>(3)</sup>				EVOUTC <sup>(3)</sup>		
20	PD0		AIN0					0-WO0 <sup>(3)</sup>			2-IN0
21	PD1		AIN1	P3				0-WO1 <sup>(3)</sup>			2-IN1
22	PD2		AIN2	P0				0-WO2 <sup>(3)</sup>		EVOUTD	2-IN2
23	PD3		AIN3	N0				0-WO3 <sup>(3)</sup>			2-OUT
24	PD4		AIN4	P1				0-WO4 <sup>(3)</sup>			
25	PD5		AIN5	N1				0-WO5 <sup>(3)</sup>			
26	PD6		AIN6	P2							2-OUT <sup>(3)</sup>
27	PD7	VREFA	AIN7	N2						EVOUTD <sup>(3)</sup>	
28	AVDD										
29	GND										
30	PE0		AIN8			MOSI <sup>(3)</sup>		0-WO0 <sup>(3)</sup>			
31	PE1		AIN9			MISO <sup>(3)</sup>		0-WO1 <sup>(3)</sup>			
32	PE2		AIN10			SCK <sup>(3)</sup>		0-WO2 <sup>(3)</sup>		EVOUTE	
33	PE3		AIN11			SS <sup>(3)</sup>		0-WO3 <sup>(3)</sup>			
34	PF0	TOSC1			2,TxD			0-WO0 <sup>(3)</sup>			3-IN0
35	PF1	TOSC2			2,RxD			0-WO1 <sup>(3)</sup>			3-IN1
36	PF2	TWI	AIN12		2,XCK		SDA(S) <sup>(3)</sup>	0-WO2 <sup>(3)</sup>		EVOUTF	3-IN2
37	PF3	TWI	AIN13		2,XDIR		SCL(S) <sup>(3)</sup>	0-WO3 <sup>(3)</sup>			3-OUT

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## I/O Multiplexing and Considerations

QFN48/ TQFP48	Pin name <a href="#">(1,2)</a>	Special	ADC0	AC0	USARTn	SPI0	TWI0	TCA0	TCBn	Other	CCL-LUTn
38	PF4		AIN14		2,TxD <sup>(3)</sup>			0-WO4 <sup>(3)</sup>	0-WO <sup>(3)</sup>		
39	PF5		AIN15		2,RxD <sup>(3)</sup>			0-WO5 <sup>(3)</sup>	1-WO <sup>(3)</sup>		
40	PF6	RESET			2,XCK <sup>(3)</sup>						3-OUT <sup>(3)</sup>
41	UPDI										
42	VDD										
43	GND										

**Note:**

1. Pin names are of type Px $n$ , with x being the PORT instance (A,B,C, ...) and n the pin number.  
Notation for signals is PORTx\_PINn. All pins can be used as event input.
2. All pins can be used for external interrupt, where pins Px2 and Px6 of each port have full asynchronous detection.
3. Alternate pin positions. For selecting the alternate positions, refer to the PORTMUX documentation.

**Table 5-10. Brownout Detection (BOD) Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$V_{BOD}$	BOD detection level (falling)	BODLEVEL=1.8V	1.71	1.78	1.85	V
		BODLEVEL=2.7V	2.45	2.60	2.75	
		BODLEVEL=4.3V	4.05	4.25	4.45	
$V_{HYS}$	Hysteresis	BODLEVEL=1.8V	-	25	-	mV
		BODLEVEL=2.7V	-	40	-	
		BODLEVEL=4.3V	-	80	-	
$t_{BOD}$	Detection time	Continuous	-	7	-	μs
		Sampled, 1 kHz	-	1	-	ms
		Sampled, 125 Hz	-	8	-	
$t_{startup}$	Start-up time	Time from enable to ready	-	40	-	μs
$\Delta V_{LVD}$	Interrupt level 0	Percentage above the selected BOD level	-	4	-	%
	Interrupt level 1		-	13	-	
	Interrupt level 2		-	25	-	

## 5.7 External Reset Characteristics

**Table 5-11. External Reset Characteristics**

Mode	Description	Condition	Min.	Typ.	Max.	Unit
$V_{VIH\_RST}$	Input Voltage for $\overline{RESET}$		0.7× $V_{DD}$	-	$V_{DD}+0.2$	V
$V_{VIL\_RST}$	Input Low Voltage for $\overline{RESET}$		-0.2	-	0.3× $V_{DD}$	
$t_{MIN\_RST}$	Minimum pulse width on $\overline{RESET}$ pin		300	-	-	ns
$R_p_{\_RST}$	RESET pull-up resistor	$V_{Reset}=0V$	20	35	50	kΩ

## 5.8 Oscillators and Clocks

Operating conditions:

- $V_{DD}=3V$ , except where specified otherwise.

**Table 5-12. 20 MHz Internal Oscillator (OSC20M) Characteristics**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$f_{OSC20M}$	Factory calibration frequency	FREQSEL=0	$T_A=25^{\circ}\text{C}, 3.0\text{V}$	16		MHz
		FREQSEL=1		20		
$f_{CAL}$	Frequency calibration range	OSC16M <sup>(2)</sup>		14.5		17.5 MHz
		OSC20M <sup>(2)</sup>		18.5		21.5 MHz

## 5.9 I/O Pin Characteristics

**Table 5-16. I/O Pin Characteristics ( $T_A=[-40, 85]^\circ\text{C}$ ,  $V_{DD}=[1.8, 5.5]\text{V}$  unless otherwise noted)**

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$V_{IL}$	Input Low Voltage		-0.2	-	$0.3 \times V_{DD}$	V
$V_{IH}$	Input High Voltage		$0.7 \times V_{DD}$	-	$V_{DD}+0.2\text{V}$	V
$I_{IH} / I_{IL}$	I/O pin Input Leakage Current	$V_{DD}=5.5\text{V}$ , Pin high	-	< 0.05	-	$\mu\text{A}$
		$V_{DD}=5.5\text{V}$ , Pin low	-	< 0.05	-	
$V_{OL}$	I/O pin drive strength	$V_{DD}=1.8\text{V}$ , $I_{OL}=1.5\text{ mA}$	-	-	0.36	V
		$V_{DD}=3.0\text{V}$ , $I_{OL}=7.5\text{ mA}$	-	-	0.6	
		$V_{DD}=5.0\text{V}$ , $I_{OL}=15\text{ mA}$	-	-	1	
$V_{OH}$	I/O pin drive strength	$V_{DD}=1.8\text{V}$ , $I_{OH}=1.5\text{ mA}$	1.44	-	-	V
		$V_{DD}=3.0\text{V}$ , $I_{OH}=7.5\text{ mA}$	2.4	-	-	
		$V_{DD}=5.0\text{V}$ , $I_{OH}=15\text{ mA}$	4	-	-	
$I_{total}$	Maximum combined I/O sink/source current per pin group <sup>(1)</sup>		-	-	100	mA
	Maximum combined I/O sink/source current per pin group <sup>(1)</sup>	$T_A=25^\circ\text{C}$	-	-	200	
$t_{RISE}$	Rise time	$V_{DD}=3.0\text{V}$ , load=20 pF	-	2.5	-	ns
		$V_{DD}=5.0\text{V}$ , load=20 pF	-	1.5	-	
		$V_{DD}=3.0\text{V}$ , load=20 pF, slew rate enabled	-	19	-	
		$V_{DD}=5.0\text{V}$ , load=20 pF, slew rate enabled	-	9	-	
$t_{FALL}$	Fall time	$V_{DD}=3.0\text{V}$ , load=20 pF	-	2.0	-	ns
		$V_{DD}=5.0\text{V}$ , load=20 pF	-	1.3	-	
		$V_{DD}=3.0\text{V}$ , load=20 pF, slew rate enabled	-	21	-	
		$V_{DD}=5.0\text{V}$ , load=20 pF, slew rate enabled	-	11	-	
$C_{pin}$	I/O pin capacitance except for TOSC, VREFA, and TWI pins		-	3.5	-	pF
$C_{pin}$	I/O pin capacitance on TOSC pins		-	4	-	pF
$C_{pin}$	I/O pin capacitance on TWI pins		-	10	-	pF
$C_{pin}$	I/O pin capacitance on VREFA pin		-	14	-	pF
$R_p$	Pull-up resistor		20	35	50	kΩ

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## Electrical Characteristics

**Table 5-21. Clock and Timing Characteristics**

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
$f_{ADC}$	Sample rate	$1.1V \leq V_{REF}$	15	-	115	ksps
		$1.1V \leq V_{REF}$ (8-bit resolution)	15	-	150	
		$V_{REF}=0.55V$ (10 bits)	7.5	-	20	
$CLK_{ADC}$	Clock frequency	$V_{REF}=0.55V$ (10 bits)	100	-	260	kHz
		$1.1V \leq V_{REF}$ (10 bits)	200	-	1500	
		$1.1V \leq V_{REF}$ (8-bit resolution)	200	-	2000	
$T_s$	Sampling time		2	2	33	$CLK_{ADC}$ cycles
$T_{CONV}$	Conversion time (latency)	Sampling time = 2 $CLK_{ADC}$	8.7	-	50	$\mu s$
$T_{START}$	Start-up time	Internal $V_{REF}$	-	22	-	$\mu s$

**Table 5-22. Accuracy Characteristics Internal Reference<sup>(2)</sup>**

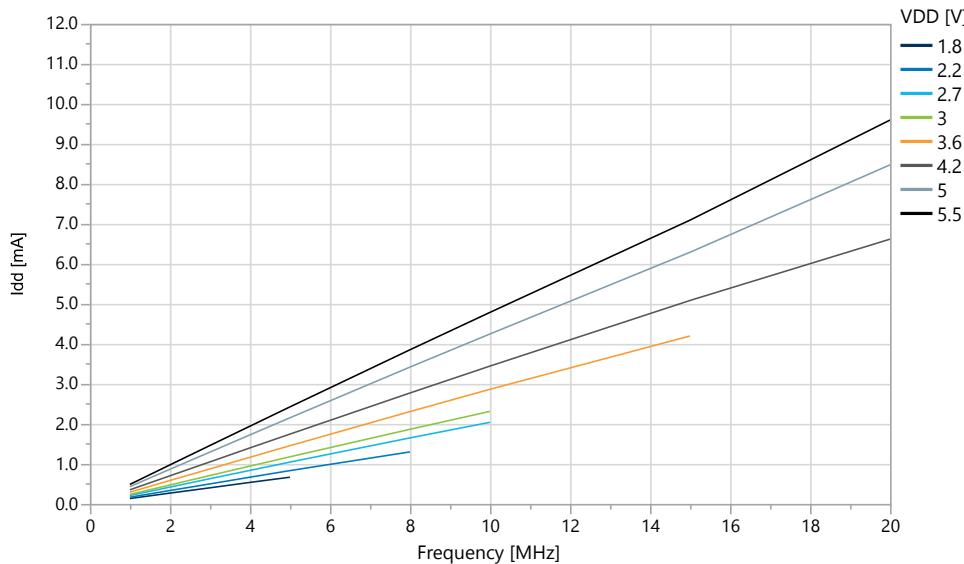
Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
Res	Resolution		-	10	-	bit
INL	Integral Non-linearity	REFSEL = INTERNAL $V_{REF}=0.55V$	$f_{ADC}=7.7$ ksps	-	1.0	-
		REFSEL = INTERNAL or VDD	$f_{ADC}=15$ ksps	-	1.0	-
		REFSEL = INTERNAL or VDD $1.1V \leq V_{REF}$	$f_{ADC}=77$ ksps	-	1.0	-
			$f_{ADC}=115$ ksps	-	1.2	-
DNL <sup>(1)</sup>	Differential Non-linearity	REFSEL = INTERNAL $V_{REF} = 0.55V$	$f_{ADC}=7.7$ ksps	-	0.6	-
		REFSEL = INTERNAL $V_{REF} = 1.1V$	$f_{ADC}=15$ ksps	-	0.4	-
		REFSEL = INTERNAL or VDD $1.5V \leq V_{REF}$	$f_{ADC}=15$ ksps	-	0.4	-
		REFSEL = INTERNAL or VDD $1.1V \leq V_{REF}$	$f_{ADC}=77$ ksps	-	0.4	-

## 6. Typical Characteristics

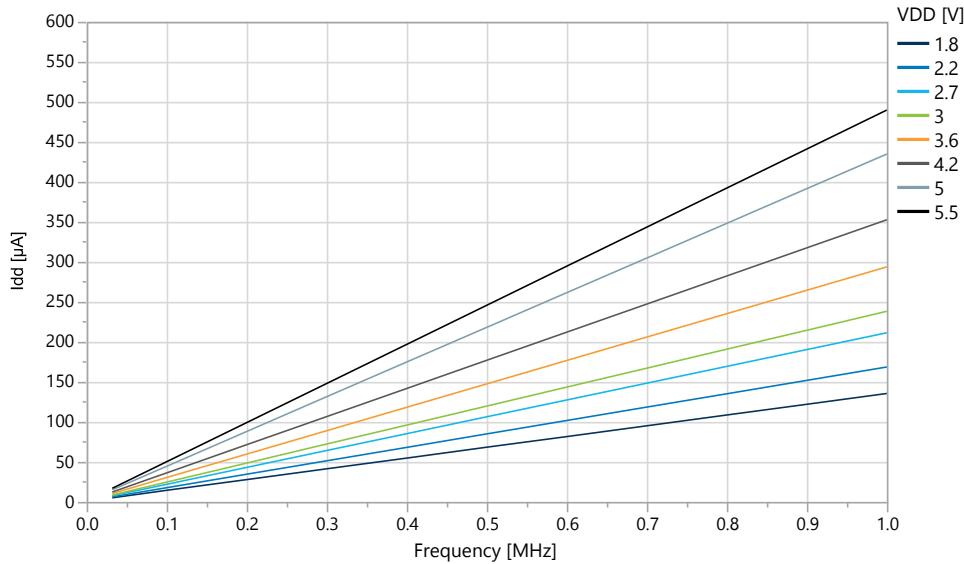
### 6.1 Power Consumption

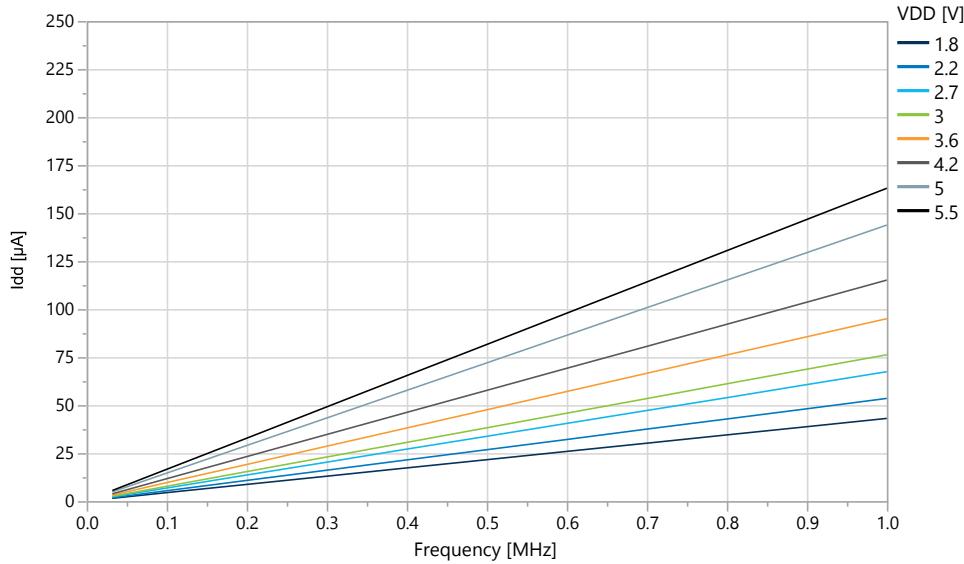
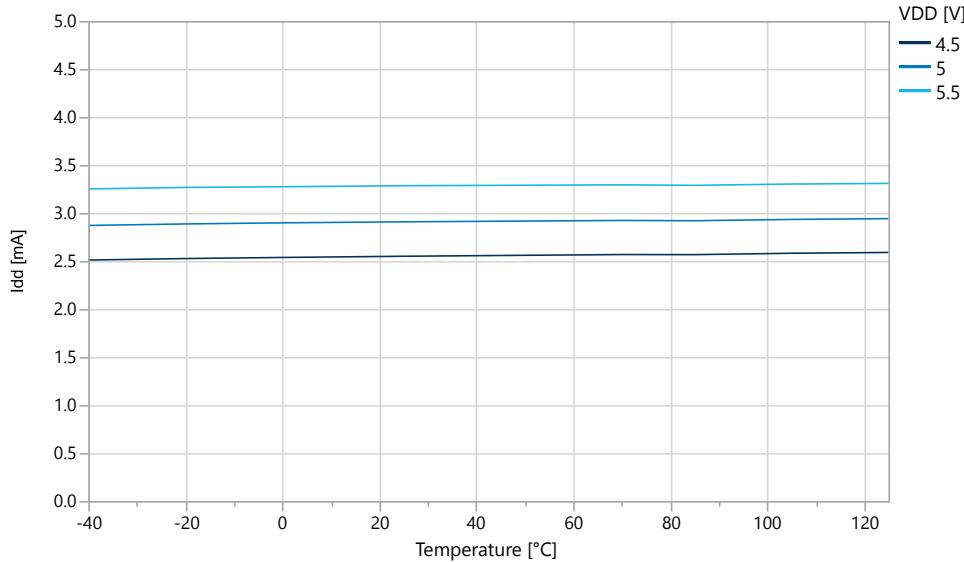
#### 6.1.1 Supply Currents in Active Mode

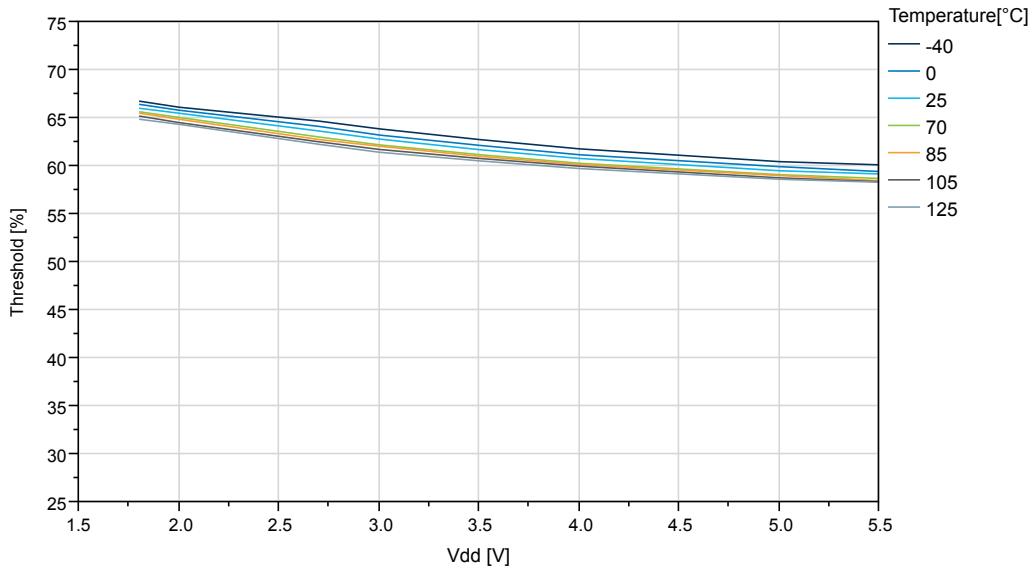
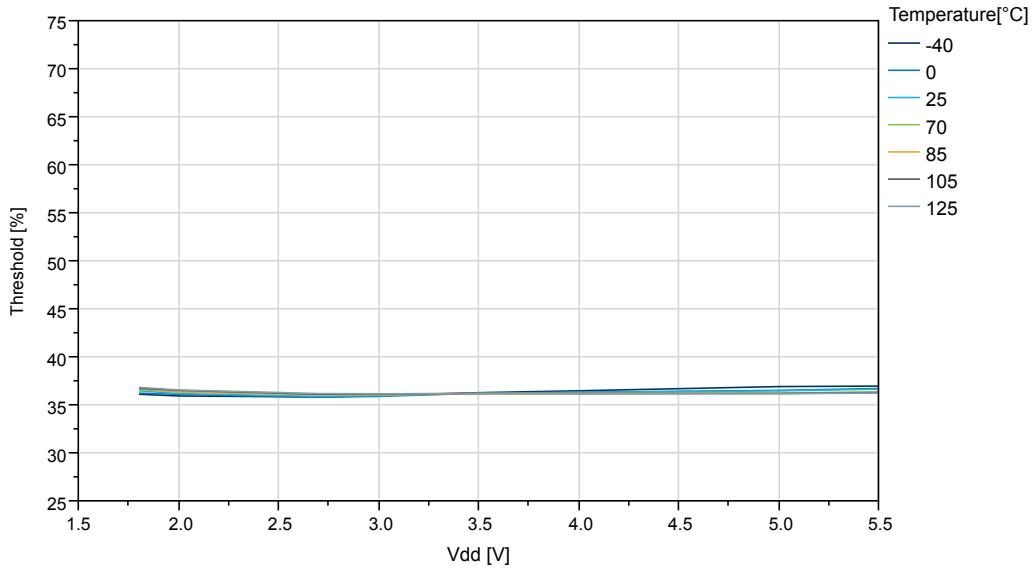
**Figure 6-1. Active Supply Current vs. Frequency (1-20 MHz) at T=25°C**

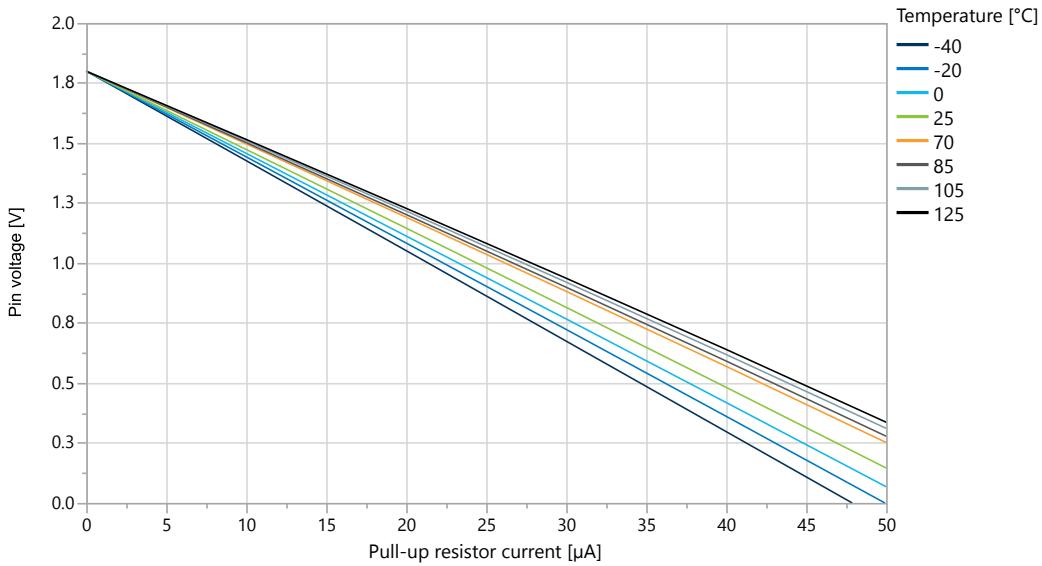
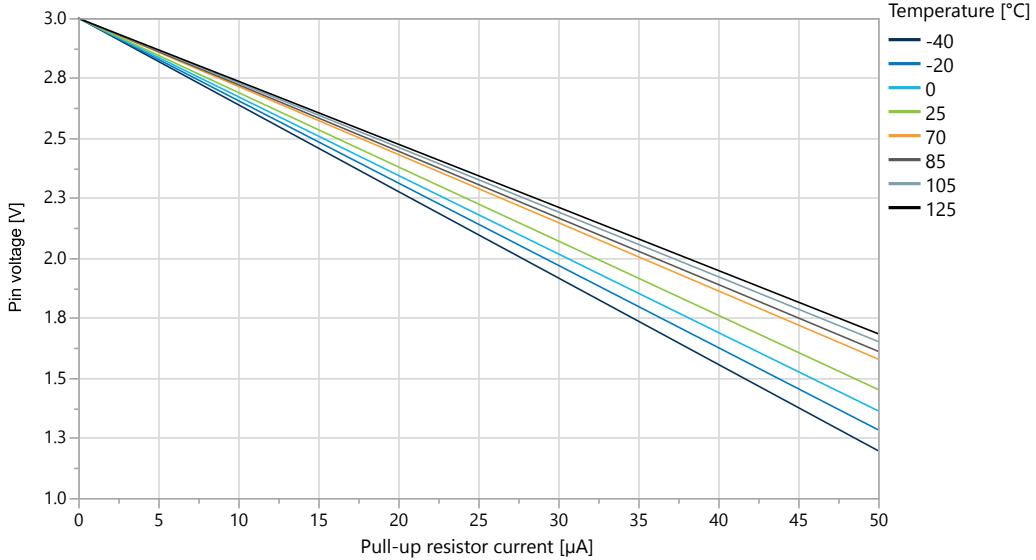


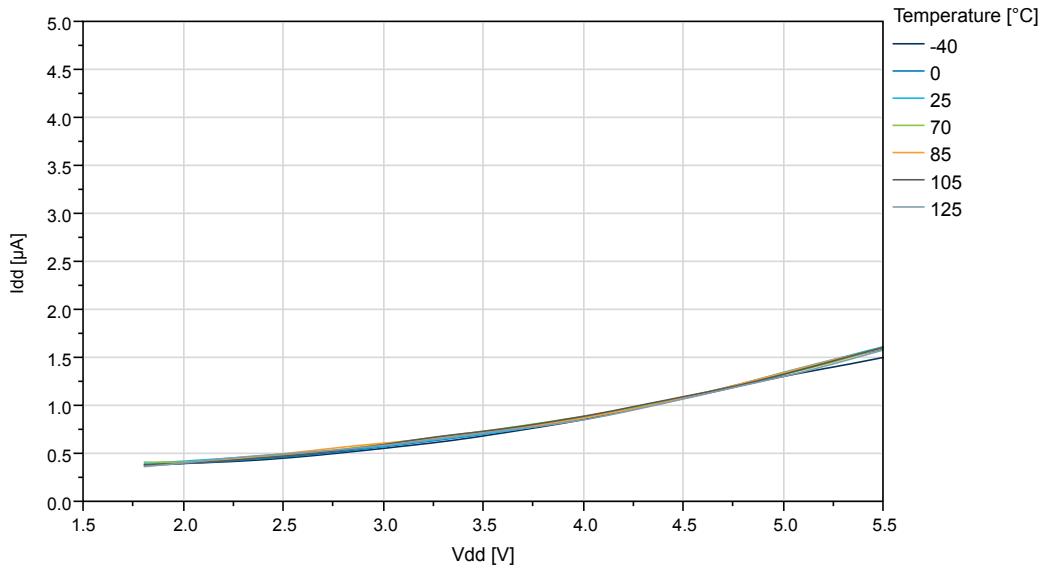
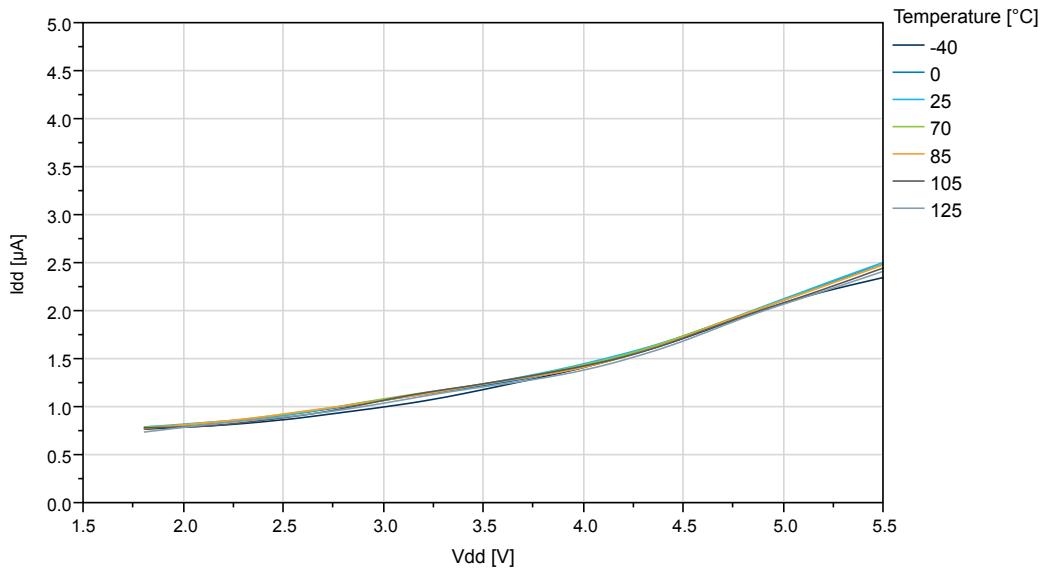
**Figure 6-2. Active Supply Current vs. Frequency [0.1, 1.0] MHz at T=25°C**



**Figure 6-7. Idle Supply Current vs. Low Frequency (0.1-1.0 MHz) at T=25°C****Figure 6-8. Idle Supply Current vs. Temperature (f=20 MHz OSC20M)**

**Figure 6-19. I/O Pin Input Threshold Voltage vs.  $V_{DD}$  ( $V_{IH}$ )****Figure 6-20. I/O Pin Input Threshold Voltage vs.  $V_{DD}$  ( $V_{IL}$ )**

**GPIO Pull-Up Characteristics****Figure 6-29. I/O Pin Pull-Up Resistor Current vs. Input Voltage ( $V_{DD}=1.8V$ )****Figure 6-30. I/O Pin Pull-Up Resistor Current vs. Input Voltage ( $V_{DD}=3.0V$ )**

**Figure 6-37. BOD Current vs.  $V_{DD}$  (Sampled BOD at 125 Hz)****Figure 6-38. BOD Current vs.  $V_{DD}$  (Sampled BOD at 1 kHz)**

# ATmega3209/4809 – 48-pin Data Sheet

## Typical Characteristics

Figure 6-45. DNL vs.  $V_{ref}$  ( $V_{DD}=5.0V$ ,  $f_{ADC}=115$  ksps), REFSEL = Internal Reference

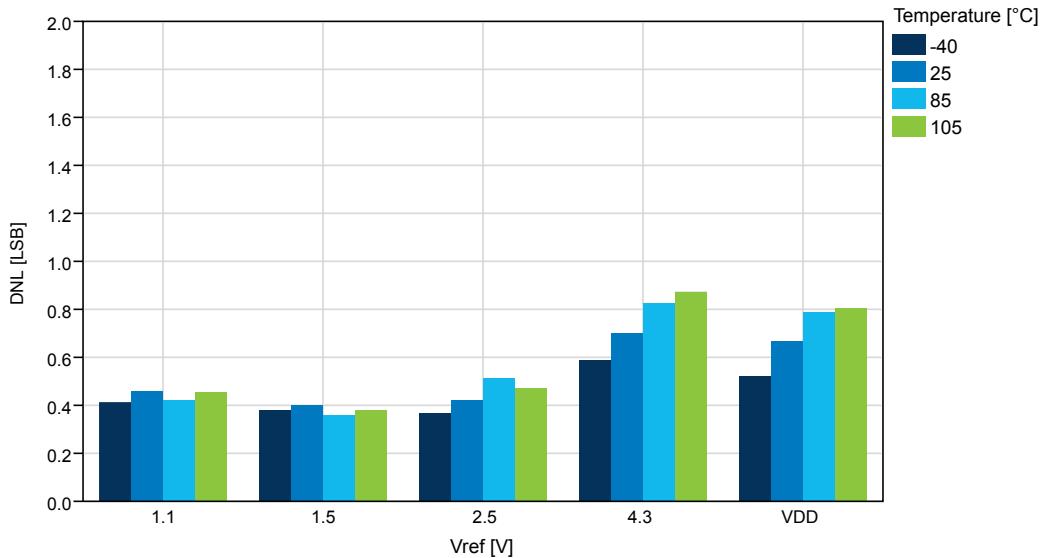
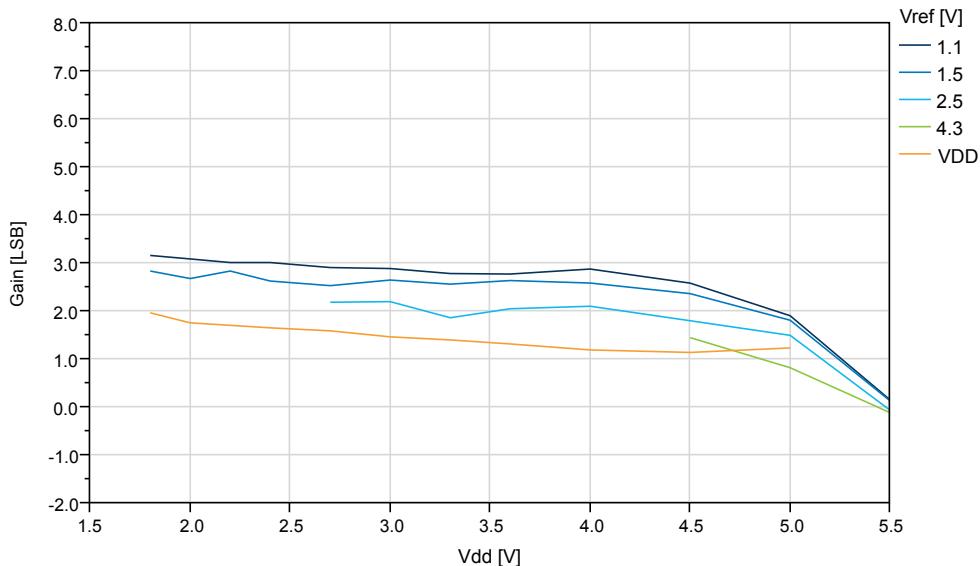
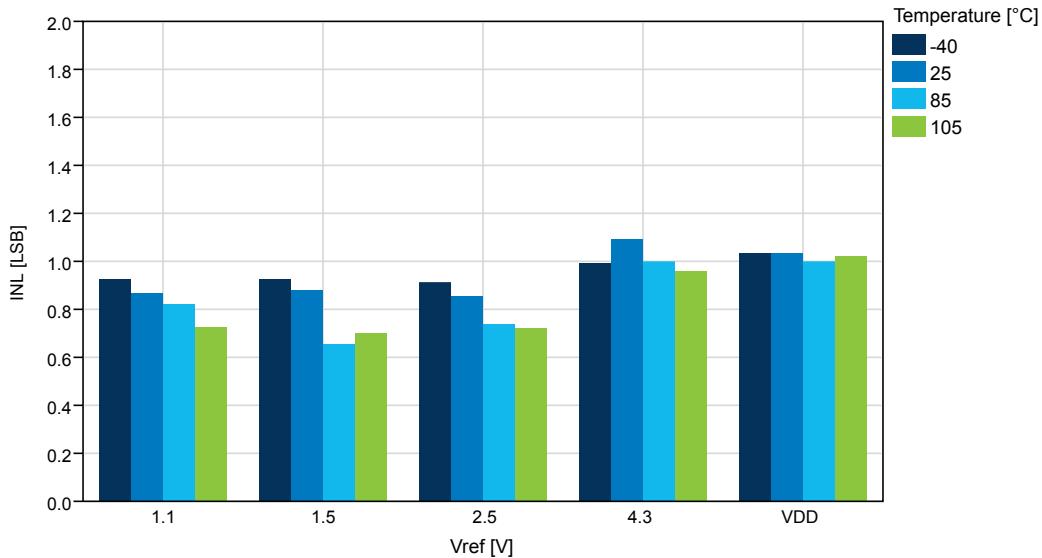
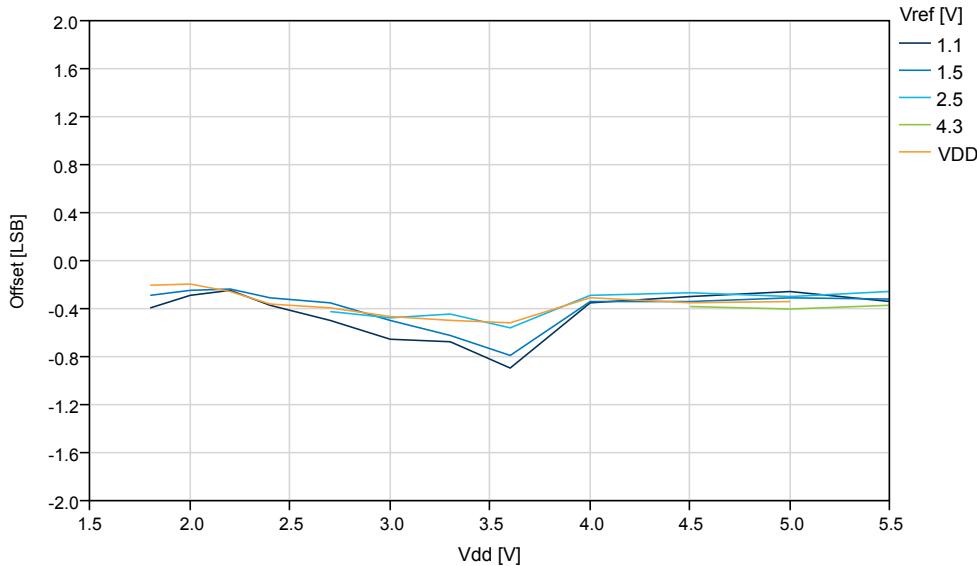


Figure 6-46. Gain Error vs.  $V_{DD}$  ( $f_{ADC}=115$  ksps) at  $T=25^{\circ}\text{C}$ , REFSEL = Internal Reference



**Figure 6-49. INL vs.  $V_{ref}$  ( $V_{DD}=5.0V$ ,  $f_{ADC}=115$  ksps), REFSEL = Internal Reference****Figure 6-50. Offset Error vs.  $V_{DD}$  ( $f_{ADC}=115$  ksps) at  $T=25^{\circ}C$ , REFSEL = Internal Reference**

# ATmega3209/4809 – 48-pin Data Sheet

## Typical Characteristics

Figure 6-51. Offset Error vs.  $V_{ref}$  ( $V_{DD}=5.0V$ ,  $f_{ADC}=115$  kspS), REFSEL = Internal Reference

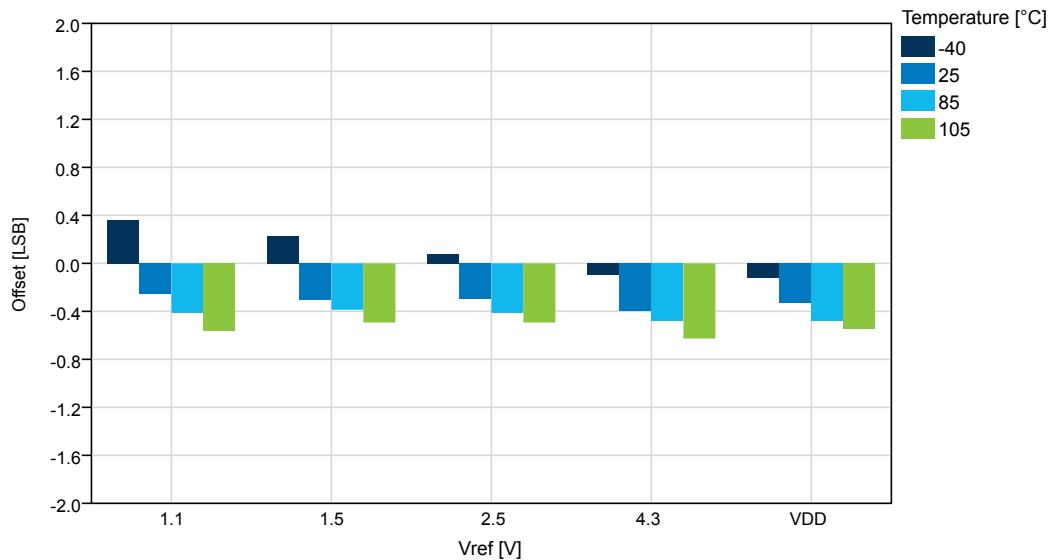
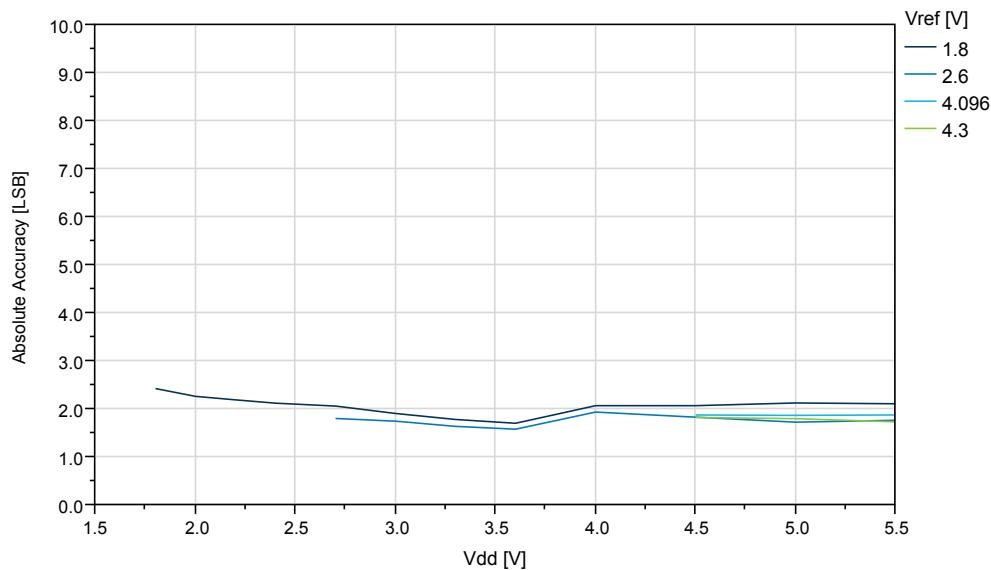
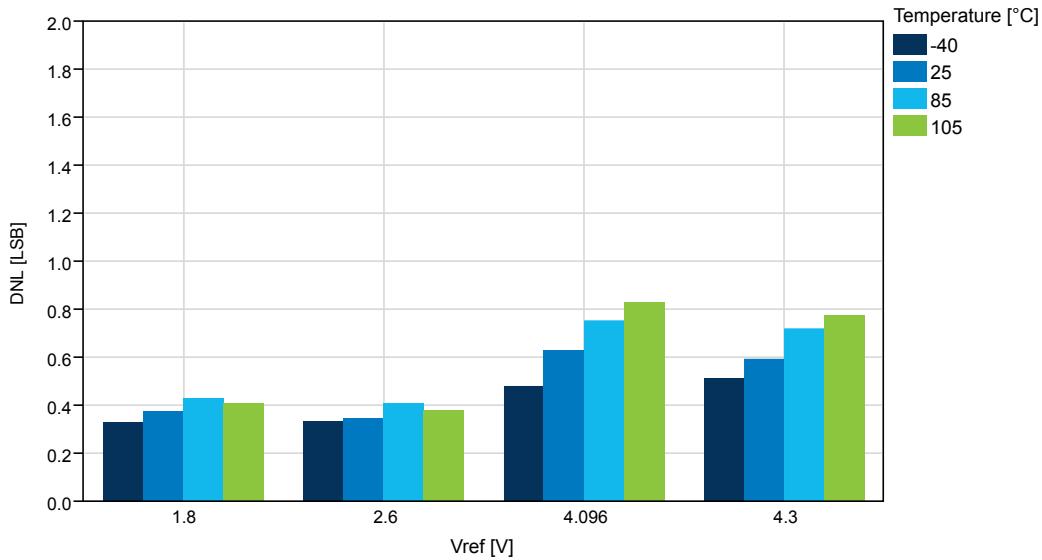
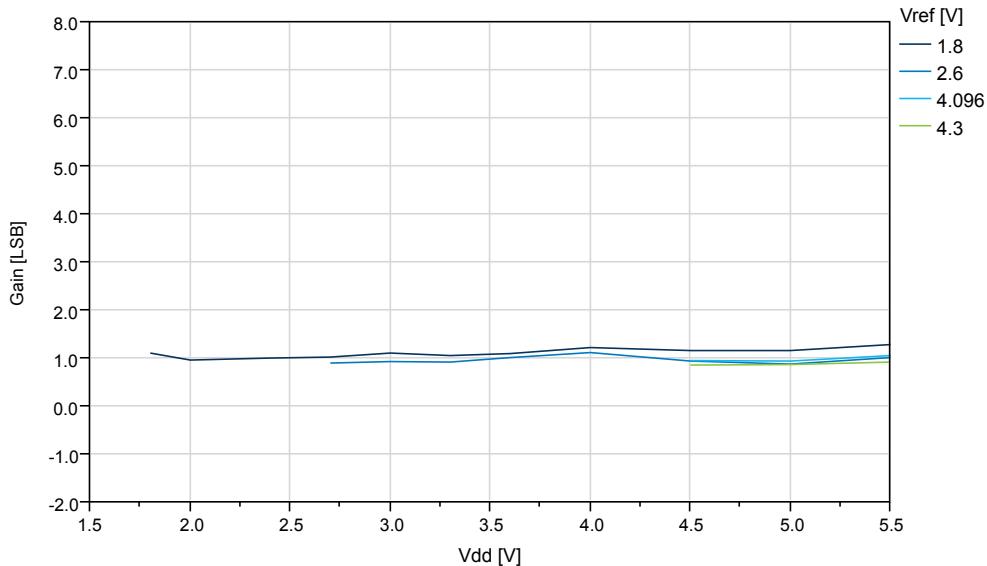
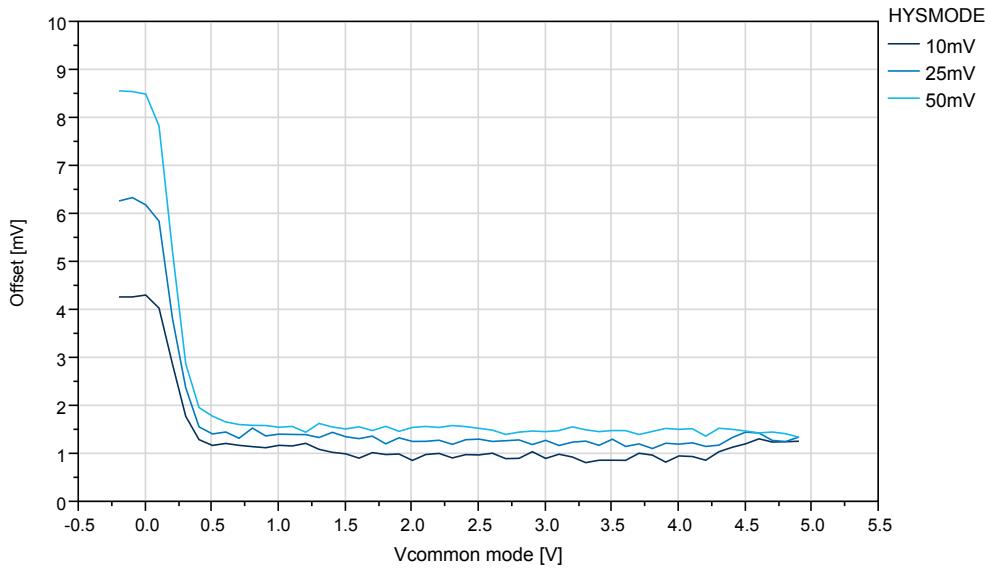


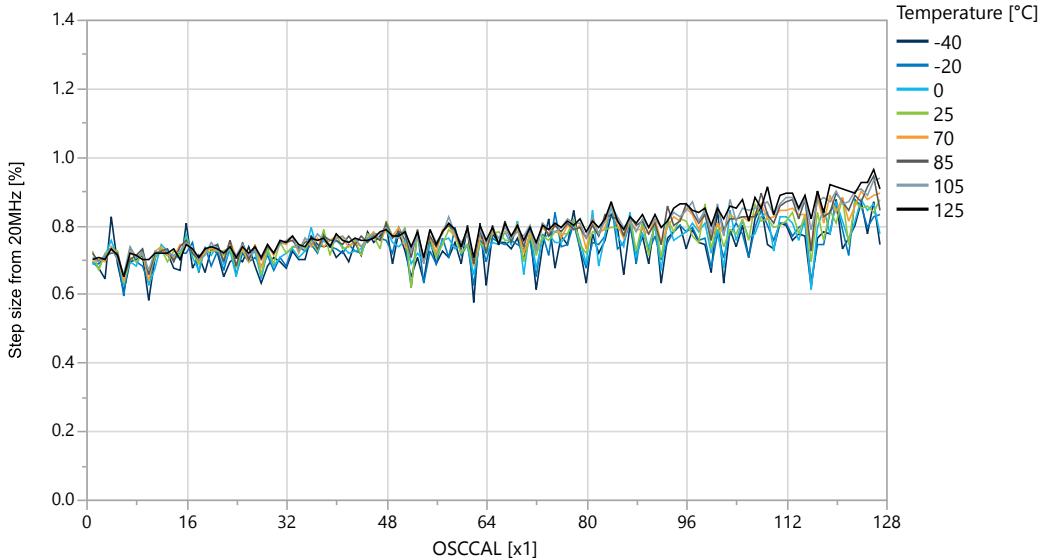
Figure 6-52. Absolute Accuracy vs.  $V_{DD}$  ( $f_{ADC}=115$  kspS,  $T=25^{\circ}C$ ), REFSEL = External Reference

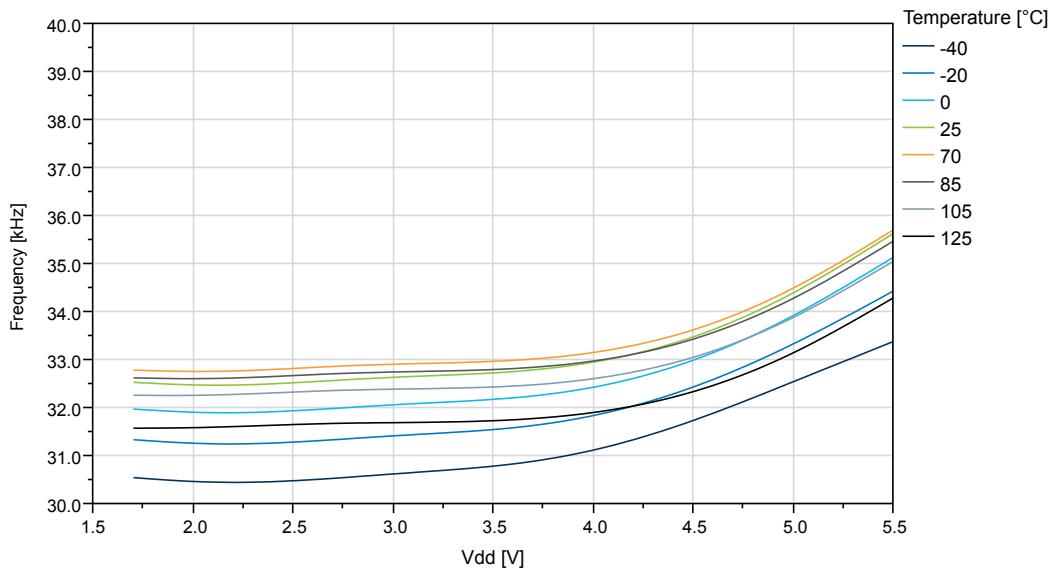


**Figure 6-55. DNL vs.  $V_{REF}$  ( $V_{DD}=5.0V$ ,  $f_{ADC}=115$  ksps, REFSEL = External Reference)****Figure 6-56. Gain vs.  $V_{DD}$  ( $f_{ADC}=115$  ksps,  $T=25^{\circ}\text{C}$ , REFSEL = External Reference)**

**Figure 6-65. Offset vs.  $V_{CM}$  - 10 mV to 50 mV ( $V_{DD}=5V$ ,  $T=25^{\circ}C$ )**

## 6.7 OSC20M Characteristics

**Figure 6-66. OSC20M Internal Oscillator: Calibration Stepsize vs. Calibration Value ( $V_{DD}=3V$ )**

**Figure 6-71. OSCULP32K Internal Oscillator Frequency vs. V<sub>DD</sub>**

## 7. Package Drawings

### 7.1 48 pin TQFP

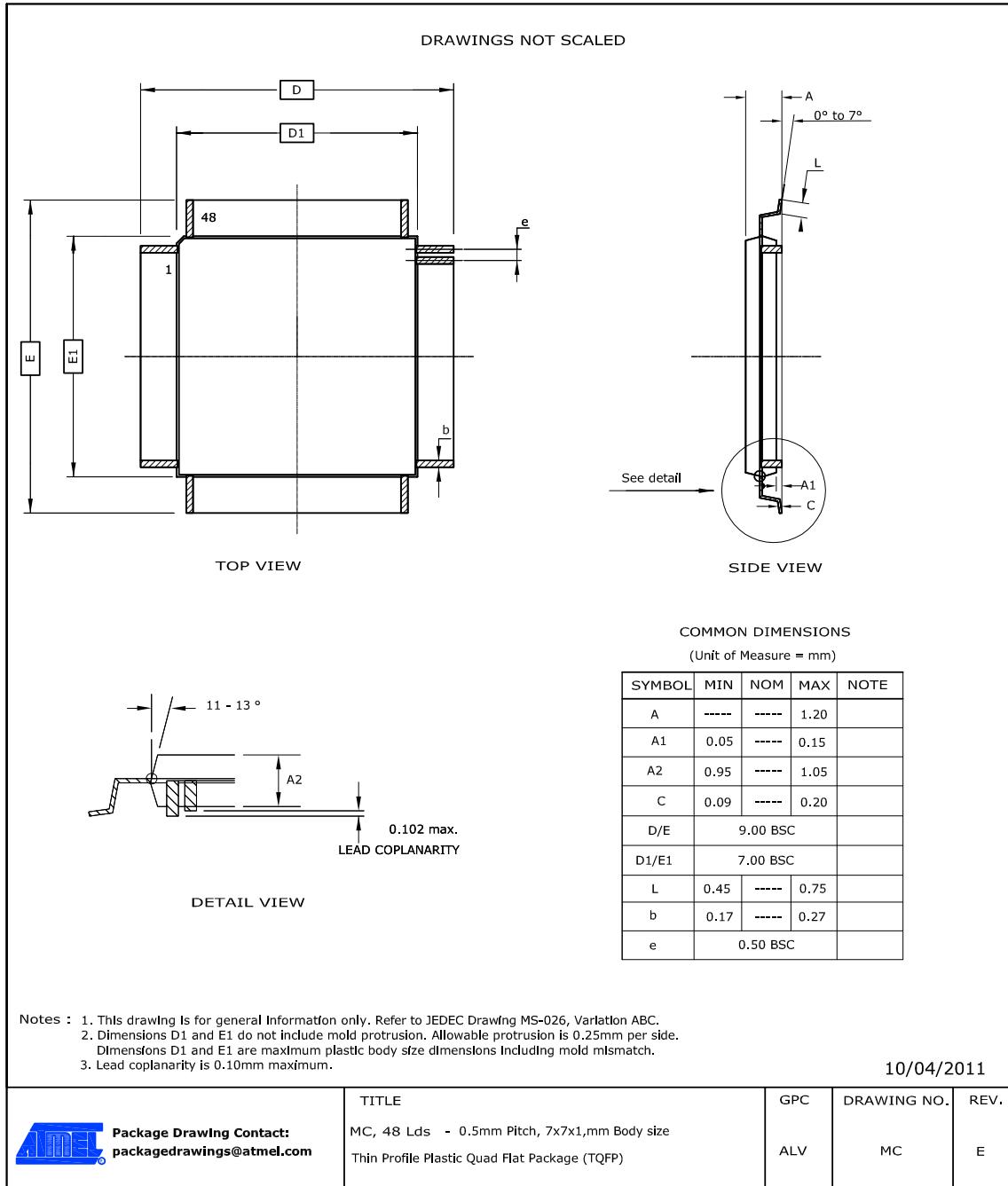


Table 7-1. Device and Package Maximum Weight

140	mg
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### 9. Data Sheet Revision History

**Note:** The data sheet revision is independent of the die revision and the device variant (last letter of the ordering number).

#### 9.1 Rev. A - 02/2018

Initial release.