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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	27
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 3x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4lc2aa-au

  - PLL up to 240MHz for device clock and for USB
  - Digital Frequency Locked Loop (DFLL) with wide input range
  - Up to 16 peripheral DMA (PDCA) channels
- Peripherals
  - USB 2.0 Device and Embedded Host: 12 Mbps, up to 8 bidirectional Endpoints and Multi-packet Ping-pong Mode. On-Chip Transceiver
  - Liquid Crystal Display (LCD) Module with Capacity up to 40 Segments and up to 4 Common Terminals
  - One USART with ISO7816, IrDA®, RS-485, SPI, Manchester and LIN Mode
  - Three USART with SPI Mode
  - One PicoUART for extended UART wake-up capabilities in all sleep modes
  - Windowed Watchdog Timer (WDT)
  - Asynchronous Timer (AST) with Real-time Clock Capability, Counter or Calendar Mode Supported
  - Frequency Meter (FREQM) for Accurate Measuring of Clock Frequency
  - Six 16-bit Timer/Counter (TC) Channels with capture, waveform, compare and PWM mode
  - One Master/Slave Serial Peripheral Interface (SPI) with Chip Select Signals
  - Four Master and Two Slave Two-wire Interfaces (TWI), up to 3.4Mbit/s I^2C-compatible
  - One Advanced Encryption System (AES) with 128-bit key length
  - One 16-channel ADC 300Ksps (ADC) with up to 12 Bits Resolution
  - One DAC 500Ksps (DACC) with up to 10 Bits Resolution
  - Four Analog Comparators (ACIFC) with Optional Window Detection
  - Capacitive Touch Module (CATB) supporting up to 32 buttons
  - Audio Bitstream DAC (ABDACB) Suitable for Stereo Audio
  - Inter-IC Sound (IISC) Controller, Compliant with Inter-IC Sound (I^2S) Specification
  - Peripheral Event System for Direct Peripheral to Peripheral Communication
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)
  - Random generator (TRNG)
  - Parallel Capture Module (PARC)
  - Glue Logic Controller (GLOC)
- I/O
  - Up to 75 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and slew-rate control
  - Up to Six High-drive I/O Pins
- Single 1.68-3.6V Power Supply
- Packages
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball VFBGA, 7x7 mm, pitch 0.65 mm
  - 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm
  - 64-ball WLCSP, 4,314x4,434 mm, pitch 0.5 mm for SAM4LC4/2 and SAM4LS4/2 series
  - 64-ball WLCSP, 5,270x5,194 mm, pitch 0.5 mm for SAM4LC8 and SAM4LS8 series
  - 48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm

3.1.2 ATSAM4LSx Pinout

Figure 3-6. ATSAM4LS TQFP100 Pinout

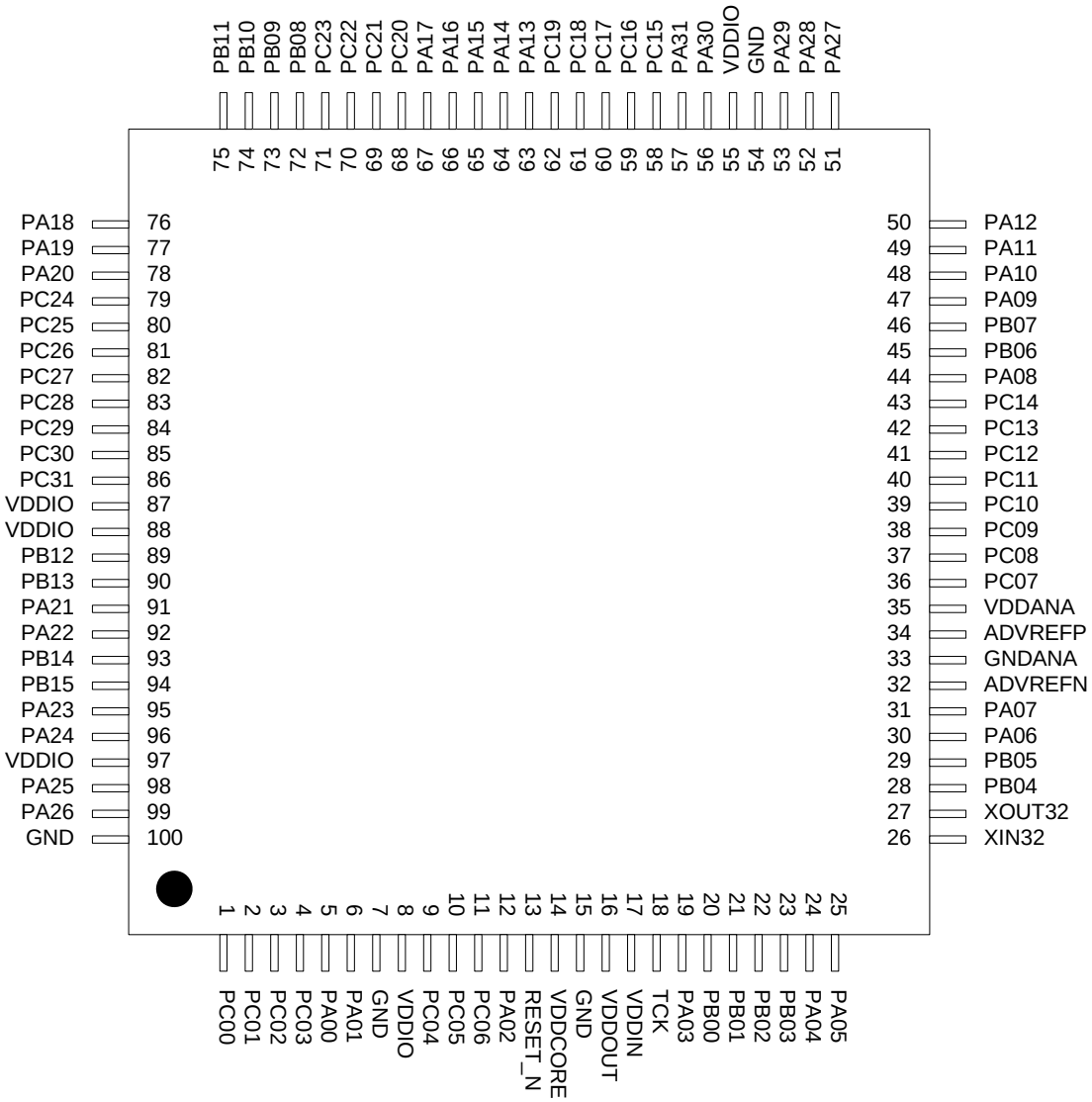


Table 3-8. Signal Descriptions List (Sheet 2 of 4)

Signal Name	Function	Type	Active Level	Comments
Inter-IC Sound (I2S) Controller - IISC				
IMCK	I2S Master Clock	Output		
ISCK	I2S Serial Clock	I/O		
ISDI	I2S Serial Data In	Input		
ISDO	I2S Serial Data Out	Output		
IWS	I2S Word Select	I/O		
LCD Controller - LCDCA				
BIASL	Bias voltage (1/3 VLCD)	Analog		
BIASH	Bias voltage (2/3 VLCD)	Analog		
CAPH	High voltage end of flying capacitor	Analog		
CAPL	Low voltage end of flying capacitor	Analog		
COM3 - COM0	Common terminals	Analog		
SEG39 - SEG0	Segment terminals	Analog		
VLCD	Bias voltage	Analog		
Parallel Capture - PARC				
PCCK	Clock	Input		
PCDATA7 - PCDATA0	Data lines	Input		
PCEN1	Data enable 1	Input		
PCEN2	Data enable 2	Input		
Peripheral Event Controller - PEVC				
PAD_EVT3 - PAD_EVT0	Event Inputs	Input		
Power Manager - PM				
RESET_N	Reset	Input	Low	
System Control Interface - SCIF				
GCLK3 - GCLK0	Generic Clock Outputs	Output		
GCLK_IN1 - GCLK_IN0	Generic Clock Inputs	Input		
XIN0	Crystal 0 Input	Analog/ Digital		
XOUT0	Crystal 0 Output	Analog		
Serial Peripheral Interface - SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS3 - NPCS0	SPI Peripheral Chip Selects	I/O	Low	
SCK	Clock	I/O		
Timer/Counter - TC0, TC1				

Table 4-2. Interrupt Request Signal Map (Sheet 2 of 3)

Line	Module	Signal
12	Peripheral DMA Controller	PDCA 11
13	Peripheral DMA Controller	PDCA 12
14	Peripheral DMA Controller	PDCA 13
15	Peripheral DMA Controller	PDCA 14
16	Peripheral DMA Controller	PDCA 15
17	CRC Calculation Unit	CRCCU
18	USB 2.0 Interface	USBC
19	Peripheral Event Controller	PEVC TR
20	Peripheral Event Controller	PEVC OV
21	Advanced Encryption Standard	AESA
22	Power Manager	PM
23	System Control Interface	SCIF
24	Frequency Meter	FREQM
25	General-Purpose Input/Output Controller	GPIO 0
26	General-Purpose Input/Output Controller	GPIO 1
27	General-Purpose Input/Output Controller	GPIO 2
28	General-Purpose Input/Output Controller	GPIO 3
29	General-Purpose Input/Output Controller	GPIO 4
30	General-Purpose Input/Output Controller	GPIO 5
31	General-Purpose Input/Output Controller	GPIO 6
32	General-Purpose Input/Output Controller	GPIO 7
33	General-Purpose Input/Output Controller	GPIO 8
34	General-Purpose Input/Output Controller	GPIO 9
35	General-Purpose Input/Output Controller	GPIO 10
36	General-Purpose Input/Output Controller	GPIO 11
37	Backup Power Manager	BPM
38	Backup System Control Interface	BSCIF
39	Asynchronous Timer	AST ALARM
40	Asynchronous Timer	AST PER
41	Asynchronous Timer	AST OVF
42	Asynchronous Timer	AST READY
43	Asynchronous Timer	AST CLKREADY
44	Watchdog Timer	WDT
45	External Interrupt Controller	EIC 1
46	External Interrupt Controller	EIC 2
47	External Interrupt Controller	EIC 3

At power-up or after a reset, the ATSAM4L8/L4/L2 is in the RUN0 mode. Only the necessary clocks are enabled allowing software execution. The Power Manager (PM) can be used to adjust the clock frequencies and to enable and disable the peripheral clocks.

When the CPU is entering a Power Save Mode, the CPU stops executing code. The user can choose between four Power Save Modes to optimize power consumption:

- SLEEP mode: the Cortex-M4 core is stopped, optionally some clocks are stopped, peripherals are kept running if enabled by the user.
- WAIT mode: all clock sources are stopped, the core and all the peripherals are stopped except the modules running with the 32kHz clock if enabled. This is the lowest power configuration where SleepWalking is supported.
- RETENTION mode: similar to the WAIT mode in terms of clock activity. This is the lowest power configuration where the logic is retained.
- BACKUP mode: the Core domain is powered off, the Backup domain is kept powered.

A wake up source exits the system to the RUN mode from which the Power Save Mode was entered.

A reset source always exits the system from the Power Save Mode to the RUN0 mode.

The configuration of the I/O lines are maintained in all Power Save Modes. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677.

7.1.1 SLEEP mode

The SLEEP mode allows power optimization with the fastest wake up time.

The CPU is stopped. To further reduce power consumption, the user can switch off modules-clocks and synchronous clock sources through the BPM.PMCON.SLEEP field (See Table 7-1). The required modules will be halted regardless of the bit settings of the mask registers in the Power Manager (PM.AHBMASK, PM.APBxMASK).

Table 7-1. SLEEP mode Configuration

BPM.PSAVE.SLEEP	CPU clock	AHB clocks	APB clocks GCLK	Clock sources: OSC, RCFAST, RC80M, PLL, DFLL	RCSYS	OSC32K RC32K(2)	Wake up Sources
0	Stop	Run	Run	Run	Run	Run	Any interrupt
1	Stop	Stop	Run	Run	Run	Run	Any interrupt(1)
2	Stop	Stop	Stop	Run	Run	Run	Any interrupt(1)
3	Stop	Stop	Stop	Stop	Run	Run	Any interrupt(1)

Notes: 1. from modules with clock running.
2. OSC32K and RC32K will only remain operational if pre-enabled.

7.1.1.1 Entering SLEEP mode

The SLEEP mode is entered by executing the WFI instruction.

Additionally, if the SLEEPONEXIT bit in the Cortex-M4 System Control Register (SCR) is set, the SLEEP mode will also be entered when the Cortex-M4 exits the lowest priority ISR. This

- Set the clock frequency to be supported in both power configurations.
- Set the high speed read mode of the FLASH to be supported in both power scaling configurations
  - Only relevant when entering or exiting BPM.PMCON.PS=2
- Configure the BPM.PMCON.PS field to the new power configuration.
- Set the BPM.PMCON.PSCREQ bit to one.
- Disable all the interrupts except the PM WCAUSE interrupt and enable only the PSOK asynchronous event in the AWEN register of PM.
- Execute the WFI instruction.
- WAIT for PM interrupt.

The new power configuration is reached when the system is waken up by the PM interrupt thanks to the PSOK event.

By default, all features are available in all Power Scaling modes. However some specific features are not available in PS1 (BPM.PMCON.PS=1) mode :

- USB
- DFLL
- PLL
- Programming/Erasing in Flash

8.5 Product dependencies

8.5.1 I/O Lines

Refer to Section 1.1.5.1 ”I/O Lines” on page 5.

8.5.2 Power management

Refer to Section 1.1.5.2 ”Power Management” on page 5.

8.5.3 Clocks

Refer to Section 1.1.5.3 ”Clocks” on page 5.

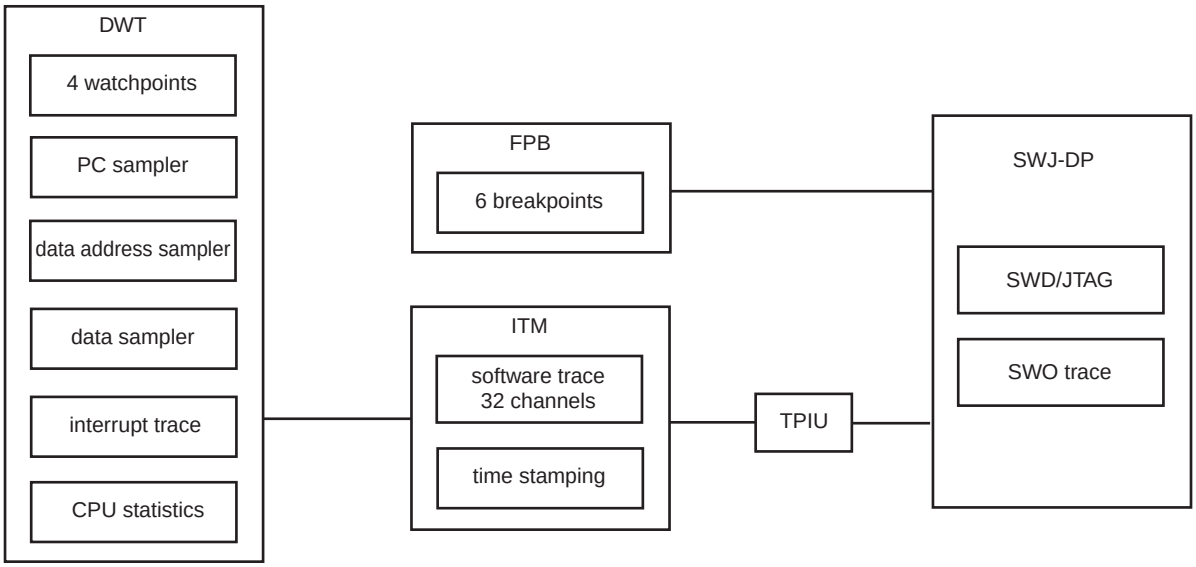
8.6 Core debug

Figure 8-2 shows the Debug Architecture used in the SAM4L. The Cortex-M4 embeds four functional units for debug:

- FPB (Flash Patch Breakpoint)
- DWT (Data Watchpoint and Trace)
- ITM (Instrumentation Trace Macrocell)
- TPIU (Trace Port Interface Unit)

The debug architecture information that follows is mainly dedicated to developers of SWJ-DP Emulators/Probes and debugging tool vendors for Cortex-M4 based microcontrollers. For further details on SWJ-DP see the Cortex-M4 technical reference manual.

Figure 8-2. Debug Architecture



8.6.1 FPB (Flash Patch Breakpoint)

The FPB:

- Implements hardware breakpoints
- Patches (on the fly) code and data being fetched by the Cortex-M4 core from code space with data in the system space. Definition of code and system spaces can be found in the System Address Map section of the ARMv7-M Architecture Reference Manual.

8.7.5 Product Dependencies

8.7.5.1 I/O Lines

The TCK pin is dedicated to the EDP. The other debug port pins default after reset to their GPIO functionality and are automatically reassigned to the JTAG functionalities on detection of a debugger. In serial wire mode, TDI and TDO can be used as GPIO functions. Note that in serial wire mode TDO can be used as a single pin trace output.

8.7.5.2 Power Management

When a debugger is present, the connection is kept alive allowing debug operations. As a side effect, the power is never turned off. The hot plugging functionality is always available except when the system is in BACKUP Power Save Mode.

8.7.5.3 Clocks

The SWJ-DP uses the external TCK pin as its clock source. This clock must be provided by the external JTAG master device.

Some of the JTAG Instructions are used to access an Access Port (SMAP or AHB-AP). These instructions require the CPU clock to be running.

If the CPU clock is not present because the CPU is in a Power Save Mode where this clock is not provided, the Power Manager(PM) will automatically restore the CPU clock on detection of a debug access.

The RCSYS clock is used as CPU clock when the external reset is applied to ensure correct Access Port operations.

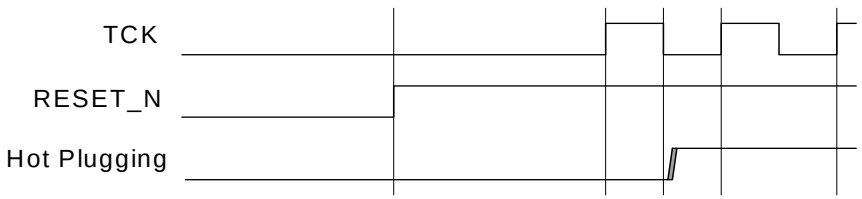
8.7.6 Module Initialization

This module is enabled as soon as a TCK falling edge is detected when RESET_N is not asserted (refer to Section 8.7.7 below). Moreover, the module is synchronously reseted as long as the TAP machine is in the TEST_LOGIC_RESET (TLR) state. It is advised asserting TMS at least 5 TCK clock periods after the debugger has been detected to ensure the module is in the TLR state prior to any operation. This module also has the ability to maintain the Cortex-M4 under reset (refer to the Section 8.7.8 ”SMAP Core Reset Request Source” on page 70).

8.7.7 Debugger Hot Plugging

The TCK pin is dedicated to the EDP. After reset has been released, the EDP detects that a debugger has been attached when a TCK falling edge arises.

Figure 8-4. Debugger Hot Plugging Detection Timings Diagram



8.7.10 SW-DP and JTAG-DP Selection Mechanism

After reset, the SWJ-DP is in JTAG mode but it can be switched to the Serial Wire mode. Debug port selection mechanism is done by sending specific **SWDIOTMS** sequence. The JTAG-DP is selected by default after reset.

- Switch from JTAG-DP to SW-DP. The sequence is:
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
  - Send the 16-bit sequence on **SWDIOTMS** = 0111100111100111 (0x79E7 MSB first)
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
- Switch from SWD to JTAG. The sequence is:
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
  - Send the 16-bit sequence on **SWDIOTMS** = 0011110011100111 (0x3CE7 MSB first)

Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1

Note that the BSCAN-TAP is not available when the debug port is switched to Serial Mode. Boundary scan instructions are not available.

8.7.11 JTAG-DP and BSCAN-TAP Selection Mechanism

After the DP has been enabled, the BSCAN-TAP and the JTAG-DP run simultaneously has long as the SWJ-DP remains in JTAG mode. Each TAP captures simultaneously the JTAG instructions that are shifted. If an instruction is recognized by the BSCAN-TAP, then the BSCAN-TAP TDO is selected instead of the SWJ-DP TDO. TDO selection changes dynamically depending on the current instruction held in the BSCAN-TAP instruction register.

8.9 System Manager Access Port (SMAP)

Rev.: 1.0.0.0

8.9.1 Features

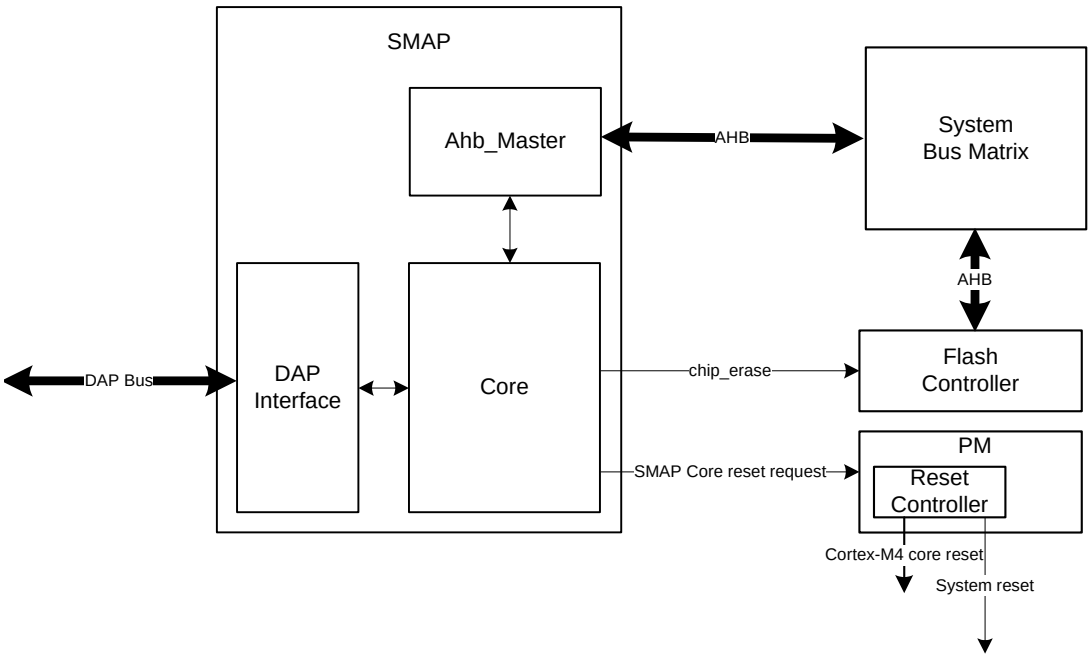
- **Chip Erase command and status**
- **Cortex-M4 core reset source**
- **32-bit Cyclic Redundancy check of any memory accessible through the bus matrix**
- **Unlimited Flash User page read access**
- **Chip identification register**

8.9.2 Overview

The SMAP provides memory-related services and also Cortex-M4 core reset control to a debugger through the Debug Port. This makes possible to halt the CPU and program the device after reset.

8.9.3 Block Diagram

Figure 8-7. SMAP Block Diagram



8.9.4 Initializing the Module

The SMAP can be accessed only if the CPU clock is running and the SWJ-DP has been activated by issuing a CDBGPWRUP request. For more details, refer to the ARM Debug Interface v5.1 Architecture Specification.

Then it must be enabled by writing a one to the EN bit of the CR register (CR.EN) before writing or reading other registers. If the SMAP is not enabled it will discard any read or write operation.

8.9.5 Stopping the Module

To stop the module, the user must write a one to the DIS bit of the CR register (CR.DIS). All the user interface and internal registers will be cleared and the internal clock will be stopped.

8.9.6 Security Considerations

In protected state this module may access sensible information located in the device memories. To avoid any risk of sensible data extraction from the module registers, all operations are non interruptible except by a disable command triggered by writing a one to CR.DIS. Issuing this command clears all the interface and internal registers.

Some registers have some special protection:

- It is not possible to read or write the LENGTH register when the part is protected.
- In addition, when the part is protected and an operation is ongoing, it is not possible to read the ADDR and DATA registers. Once an operation has started, the user has to wait until it has terminated by polling the DONE field in the Status Register (SR.DONE).

8.9.7 Chip Erase

The Chip erase operation consists in:

1. clearing all the volatile memories in the system
2. clearing the whole flash array
3. clearing the protected state

No proprietary or sensitive information is left in volatile memories once the protected state is disabled.

This feature is operated by writing a one to the CE bit of the Control Register (CR.CE). When the operation completes, SR.DONE is asserted.

8.9.8 Cortex-M4 Core Reset Source

The SMAP processes the EDP Core hold reset requests (Refer to Section 1.1.8 ”SMAP Core Reset Request Source” on page 6). When requested, it instructs the Power Manager to hold the Cortex-M4 core under reset.

The SMAP can de-assert the core reset request if a one is written to the Hold Core Reset bit in the Status Clear Register (SCR.HCR). This has the effect of releasing the CPU from its reset state. To assert again this signal, a new reset sequence with TCK tied low must be issued.

Note that clearing HCR with this module is only possible when it is enabled, for more information refer to Section 8.9.4 ”Initializing the Module” on page 78. Also note that asserting RESET_N automatically clears HCR.

8.9.11.2 Status Register

Name: SR

Access Type: Read-Only

Offset: 0x04

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	STATE		

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	DBGP	PROT	EN

7	6	5	4	3	2	1	0
-	-	-	LCK	FAIL	BERR	HCR	DONE

- **STATE: State**

Value	State	Description
0	IDLE	Idle state
1	CE	Chip erase operation is ongoing
2	CRC32	CRC32 operation is ongoing
3	FSPR	Flash User Page Read
4-7	-	reserved

- **DBGP: Debugger present**
  1: A debugger is present (TCK falling edge detected)
  0: No debugger is present
- **PROT: Protected**
  1: The protected state is set. The only way to overcome this is to issue a Chip Erase command.
  0: The protected state is not set
- **EN: Enabled**
  1: The block is in ready for operation
  0: the block is disabled. Write operations are not possible until the block is enabled by writing a one in CR.EN.
- **LCK: Lock**
  1: An operation could not be performed because chip protected state is on.
  0: No security issues have been detected sincle last clear of this bit
- **FAIL: Failure**
  1: The requested operation failed
  0: No failure has been detected sincle last clear of this bit
- **BERR: Bus Error**
  1: A bus error occured due to the unability to access part of the requested memory area.

8.9.11.6 Data Register

Name: DATA

Access Type: Read/Write

Offset: 0x14

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DATA							

23	22	21	20	19	18	17	16
DATA							

15	14	13	12	11	10	9	8
DATA							

7	6	5	4	3	2	1	0
DATA							

- **DATA: Generic data register**

8.9.11.9 *Chip Identification Extension Register*

Name: EXID

Access Type: Read-Only

Offset: 0xF4

Reset Value: -

31	30	29	28	27	26	25	24
EXID							

23	22	21	20	19	18	17	16
EXID							

15	14	13	12	11	10	9	8
EXID							

7	6	5	4	3	2	1	0
EXID							

Note: Refer to section CHIPID for more information on this register.

instruction for the first time. SAMPLE/PRELOAD can also be used for taking a snapshot of the external pins during normal operation of the part.

When using the JTAG interface for Boundary-Scan, the JTAG TCK clock is independent of the internal chip clock, which is not required to run.

NOTE: For pins connected to 5V lines care should be taken to not drive the pins to a logic one using boundary scan, as this will create a current flowing from the 3,3V driver to the 5V pullup on the line. Optionally a series resistor can be added between the line and the pin to reduce the current.

8.11.7 Flash Programming typical procedure

Flash programming is performed by operating Flash controller commands. The Flash controller is connected to the system bus matrix and is then controllable from the AHP-AP. The AHB-AP cannot write the FLASH page buffer while the core_hold_reset is asserted. The AHB-AP cannot be accessed when the device is in protected state. It is important to ensure that the CPU is halted prior to operating any flash programming operation to prevent it from corrupting the system configuration. The recommended sequence is shown below:

1. At power up, RESET_N is driven low by a debugger. The on-chip regulator holds the system in a POR state until the input supply is above the POR threshold. The system continues to be held in this static state until the internally regulated supplies have reached a safe operating.
2. PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock, and any Bus Clocks that do not have clock gate control). Internal resets are maintained due to the external reset.
   – The Debug Port (DP) and Access Ports (AP) receives a clock and leave the reset state,
3. The debugger maintains a low level on TCK and release RESET_N.
   – The SMAP asserts the core_hold_reset signal
4. The Cortex-M4 core remains in reset state, meanwhile the rest of the system is released.
5. The debugger then configures the NVIC to catch the Cortex-M4 core reset vector fetch. For more information on how to program the NVIC, refer to the ARMv7-M Architecture Reference Manual.
6. The debugger writes a one in the SMAP SCR.HCR to release the Cortex-M4 core reset to make the system bus matrix accessible from the AHB-AP.
7. The Cortex-M4 core initializes the SP, then read the exception vector and stalls
8. Programming is available through the AHB-AP
9. After operation is completed, the chip can be restarted either by asserting RESET_N or switching power off/on or clearing SCR.HCR. Make sure that the TCK pin is high when releasing RESET_N not to halt the core.

Table 9-9. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 1

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	222	240	µA/MHz
		85°C		233	276	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	233	276	
		85°C		230	270	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	100	112	
		85°C		100	119	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	104	128	
		85°C		107	138	
SLEEP0	Switching mode	25°C	9 * Main clock cycles	527	627	µA
		85°C		579	739	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	369	445	
		85°C		404	564	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	305	381	
		85°C		334	442	
SLEEP3	Linear mode	25°C		46	55	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	5.5		
	OSC32K and AST stopped Fast wake-up enable			4.3		
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.4		
	AST and OSC32K stopped			2.3		
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-10. Typical Power Consumption running CoreMark on CPU clock sources (1)

Clock Source	Conditions	Regulator	Frequency (MHz)	Typ	Unit

9.6.5 High Drive TWI Pin : PB00, PB01

Table 9-19. High Drive TWI Pin Characteristics in TWI configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)	PB00, PB01			40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.3 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.7 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	DRIVEL=0				0.5	mA
		DRIVEL=1				1.0	
		DRIVEL=2				1.6	
		DRIVEL=3				3.1	
		DRIVEL=4				6.2	
		DRIVEL=5				9.3	
		DRIVEL=6				15.5	
		DRIVEL=7				21.8	
I_{CS}	Current Source(2)	DRIVEH=0			0.5		mA
		DRIVEH=1			1		
		DRIVEH=2			1.5		
		DRIVEH=3			3		
f_{MAX}	Max frequency(2)	HsMode with Current source; DRIVEx=3, SLEW=0 Cbus = 400pF, V_{VDD} = 1.68V		3.5	6.4		MHz
t_{RISE}	Rise time(2)	HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			28	38	ns
t_{FALL}	Fall time(2)	Standard Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	ns
		HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Figure 9-10. USART in SPI Slave Mode with (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

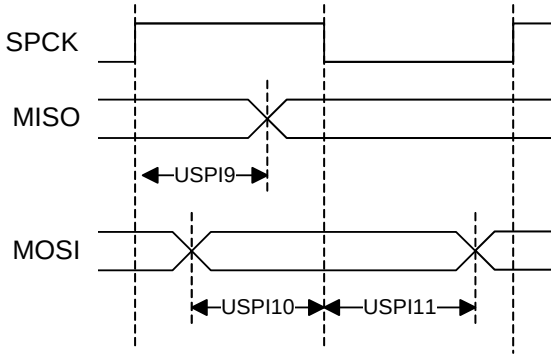


Figure 9-11. USART in SPI Slave Mode, NPCS Timing

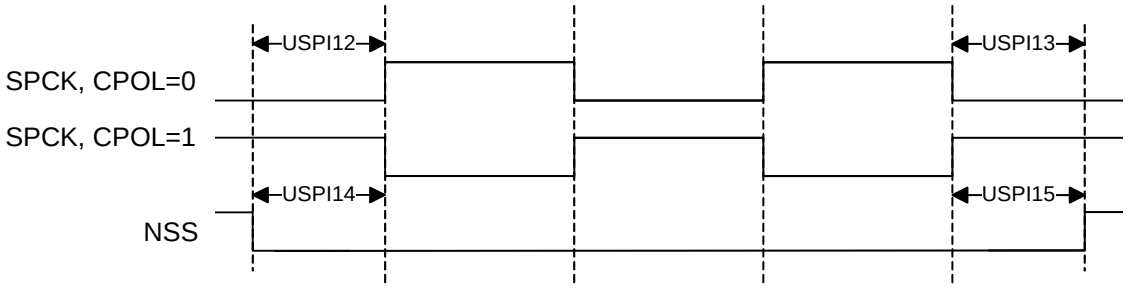


Table 9-58. USART0 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		740.67	ns
USPI7	MOSI setup time before SPCK rises		56.73 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		45.18 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			670.18	
USPI10	MOSI setup time before SPCK falls		56.73 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		45.18 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		688.71		
USPI13	NSS hold time after SPCK falls		-2.25		
USPI14	NSS setup time before SPCK falls		688.71		
USPI15	NSS hold time after SPCK rises		-2.25		

Table 9-66. SWD Timings[1]

Symbol	Parameter	Conditions	Min	Max	Units
Thigh	SWDCLK High period	V_{VDDIO} from 3.0 V to 3.6 V, maximum external capacitor = 40 pF	10	500 000	ns
Tlow	SWDCLK Low period		10	500 000	
Tos	SWDIO output skew to falling edge SWDCLK		-5	5	
Tis	Input Setup time required between SWDIO		4	-	
Tih	Input Hold time required between SWDIO and rising edge SWDCLK		1	-	

Note: 1. These values are based on simulation. These values are not covered by test limits in production or characterization.

10.3 Soldering Profile

Table 10-35 gives the recommended soldering profile from J-STD-20.

Table 10-35. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150 s
Time within 5·C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25·C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.