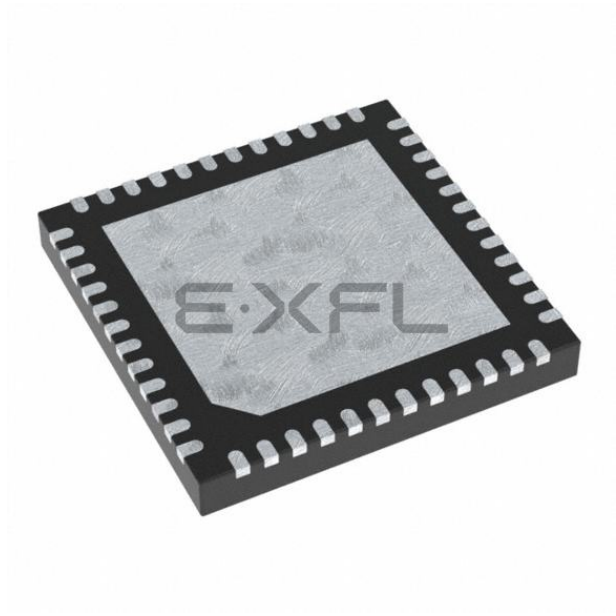

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	27
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 3x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4lc2aa-mu

events, even in sleep modes where the module clock is stopped. Power monitoring is supported by on-chip Power-on Reset (POR18, POR33), Brown-out Detectors (BOD18, BOD33). The device features several oscillators, such as Phase Locked Loop (PLL), Digital Frequency Locked Loop (DFLL), Oscillator 0 (OSC0), Internal RC 4,8,12MHz oscillator (RCFAST), system RC oscillator (RCSYS), Internal RC 80MHz, Internal 32kHz RC and 32kHz Crystal Oscillator. Either of these oscillators can be used as source for the system clock. The DFLL is a programmable internal oscillator from 40 to 150MHz. It can be tuned to a high accuracy if an accurate reference clock is running, e.g. the 32kHz crystal oscillator.

The Watchdog Timer (WDT) will reset the device unless it is periodically serviced by the software. This allows the device to recover from a condition that has caused the system to be unstable.

The Asynchronous Timer (AST) combined with the 32kHz crystal oscillator supports powerful real-time clock capabilities, with a maximum timeout of up to 136 years. The AST can operate in counter or calendar mode.

The Frequency Meter (FREQM) allows accurate measuring of a clock frequency by comparing it to a known reference clock.

The Full-speed USB 2.0 device and embedded host interface (USBC) supports several USB classes at the same time utilizing the rich end-point configuration.

The device includes six identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing, and pulse width modulation.

The ATSAM4L8/L4/L2 also features many communication interfaces, like USART, SPI, or TWI, for communication intensive applications. The USART supports different communication modes, like SPI Mode and LIN Mode.

A general purpose 16-channel ADC is provided, as well as four analog comparators (ACIFC). The ADC can operate in 12-bit mode at full speed. The analog comparators can be paired to detect when the sensing voltage is within or outside the defined reference window.

Atmel offers the QTouch Library for embedding capacitive touch buttons, sliders, and wheels functionality. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys as well as Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop, and debug your own touch applications.

The Audio Bitstream DAC (ABDACB) converts a 16-bit sample value to a digital bitstream with an average value proportional to the sample value. Two channels are supported, making the ABDAC particularly suitable for stereo audio.

The Inter-IC Sound Controller (IISC) provides a 5-bit wide, bidirectional, synchronous, digital audio link with external audio devices. The controller is compliant with the Inter-IC Sound (I2S) bus specification.

Figure 3-9. ATSAM4LS TQFP64/QFN64 Pinout

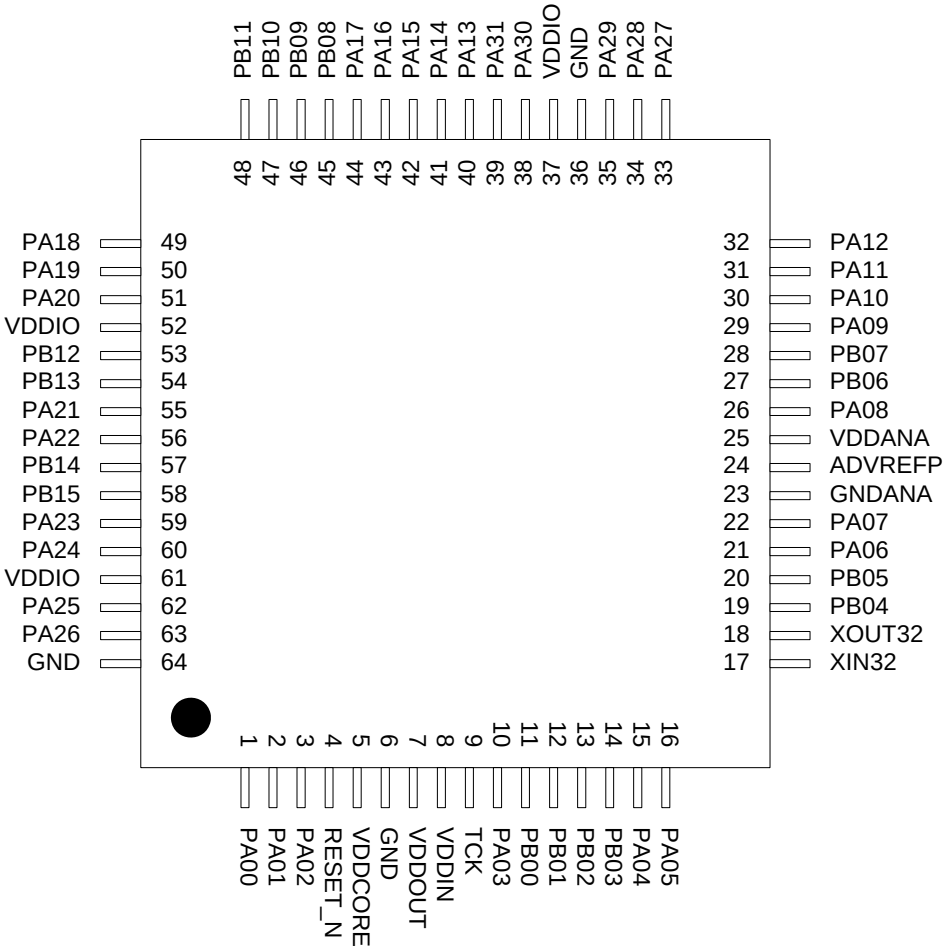


Table 3-3. 64-pin GPIO Controller Function Multiplexing for WLCSP package (Sheet 1 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
WLCSP	WLCSP				A	B	C	D	E	F	G
G4	G4	PA00	0	VDDIO							
G5	G5	PA01	1	VDDIO							
F3	F3	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
E2	E2	PA03	3	VDDIN		SPI MISO					
D3	D3	PA04	4	VDDANA	ADCIFE AD0	USART0 CLK	EIC EXTINT2	GLOC IN1			CATB SENSE0
C3	C3	PA05	5	VDDANA	ADCIFE AD1	USART0 RXD	EIC EXTINT3	GLOC IN2	ADCIFE TRIGGER		CATB SENSE1
C4	C4	PA06	6	VDDANA	DACC VOUT	USART0 RTS	EIC EXTINT1	GLOC IN0	ACIFC ACAN0		CATB SENSE2
C5	C5	PA07	7	VDDANA	ADCIFE AD2	USART0 TXD	EIC EXTINT4	GLOC IN3	ACIFC ACAP0		CATB SENSE3
B4	B4	PA08	8	LCDA	USART0 RTS	TC0 A0	PEVC PAD EVT0	GLOC OUT0		LCDCA SEG23	CATB SENSE4
A5	A5	PA09	9	LCDA	USART0 CTS	TC0 B0	PEVC PAD EVT1	PARC PCDATA0		LCDCA COM3	CATB SENSE5
B6	B6	PA10	10	LCDA	USART0 CLK	TC0 A1	PEVC PAD EVT2	PARC PCDATA1		LCDCA COM2	CATB SENSE6
B7	B7	PA11	11	LCDA	USART0 RXD	TC0 B1	PEVC PAD EVT3	PARC PCDATA2		LCDCA COM1	CATB SENSE7
A8	A8	PA12	12	LCDA	USART0 TXD	TC0 A2		PARC PCDATA3		LCDCA COM0	CATB DIS
C7	C7	PA13	13	LCDA	USART1 RTS	TC0 B2	SPI NPCS1	PARC PCDATA4		LCDCA SEG5	CATB SENSE8
D7	D7	PA14	14	LCDA	USART1 CLK	TC0 CLK0	SPI NPCS2	PARC PCDATA5		LCDCA SEG6	CATB SENSE9
E7	E7	PA15	15	LCDA	USART1 RXD	TC0 CLK1	SPI NPCS3	PARC PCDATA6		LCDCA SEG7	CATB SENSE10
F7	F7	PA16	16	LCDA	USART1 TXD	TC0 CLK2	EIC EXTINT1	PARC PCDATA7		LCDCA SEG8	CATB SENSE11
G8	G8	PA17	17	LCDA	USART2 RTS	ABDACB DAC0	EIC EXTINT2	PARC PCCK		LCDCA SEG9	CATB SENSE12
G7	G7	PA18	18	LCDA	USART2 CLK	ABDACB DACN0	EIC EXTINT3	PARC PCEN1		LCDCA SEG18	CATB SENSE13
G6	G6	PA19	19	LCDA	USART2 RXD	ABDACB DAC1	EIC EXTINT4	PARC PCEN2	SCIF GCLK0	LCDCA SEG19	CATB SENSE14
H7	H7	PA20	20	LCDA	USART2 TXD	ABDACB DACN1	EIC EXTINT5	GLOC IN0	SCIF GCLK1	LCDCA SEG20	CATB SENSE15
H5	H5	PA21	21	LCDC	SPI MISO	USART1 CTS	EIC EXTINT6	GLOC IN1	TWIM2 TWD	LCDCA SEG34	CATB SENSE16
F5	F5	PA22	22	LCDC	SPI MOSI	USART2 CTS	EIC EXTINT7	GLOC IN2	TWIM2 TWCK	LCDCA SEG35	CATB SENSE17

Table 3-3. 64-pin GPIO Controller Function Multiplexing for WLCSP package (Sheet 2 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
WLCSP	WLCSP				A	B	C	D	E	F	G
H3	H3	PA23	23	LCDC	SPI SCK	TWIMS0 TWD	EIC EXTINT8	GLOC IN3	SCIF GCLK IN0	LCDCA SEG38	CATB DIS
G3	G3	PA24	24	LCDC	SPI NPCS0	TWIMS0 TWCK		GLOC OUT0	SCIF GCLK IN1	LCDCA SEG39	CATB SENSE18
H2	H2	PA25	25	VDDIO	USBC DM	USART2 RXD					CATB SENSE19
G2	G2	PA26	26	VDDIO	USBC DP	USART2 TXD					CATB SENSE20
	A7	PA27	27	LCDA	SPI MISO	IISC ISCK	ABDACB DAC0	GLOC IN4	USART3 RTS		CATB SENSE0
	A6	PA28	28	LCDA	SPI MOSI	IISC ISDI	ABDACB DACN0	GLOC IN5	USART3 CTS		CATB SENSE1
	B8	PA29	29	LCDA	SPI SCK	IISC IWS	ABDACB DAC1	GLOC IN6	USART3 CLK		CATB SENSE2
	E8	PA30	30	LCDA	SPI NPCS0	IISC ISDO	ABDACB DACN1	GLOC IN7	USART3 RXD		CATB SENSE3
	F8	PA31	31	LCDA	SPI NPCS1	IISC IMCK	ABDACB CLK	GLOC OUT1	USART3 TXD		CATB DIS
D2	D2	PB00	32	VDDIN	TWIMS1 TWD	USART0 RXD					CATB SENSE21
C2	C2	PB01	33	VDDIN	TWIMS1 TWCK	USART0 TXD	EIC EXTINT0				CATB SENSE22
E3	E3	PB02	34	VDDANA	ADCIFE AD3	USART1 RTS	ABDACB DAC0	IISC ISCK	ACIFC ACBN0		CATB SENSE23
B1	B1	PB03	35	VDDANA	ADCIFE AD4	USART1 CLK	ABDACB DACN0	IISC ISDI	ACIFC ACBP0		CATB DIS
A1	A1	PB04	36	VDDANA	ADCIFE AD5	USART1 RXD	ABDACB DAC1	IISC ISDO	DACC EXT TRIG0		CATB SENSE24
D4	D4	PB05	37	VDDANA	ADCIFE AD6	USART1 TXD	ABDACB DACN1	IISC IMCK			CATB SENSE25
B5	B5	PB06	38	LCDA	USART3 RTS		GLOC IN4	IISC IWS		LCDCA SEG22	CATB SENSE26
C6	C6	PB07	39	LCDA	USART3 CTS		GLOC IN5	TC0 A0		LCDCA SEG21	CATB SENSE27
D6	D6	PB08	40	LCDA	USART3 CLK		GLOC IN6	TC0 B0		LCDCA SEG14	CATB SENSE28
E6	E6	PB09	41	LCDA	USART3 RXD	PEVC PAD EVT2	GLOC IN7	TC0 A1		LCDCA SEG15	CATB SENSE29
F6	F6	PB10	42	LCDA	USART3 TXD	PEVC PAD EVT3	GLOC OUT1	TC0 B1	SCIF GCLK0	LCDCA SEG16	CATB SENSE30
H8	H8	PB11	43	LCDA	USART0 CTS	SPI NPCS2		TC0 A2	SCIF GCLK1	LCDCA SEG17	CATB SENSE31
D5	D5	PB12	44	LCDC	USART0 RTS	SPI NPCS3	PEVC PAD EVT0	TC0 B2	SCIF GCLK2	LCDCA SEG32	CATB DIS

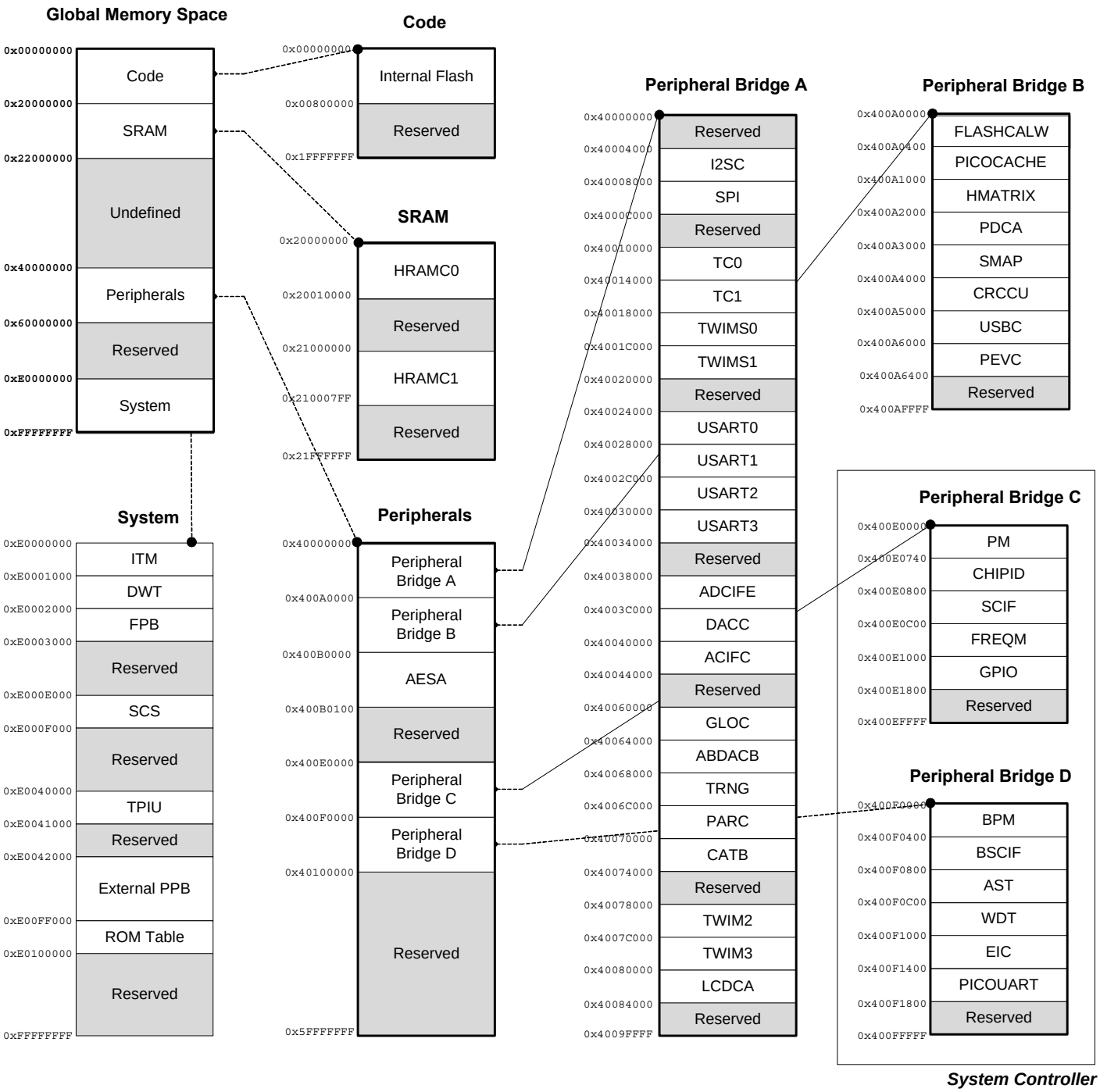
Table 4-2. Interrupt Request Signal Map (Sheet 3 of 3)

Line	Module	Signal
48	External Interrupt Controller	EIC 4
49	External Interrupt Controller	EIC 5
50	External Interrupt Controller	EIC 6
51	External Interrupt Controller	EIC 7
52	External Interrupt Controller	EIC 8
53	Inter-IC Sound (I2S) Controller	IISC
54	Serial Peripheral Interface	SPI
55	Timer/Counter	TC00
56	Timer/Counter	TC01
57	Timer/Counter	TC02
58	Timer/Counter	TC10
59	Timer/Counter	TC11
60	Timer/Counter	TC12
61	Two-wire Master Interface	TWIM0
62	Two-wire Slave Interface	TWIS0
63	Two-wire Master Interface	TWIM1
64	Two-wire Slave Interface	TWIS1
65	Universal Synchronous Asynchronous Receiver Transmitter	USART0
66	Universal Synchronous Asynchronous Receiver Transmitter	USART1
67	Universal Synchronous Asynchronous Receiver Transmitter	USART2
68	Universal Synchronous Asynchronous Receiver Transmitter	USART3
69	ADC controller interface	ADCIFE
70	DAC Controller	DACC
71	Analog Comparator Interface	ACIFC
72	Audio Bitstream DAC	ABDACB
73	True Random Number Generator	TRNG
74	Parallel Capture	PARC
75	Capacitive Touch Module B	CATB
77	Two-wire Master Interface	TWIM2
78	Two-wire Master Interface	TWIM3
79	LCD Controller A	LCDCA

5. Memories

5.1 Product Mapping

Figure 5-1. ATSAM4L8/L4/L2 Product Mapping



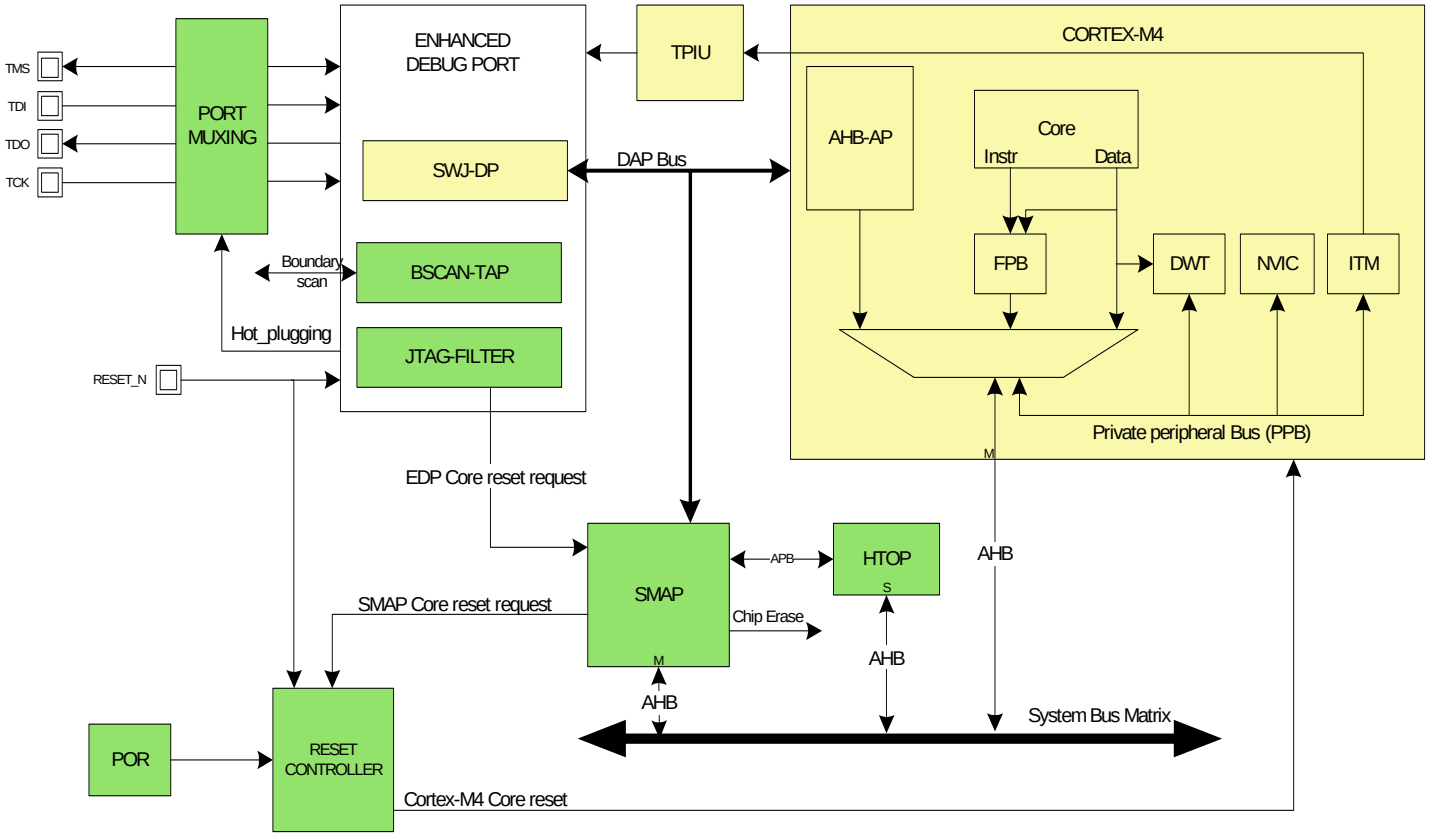
Memory	Start Address	Size
		ATSAM4Lx8
AESA	0x400B0000	256 bytes
Peripheral Bridge C	0x400E0000	64 Kbytes
Peripheral Bridge D	0x400F0000	64 Kbytes

Table 5-2. Flash Memory Parameters

Device	Flash Size (*FLASH_PW*)	Number of Pages (*FLASH_P*)	Page Size (*FLASH_W*)
ATSAM4Lx8	512 Kbytes	1024	512 bytes
ATSAM4Lx4	256 Kbytes	512	512 bytes
ATSAM4Lx2	128 Kbytes	256	512 bytes

8.3 Block diagram

Figure 8-1. Debug and Test Block Diagram



note: Boxes with a plain corner are SAM4L specific.

8.4 I/O Lines Description

Refer to Section 1.1.4 ”I/O Lines Description” on page 4.

8.9.11.1 Control Register

Name: CR

Access Type: Write-Only

Offset: 0x00

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	CE	FSPR	CRC	DIS	EN

Writing a zero to a bit in this register has no effect.

- **CE: Chip Erase**
  Writing a one to this bit triggers the FLASH Erase All (EA) operation which clears all volatile memories, the whole flash array, the general purpose fuses and the protected state. The Status register DONE field indicates the completion of the operation.
  Reading this bit always returns 0
- **FSPR: Flash User Page Read**
  Writing a one to this bit triggers a read operation in the User page. The word pointed by the ADDR register in the page is read and written to the DATA register. ADDR is post incremented allowing a burst of reads without modifying ADDR. SR.DONE must be read high prior to reading the DATA register.
  Reading this bit always returns 0
- **CRC: Cyclic Redundancy Code**
  Writing a one triggers a CRC calculation over a memory area defined by the ADDR and LENGTH registers. Reading this bit always returns 0
  Note: This feature is restricted while in protected state
- **DIS: Disable**
  Writing a one to this bit disables the module. Disabling the module resets the whole module immediately.
- **EN: Enable**
  Writing a one to this bit enables the module.

Table 9-5. Maximum Clock Frequencies in Power Scaling Mode 1 and RUN Mode

Symbol	Parameter	Description	Max	Units
f_{CPU}	CPU clock frequency		12	MHz
f_{PBA}	PBA clock frequency		12	
f_{PBB}	PBB clock frequency		12	
f_{PBC}	PBC clock frequency		12	
f_{PBD}	PBD clock frequency		12	
f_{GCLK0}	GCLK0 clock frequency	DFLLIF main reference, GCLK0 pin	16.6	
f_{GCLK1}	GCLK1 clock frequency	DFLLIF dithering and SSGreference, GCLK1 pin	16.6	
f_{GCLK2}	GCLK2 clock frequency	AST, GCLK2 pin	6.6	
f_{GCLK3}	GCLK3 clock frequency	CATB, GCLK3 pin	17.3	
f_{GCLK4}	GCLK4 clock frequency	FLO and AESA	16.6	
f_{GCLK5}	GCLK5 clock frequency	GLOC, TC0 and RC32KIFB_REF	26.6	
f_{GCLK6}	GCLK6 clock frequency	ABDACB and IISC	16.6	
f_{GCLK7}	GCLK7 clock frequency	USBC	16.6	
f_{GCLK8}	GCLK8 clock frequency	TC1 and PEVC[0]	16.6	
f_{GCLK9}	GCLK9 clock frequency	PLL0 and PEVC[1]	16.6	
f_{GCLK10}	GCLK10 clock frequency	ADCIFE	16.6	
f_{GCLK11}	GCLK11 clock frequency	Master generic clock. Can be used as source for other generic clocks	51.2	
f_{OSC0}	OSC0 output frequency	Oscillator 0 in crystal mode	16	
		Oscillator 0 in digital clock mode	16	
f_{PLL}	PLL output frequency	Phase Locked Loop	N/A	
f_{DFLL}	DFLL output frequency	Digital Frequency Locked Loop	N/A	
f_{RC80M}	RC80M output frequency	Internal 80MHz RC Oscillator	N/A	

- Operating conditions, internal core supply (Figure 9-2)
  - V_{VDDIN} = 3.3V
  - $V_{VDDCORE}$ = 1.2 V, supplied by the internal regulator in switching mode
- T_A = 25°C
- Oscillators
  - OSC0 (crystal oscillator) stopped
  - OSC32K (32KHz crystal oscillator) running with external 32KHz crystal
  - RCFAST running @ 12MHz
- Clocks
  - RCFAST used as main clock source
  - CPU, AHB, and PB clocks undivided
- I/Os are inactive with internal pull-up
- Flash enabled in normal mode
- CPU in SLEEP0 mode
- BOD18 and BOD33 disabled

Consumption active is the added current consumption when the module clock is turned on

9.6 I/O Pin Characteristics

9.6.1 Normal I/O Pin

Table 9-13. Normal I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			V
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			0.8	mA
			2.7V<V_{VDD}<3.6V			1.6	mA
		ODCR0=1	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	mA
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			0.8	mA
			2.7V<V_{VDD}<3.6V			1.6	mA
		ODCR0=1	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	mA
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, load = 25pF			35	ns
		OSRR0=1				45	ns
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, load = 25pF			19	ns
		OSRR0=1				23	ns
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, load = 25pF			36	ns
		OSRR0=1				47	ns
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, load = 25pF			20	ns
		OSRR0=1				24	ns
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			17	MHz
		OSRR0=1				15	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			27	MHz
		OSRR0=1				23	MHz
I_{LEAK}	Input leakage current(3)		Pull-up resistors disabled		0.01	1	µA
C_{IN}	Input capacitance(2)				5		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization

3. These values are based on characterization. These values are not covered by test limits in production

9.6.2 High-drive I/O Pin : PA02, PC04, PC05, PC06

Table 9-14. High-drive I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.8	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			22	MHz
		OSRR0=1				17	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			35	MHz
		OSRR0=1				26	MHz
I_{LEAK}	Input leakage current(3)	Pull-up resistors disabled			0.01	2	µA
C_{IN}	Input capacitance(2)				10		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.9 Analog Characteristics

9.9.1 Voltage Regulator Characteristics

Table 9-36. VREG Electrical Characteristics in Linear and Switching Modes

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	DC output current (1) Power scaling mode 0 & 2	Low power mode (WAIT)	2000	3600	5600	µA
		Ultra Low power mode (RETENTION)	100	180	300	
	DC output current(1) Power scaling mode 1	Low power mode (WAIT)	4000	7000	10000	
		Ultra Low power mode (RETENTION)	200	350	600	
$V_{VDDCORE}$	DC output voltage	All modes			1.9	V

1. These values are based on simulation. These values are not covered by test limits in production.

Table 9-37. VREG Electrical Characteristics in Linear mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VDDIN}	Input voltage range	I_{OUT}=10mA	1.68		3.6	V
		I_{OUT}=50mA	1.8		3.6	
$V_{VDDCORE}$	DC output voltage (1) Power scaling mode 0 & 2	I_{OUT} = 0 mA	1.777	1.814	1.854	
		I_{OUT} = 50 mA	1.75	1.79	1.83	
I_{OUT}	DC output current(1)	$V_{VDDCORE}$ > 1.65V			100	mA
	Output DC load regulation(1) Transient load regulation	I_{OUT} = 0 to 80mA, V_{VDDIN} = 3V	-34	-27	-19	mV
	Output DC regulation(1)	I_{OUT} = 80 mA, V_{VDDIN} = 2V to 3.6V	10	28	48	mV
I_Q	Quescient current(1)	I_{OUT} = 0 mA RUN and SLEEPx modes	88	107	128	µA

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-38. External components requirements in Linear Mode

Symbol	Parameter	Technology	Typ	Units
C_{IN1}	Input regulator capacitor 1		33	nF
C_{IN2}	Input regulator capacitor 2		100	
C_{IN3}	Input regulator capacitor 3		10	µF
C_{OUT1}	Output regulator capacitor 1		100	nF
C_{OUT2}	Output regulator capacitor 2	Tantalum or MLCC 0.5<ESR<10Ω	4.7	µF

Table 9-39. VREG Electrical Characteristics in Switching mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VDDIN}	Input voltage range	$V_{VDDCORE}$ = 1.65V, I_{OUT}=50mA	2.0		3.6	V
$V_{VDDCORE}$	DC output voltage (1) Power scaling mode 0 & 2	I_{OUT} = 0 mA	1.75	1.82	1.87	
		I_{OUT} = 50 mA	1.66	1.71	1.79	

9.9.7 Liquid Crystal Display Controler characteristics

Table 9-51. Liquid Crystal Display Controler characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SEG	Segment Terminal Pins				40	
COM	Common Terminal Pins				4	
f_{Frame}	LCD Frame Frequency	F_{CLKLCD}	31.25		512	Hz
C_{Flying}	Flying Capacitor			100		nF
V_{LCD}	LCD Regulated Voltages (1) CFG.FCST=0	C_{Flying} = 100nF 100nF on V_{LCD}, BIAS2 and BIAS1 pins		3		V
BIAS2				$2*V_{LCD}/3$		
BIAS1				$V_{LCD}/3$		

1. These values are based on simulation. These values are not covered by test limits in production or characterization

9.9.7.1 Liquid Crystal Controler supply current

The values in Table 9-52 are measured values of power consumption under the following conditions, except where noted:

- T=25°C, WAIT mode, Low power waveform, Frame Rate = 32Hz from OSC32K
- Configuration: 4COMx40SEG, 1/4 Duty, 1/3 Bias, No animation
- All segments on, Load = 160 x 22pF between each COM and each SEG.
- LCDCA current based on $I_{LCD} = I_{WAIT}$(Lcd On) - I_{WAIT}(Lcd Off)

Table 9-52. Liquid Crystal Display Controler supply current

Symbol	Conditions		Min	Typ	Max	Units
I_{LCD}	Internal voltage generation CFG.FCST=0	V_{VDDIN} = 3.6V		8.85		µA
		V_{VDDIN} = 1.8V		6.16		
	External bias V_{LCD}=3.0V	V_{VDDIN} = 3.3V		0.98		
		V_{VDDIN} = 1.8V		1.17		

Table 9-61. USART3 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		593.9	ns
USPI7	MOSI setup time before SPCK rises		45.93 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		47.03 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			593.38	
USPI10	MOSI setup time before SPCK falls		45.93 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		47.03 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		237.5		
USPI13	NSS hold time after SPCK falls		-1.81		
USPI14	NSS setup time before SPCK falls		237.5		
USPI15	NSS hold time after SPCK rises		-1.81		

Notes: 1. These values are based on simulation. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left(\left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor + \frac{1}{2}\right) \times t_{CLKUSART}$

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, USPI7 + USPI8 or USPI10 + USPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

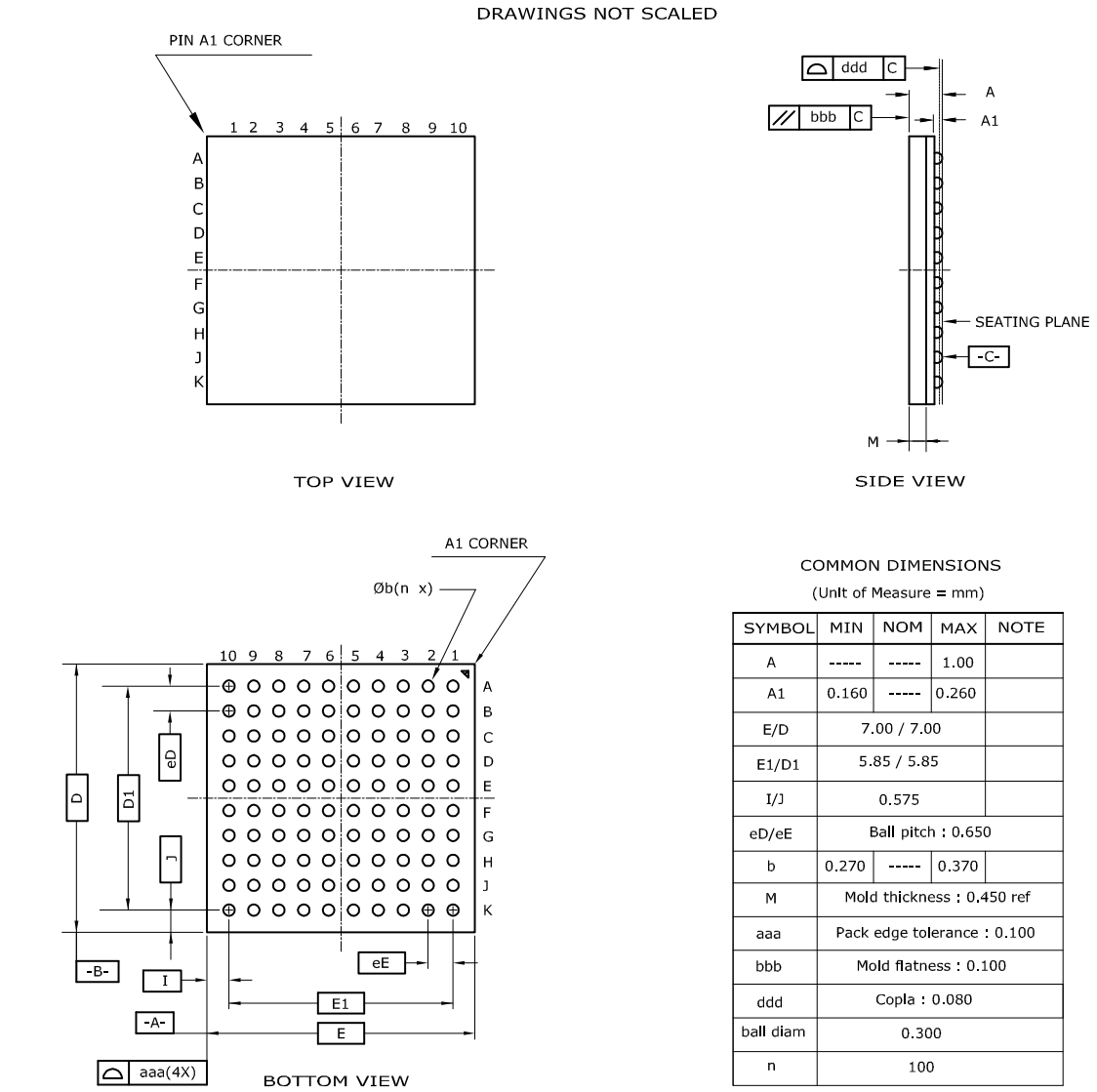
The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

Where $SPIn$ is the MISO delay, USPI6 or USPI9 depending on CPOL and NCPHA. T_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for T_{SETUP} . f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

10.2 Package Drawings

Figure 10-1. VFBGA-100 package drawing



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.00	
A1	0.160	-----	0.260	
E/D	7.00 / 7.00			
E1/D1	5.85 / 5.85			
I/J	0.575			
eD/eE	Ball pitch : 0.650			
b	0.270	-----	0.370	
M	Mold thickness : 0.450 ref			
aaa	Pack edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Copla : 0.080			
ball diam	0.300			
n	100			

Notes : 1. No JEDEC Drawing Reference.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

Table 10-2. Device and Package Maximum Weight

120	mg

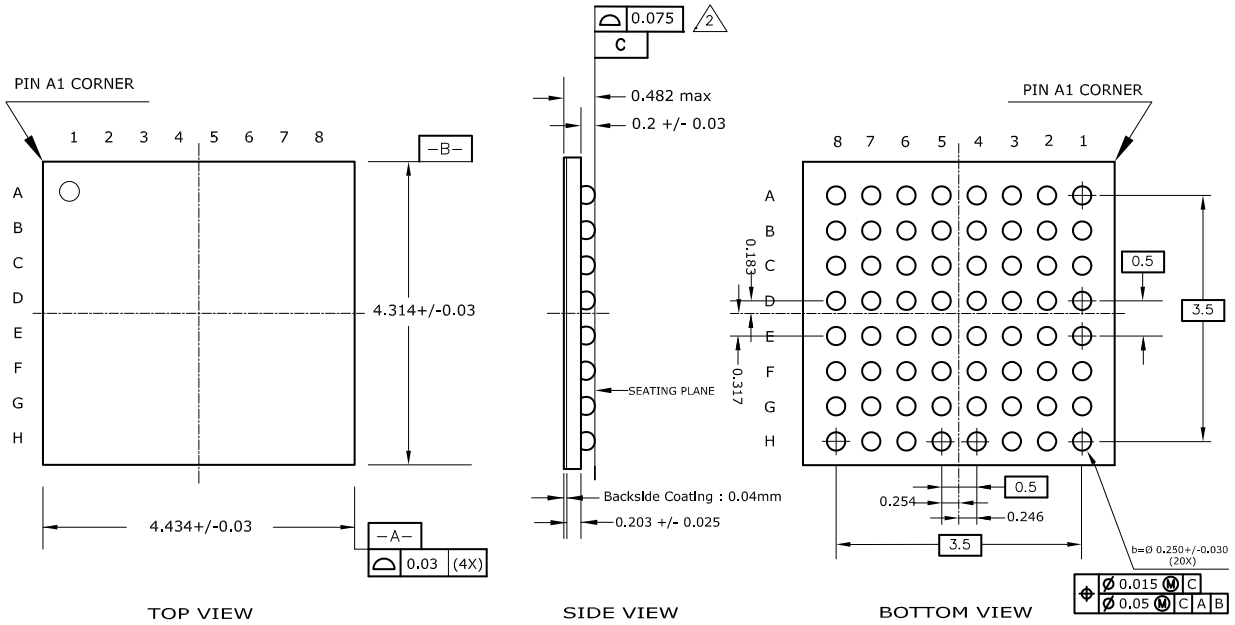
Table 10-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-4. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

Figure 10-4. WLCSP64 SAM4LS4/2 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.746	1.683
A2	GNDANA	1.246	1.683
A3	ADVREFP	0.746	1.683
A4	VDDANA	0.246	1.683
A5	PA09	-0.254	1.683
A6	PA28	-0.754	1.683
A7	PA27	-1.254	1.683
A8	PA12	-1.754	1.683
B1	PB03	1.746	1.183
B2	XIN32	1.246	1.183
B3	XOUT32	0.746	1.183
B4	PA08	0.246	1.183
B5	PB06	-0.254	1.183
B6	PA10	-0.754	1.183
B7	PA11	-1.254	1.183
B8	PA29	-1.754	1.183
C1	VDDIN	1.746	0.683
C2	PB01	1.246	0.683
C3	PA05	0.746	0.683
C4	PA06	0.246	0.683
C5	PA07	-0.254	0.683
C6	PB07	-0.754	0.683

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	-1.254	0.683
C8	GNDIO0	-1.754	0.683
D1	VDDOUT	1.746	0.183
D2	PB00	1.246	0.183
D3	PA04	0.746	0.183
D4	PB05	0.246	0.183
D5	PB12	-0.254	0.183
D6	PB08	-0.754	0.183
D7	PA14	-1.254	0.183
D8	VLCDIN	-1.754	0.183
E1	GNDIN	1.746	-0.317
E2	PA03	1.246	-0.317
E3	PB02	0.746	-0.317
E4	RESET_N	0.246	-0.317
E5	PB13	-0.254	-0.317
E6	PB09	-0.754	-0.317
E7	PA15	-1.254	-0.317
E8	PA30	-1.754	-0.317
F1	VDDCORE	1.746	-0.817
F2	TCK	1.246	-0.817
F3	PA02	0.746	-0.817
F4	PB14	0.246	-0.817

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.254	-0.817
F6	PB10	-0.754	-0.817
F7	PA16	-1.254	-0.817
F8	PA31	-1.754	-0.817
G1	GNDIO1	1.746	-1.317
G2	PA26	1.246	-1.317
G3	PA24	0.746	-1.317
G4	PA00	0.246	-1.317
G5	PA01	-0.254	-1.317
G6	PA19	-0.754	-1.317
G7	PA18	-1.254	-1.317
G8	PA17	-1.754	-1.317
H1	VDDIO1	1.746	-1.817
H2	PA25	1.246	-1.817
H3	PA23	0.746	-1.817
H4	PB15	0.246	-1.817
H5	PA21	-0.254	-1.817
H6	VDDIO0	-0.754	-1.817
H7	PA20	-1.254	-1.817
H8	PB11	-1.754	-1.817

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-11. Device and Package Maximum Weight

14.8	mg

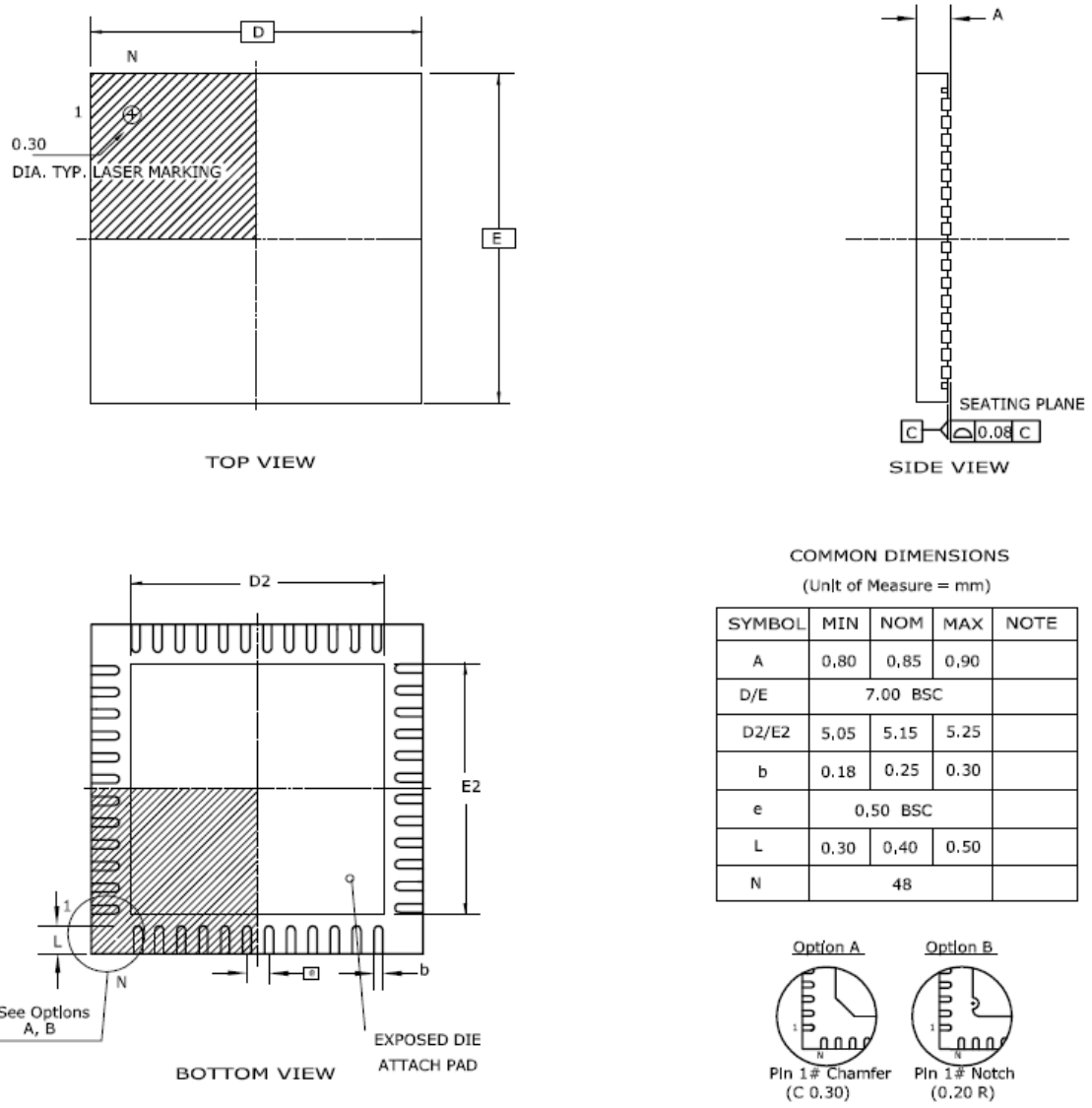
Table 10-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

Figure 10-10. QFN-48 Package Drawing for ATSAM4LC4/2 and ATSAM4LS4/2



SYMBOL	MIN	NOM	MAX	NOTE
A	0,80	0,85	0,90	
D/E		7.00 BSC		
D2/E2	5,05	5.15	5.25	
b	0.18	0.25	0.30	
e		0,50 BSC		
L	0.30	0,40	0.50	
N		48		

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 10-29. Device and Package Maximum Weight

140	mg

Table 10-30. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-31. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3