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## What is "Embedded - Microcontrollers"?

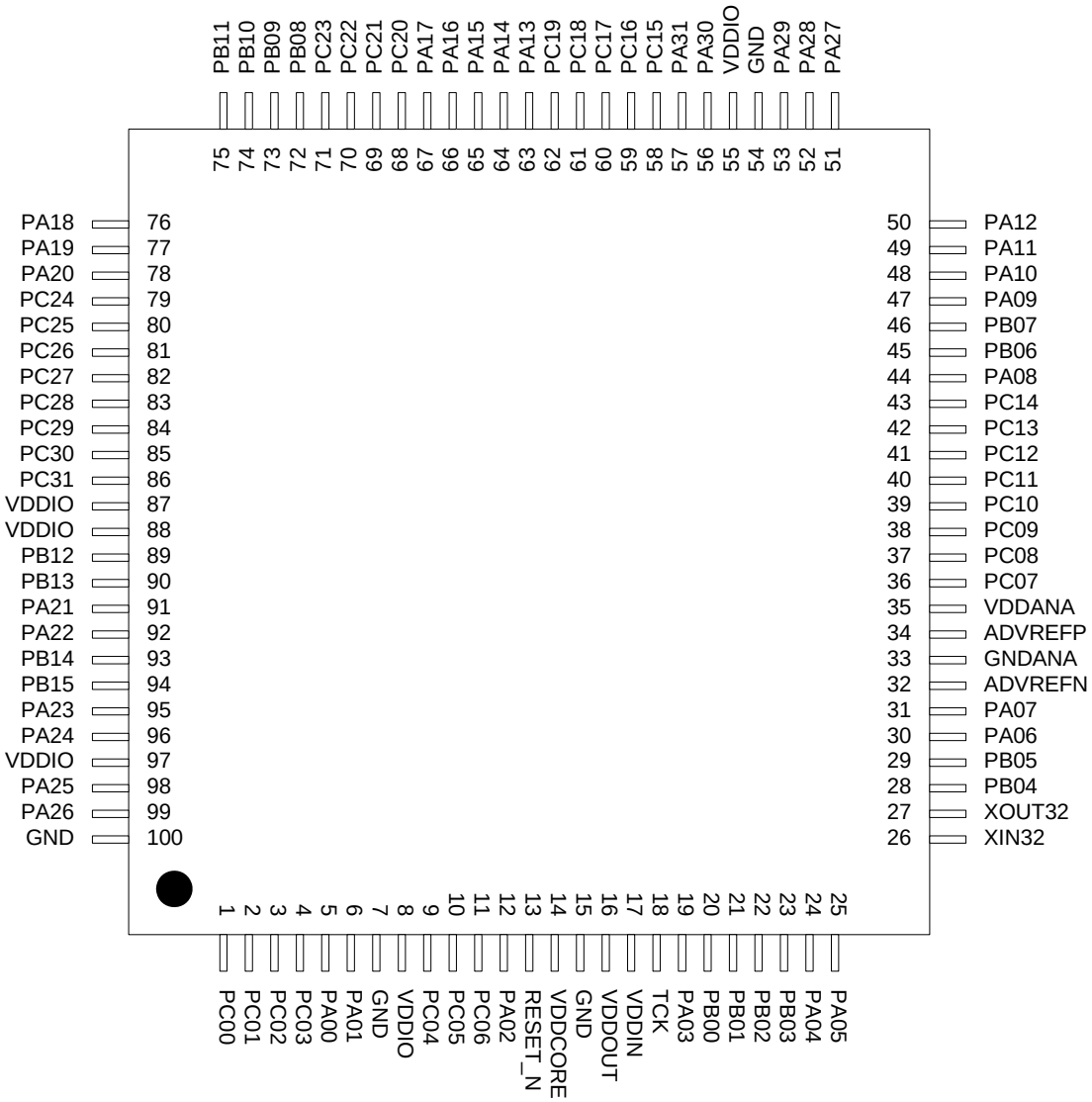
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 43 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.68V ~ 3.6V |
| Data Converters | A/D 7x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-TQFP |
| Supplier Device Package | 64-TQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atsam4lc2ba-au |

### 3.1.2 ATSAM4LSx Pinout

**Figure 3-6.** ATSAM4LS TQFP100 Pinout



## 3.2 Peripheral Multiplexing on I/O lines

### 3.2.1 Multiplexed Signals

Each GPIO line can be assigned to one of the peripheral functions. The following tables (Section 3-1 ”100-pin GPIO Controller Function Multiplexing” on page 19 to Section 3-4 ”48-pin GPIO Controller Function Multiplexing” on page 28) describes the peripheral signals multiplexed to the GPIO lines.

Peripheral functions that are not relevant in some parts of the family are grey-shaded.

For description of differents Supply voltage source, refer to the Section 6. ”Power and Startup Considerations” on page 46.

**Table 3-1.** 100-pin GPIO Controller Function Multiplexing (Sheet 1 of 4)

| ATSAM4LC | | ATSAM4LS | | Pin | GPIO | Supply | GPIO Functions | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| QFN | VFBGA | QFN | VFBGA | | | | A | B | C | D | E | F | G |
| 5 | B9 | 5 | B9 | PA00 | 0 | VDDIO | | | | | | | |
| 6 | B8 | 6 | B8 | PA01 | 1 | VDDIO | | | | | | | |
| 12 | A7 | 12 | A7 | PA02 | 2 | VDDIN | SCIF GCLK0 | SPI NPCS0 | | | | | CATB DIS |
| 19 | B3 | 19 | B3 | PA03 | 3 | VDDIN | | SPI MISO | | | | | |
| 24 | A2 | 24 | A2 | PA04 | 4 | VDDANA | ADCIFE AD0 | USART0 CLK | EIC EXTINT2 | GLOC IN1 | | | CATB SENSE0 |
| 25 | A1 | 25 | A1 | PA05 | 5 | VDDANA | ADCIFE AD1 | USART0 RXD | EIC EXTINT3 | GLOC IN2 | ADCIFE TRIGGER | | CATB SENSE1 |
| 30 | C3 | 30 | C3 | PA06 | 6 | VDDANA | DACC VOUT | USART0 RTS | EIC EXTINT1 | GLOC IN0 | ACIFC ACAN0 | | CATB SENSE2 |
| 31 | D3 | 31 | D3 | PA07 | 7 | VDDANA | ADCIFE AD2 | USART0 TXD | EIC EXTINT4 | GLOC IN3 | ACIFC ACAP0 | | CATB SENSE3 |
| 44 | G2 | 44 | G2 | PA08 | 8 | LCDA | USART0 RTS | TC0 A0 | PEVC PAD EVT0 | GLOC OUT0 | | LCDCA SEG23 | CATB SENSE4 |
| 47 | F5 | 47 | F5 | PA09 | 9 | LCDA | USART0 CTS | TC0 B0 | PEVC PAD EVT1 | PARC PCDATA0 | | LCDCA COM3 | CATB SENSE5 |
| 48 | H2 | 48 | H2 | PA10 | 10 | LCDA | USART0 CLK | TC0 A1 | PEVC PAD EVT2 | PARC PCDATA1 | | LCDCA COM2 | CATB SENSE6 |
| 49 | H3 | 49 | H3 | PA11 | 11 | LCDA | USART0 RXD | TC0 B1 | PEVC PAD EVT3 | PARC PCDATA2 | | LCDCA COM1 | CATB SENSE7 |
| 50 | J2 | 50 | J2 | PA12 | 12 | LCDA | USART0 TXD | TC0 A2 | | PARC PCDATA3 | | LCDCA COM0 | CATB DIS |
| 63 | H5 | 63 | H5 | PA13 | 13 | LCDA | USART1 RTS | TC0 B2 | SPI NPCS1 | PARC PCDATA4 | | LCDCA SEG5 | CATB SENSE8 |
| 64 | K7 | 64 | K7 | PA14 | 14 | LCDA | USART1 CLK | TC0 CLK0 | SPI NPCS2 | PARC PCDATA5 | | LCDCA SEG6 | CATB SENSE9 |
| 65 | G5 | 65 | G5 | PA15 | 15 | LCDA | USART1 RXD | TC0 CLK1 | SPI NPCS3 | PARC PCDATA6 | | LCDCA SEG7 | CATB SENSE10 |

**Table 3-1.** 100-pin GPIO Controller Function Multiplexing (Sheet 4 of 4)

| ATSAM4LC | | ATSAM4LS | | Pin | GPIO | Supply | GPIO Functions | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| QFN | VFBGA | QFN | VFBGA | | | | A | B | C | D | E | F | G |
| 59 | J6 | 59 | J6 | PC16 | 80 | LCDA | TC1 B0 | | | GLOC IN5 | | LCDCA SEG1 | CATB SENSE17 |
| 60 | H4 | 60 | H4 | PC17 | 81 | LCDA | TC1 A1 | | | GLOC IN6 | | LCDCA SEG2 | CATB SENSE18 |
| 61 | K6 | 61 | K6 | PC18 | 82 | LCDA | TC1 B1 | | | GLOC IN7 | | LCDCA SEG3 | CATB SENSE19 |
| 62 | G4 | 62 | G4 | PC19 | 83 | LCDA | TC1 A2 | | | GLOC OUT1 | | LCDCA SEG4 | CATB SENSE20 |
| 68 | H7 | 68 | H7 | PC20 | 84 | LCDA | TC1 B2 | | | | | LCDCA SEG10 | CATB SENSE21 |
| 69 | K8 | 69 | K8 | PC21 | 85 | LCDA | TC1 CLK0 | | | PARC PCCK | | LCDCA SEG11 | CATB SENSE22 |
| 70 | J8 | 70 | J8 | PC22 | 86 | LCDA | TC1 CLK1 | | | PARC PCEN1 | | LCDCA SEG12 | CATB SENSE23 |
| 71 | H8 | 71 | H8 | PC23 | 87 | LCDA | TC1 CLK2 | | | PARC PCEN2 | | LCDCA SEG13 | CATB DIS |
| 79 | J9 | 79 | J9 | PC24 | 88 | LCDB | USART1 RTS | EIC EXTINT1 | PEVC PAD EVT0 | PARC PCDATA0 | | LCDCA SEG24 | CATB SENSE24 |
| 80 | H9 | 80 | H9 | PC25 | 89 | LCDB | USART1 CLK | EIC EXTINT2 | PEVC PAD EVT1 | PARC PCDATA1 | | LCDCA SEG25 | CATB SENSE25 |
| 81 | G9 | 81 | G9 | PC26 | 90 | LCDB | USART1 RXD | EIC EXTINT3 | PEVC PAD EVT2 | PARC PCDATA2 | SCIF GCLK0 | LCDCA SEG26 | CATB SENSE26 |
| 82 | F6 | 82 | F6 | PC27 | 91 | LCDB | USART1 TXD | EIC EXTINT4 | PEVC PAD EVT3 | PARC PCDATA3 | SCIF GCLK1 | LCDCA SEG27 | CATB SENSE27 |
| 83 | G10 | 83 | G10 | PC28 | 92 | LCDB | USART3 RXD | SPI MISO | GLOC IN4 | PARC PCDATA4 | SCIF GCLK2 | LCDCA SEG28 | CATB SENSE28 |
| 84 | F7 | 84 | F7 | PC29 | 93 | LCDB | USART3 TXD | SPI MOSI | GLOC IN5 | PARC PCDATA5 | SCIF GCLK3 | LCDCA SEG29 | CATB SENSE29 |
| 85 | F8 | 85 | F8 | PC30 | 94 | LCDB | USART3 RTS | SPI SCK | GLOC IN6 | PARC PCDATA6 | SCIF GCLK IN0 | LCDCA SEG30 | CATB SENSE30 |
| 86 | F9 | 86 | F9 | PC31 | 95 | LCDB | USART3 CLK | SPI NPCS0 | GLOC OUT1 | PARC PCDATA7 | SCIF GCLK IN1 | LCDCA SEG31 | CATB SENSE31 |

**Table 3-2.** 64-pin GPIO Controller Function Multiplexing (Sheet 1 of 3)

| ATSAM4LC | ATSAM4LS | Pin | GPIO | Supply | GPIO Functions | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| QFP QFN | QFP QFN | | | | A | B | C | D | E | F | G |
| 1 | 1 | PA00 | 0 | VDDIO | | | | | | | |
| 2 | 2 | PA01 | 1 | VDDIO | | | | | | | |
| 3 | 3 | PA02 | 2 | VDDIN | SCIF GCLK0 | SPI NPCS0 | | | | | CATB DIS |
| 10 | 10 | PA03 | 3 | VDDIN | | SPI MISO | | | | | |

### 3.4.7 ADC Input Pins

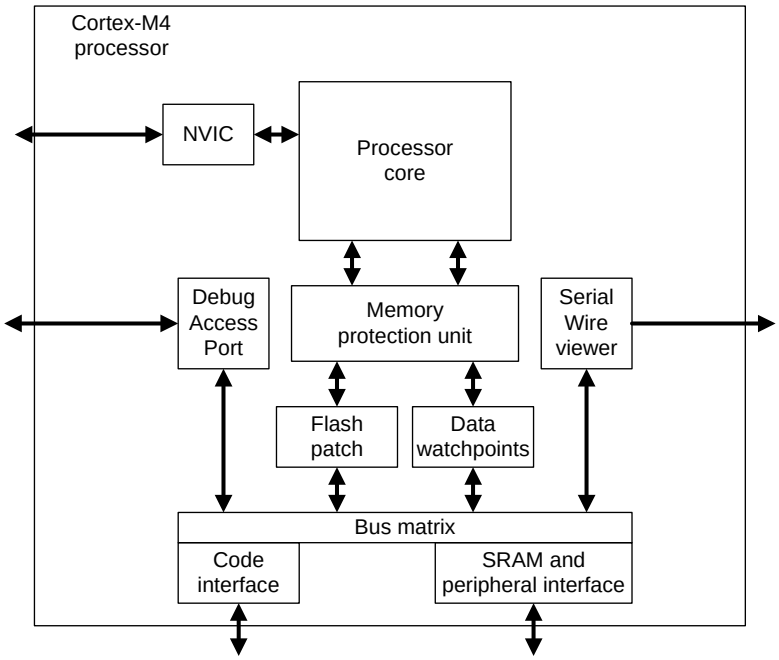
These pins are regular I/O pins powered from the VDDANA.

# 4. Cortex-M4 processor and core peripherals

## 4.1 Cortex-M4

The Cortex-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- **outstanding processing performance combined with fast interrupt handling**
- **enhanced system debug with extensive breakpoint and trace capabilities**
- **efficient processor core, system and memories**
- **ultra-low power consumption with integrated sleep modes**
- **platform security robustness, with integrated memory protection unit (MPU).**




The Cortex-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division.

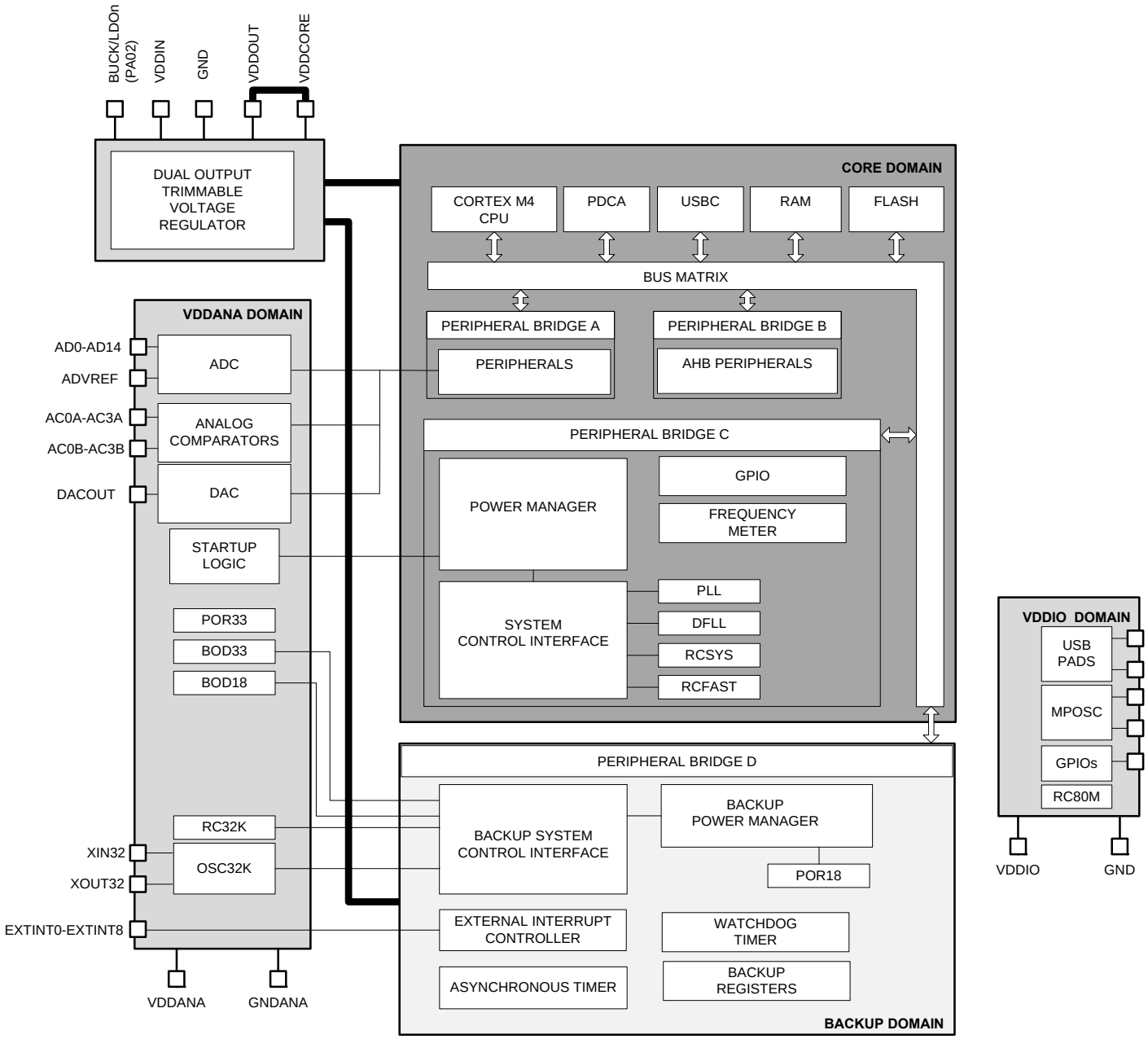
To facilitate the design of cost-sensitive devices, the Cortex-M4 processor implements tightly-coupled system components that reduce processor area while significantly improving interrupt handling and system debug capabilities. The Cortex-M4 processor implements a version of the Thumb® instruction set based on Thumb-2 technology, ensuring high code density and reduced program memory requirements. The Cortex-M4 instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers.

The Cortex-M4 processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC includes a *non-maskable interrupt* (NMI), and provides up to 80 interrupt priority levels. The tight integration of the proces-

# 6. Power and Startup Considerations

## 6.1 Power Domain Overview

**Figure 6-1.** ATSAM4LS Power Domain Diagram



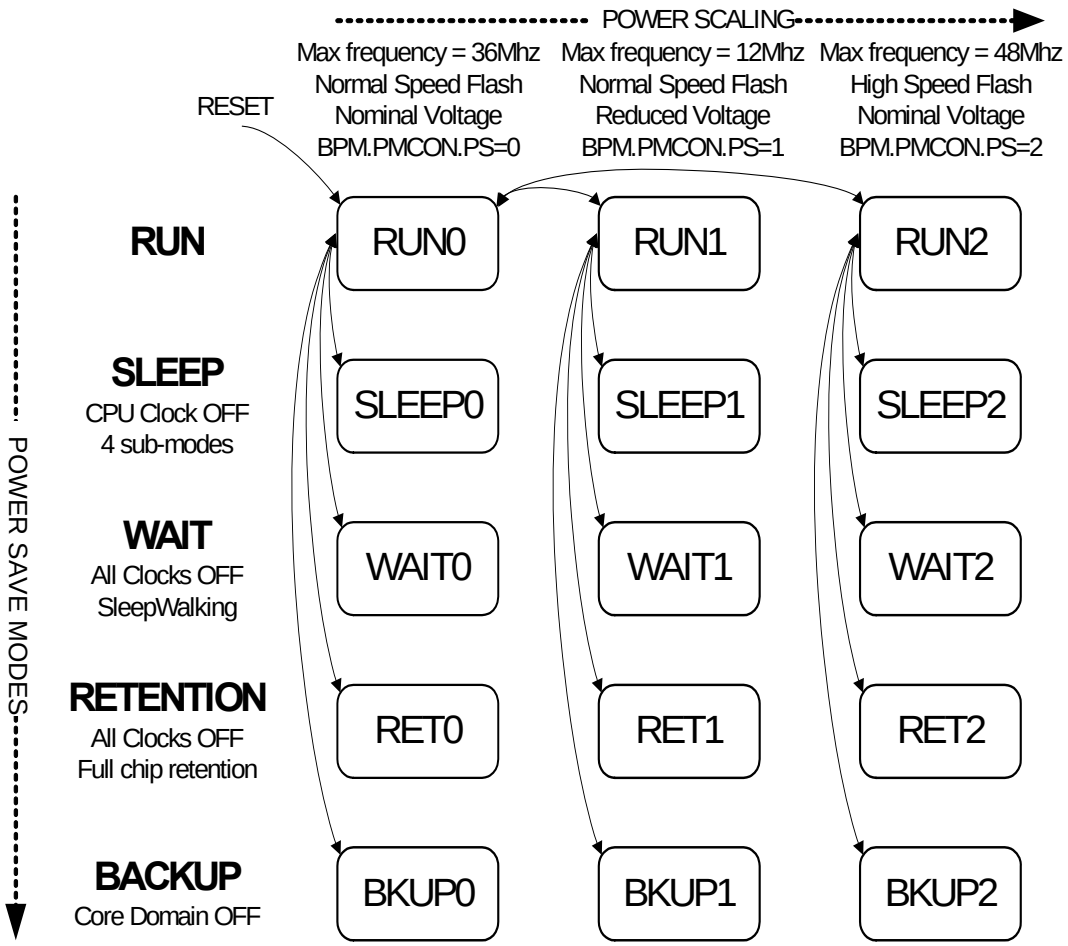
# 7. Low Power Techniques

The ATSAM4L8/L4/L2 supports multiple power configurations to allow the user to optimize its power consumption in different use cases. The Backup Power Manager (BPM) implements different solutions to reduce the power consumption:

- The Power Save modes intended to reduce the logic activity and to adapt the power configuration. See "Power Save Modes" on page 55.
- The Power Scaling intended to scale the power configuration (voltage scaling of the regulator). See "Power Scaling" on page 60.

These two techniques can be combined together.

**Figure 7-1.** Power Scaling and Power Save Mode Overview




## 7.1 Power Save Modes

Refer to Section 6. "Power and Startup Considerations" on page 46 to get definition of the core and the backup domains.

mechanism can be useful for applications that only require the processor to run when an interrupt occurs.

Before entering the SLEEP mode, the user must configure:

- the SLEEP mode configuration field (BPM.PMCON.SLEEP), Refer to Table 7-1.
- the SCR.SLEEPDEEP bit to 0. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- the BPM.PMCON.RET bit to 0.
- the BPM.PMCON.BKUP bit to 0.

#### *7.1.1.2 Exiting SLEEP mode*

The NVIC wakes the system up when it detects any non-masked interrupt with sufficient priority to cause exception entry. The system goes back to the RUN mode from which the SLEEP mode was entered. The CPU and affected modules are restarted. Note that even if an interrupt is enabled in SLEEP mode, it will not trigger if the source module is not clocked.

### 7.1.2 WAIT Mode and RETENTION Mode

The WAIT and RETENTION modes allow achieving very low power consumption while maintaining the Core domain powered-on. Internal SRAM and registers contents of the Core domain are preserved.

In these modes, all clocks are stopped except the 32kHz clocks (OSC32K, RC32K) which are kept running if enabled.

In RETENTION mode, the SleepWalking feature is not supported and must not be used.

#### *7.1.2.1 Entering WAIT or RETENTION Mode*

The WAIT or RETENTION modes are entered by executing the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 0.
- set the BPM.PMCON.RET bit to RETENTION or WAIT mode.

SLEEPONEXIT feature is also available. See ”Entering SLEEP mode” on page 56.

#### *7.1.2.2 Exiting WAIT or RETENTION Mode*

In WAIT or RETENTION modes, synchronous clocks are stopped preventing interrupt sources from triggering. To wakeup the system, asynchronous wake up sources (AST, EIC, USBC ...) should be enabled in the peripheral (refer to the documentation of the peripheral). The PM.AWEN (Asynchronous Wake Up Enable) register should also be enabled for all peripheral except for EIC and AST.

When the enabled asynchronous wake up event occurs and the system is waken-up, it will generate either:

- an interrupt on the PM WAKE interrupt line if enabled (Refer to Section 9. ”Power Manager (PM)” on page 677). In that case, the PM.WCAUSE register indicates the wakeup source.
- or an interrupt directly from the peripheral if enabled (Refer to the section of the peripheral).

When waking up, the system goes back to the RUN mode mode from which the WAIT or RETENTION mode was entered.

## 8.7 Enhanced Debug Port (EDP)

Rev.: 1.0.0.0

### 8.7.1 Features

- **IEEE1149.1 compliant JTAG debug port**
- **Serial Wire Debug Port**
- **Boundary-Scan chain on all digital pins for board-level testing**
- **Debugger Hot-Plugging**
- **SMAP core reset request source**

### 8.7.2 Overview

The enhanced debug port embeds a standard ARM debug port plus some specific hardware intended for testability and activation of the debug port features. All the information related to the ARM Debug Interface implementation can be found in the ARM Debug Interface v5.1 Architecture Specification document.

It features:

- A single Debug Port (SWJ-DP), that provides the external physical connection to the interface and supports two DP implementations:
  - the JTAG Debug Port (JTAG-DP)
  - the Serial Wire Debug Port (SW-DP)
- A supplementary JTAG TAP (BSCAN-TAP) connected in parallel with the JTAG-DP that implements the boundary scan instructions detailed in
- A JTAG-FILTER module that monitors TCK and RESET_N pins to handle specific features like the detection of a debugger hot-plugging and the request of reset of the Cortex-M4 at startup.

The JTAG-FILTER module detects the presence of a debugger. When present, JTAG pins are automatically assigned to the Enhanced Debug Port(EDP). If the SWJ-DP is switched to the SW mode, then TDI and TDO alternate functions are released. The JTAG-FILTER also implements a CPU halt mechanism. When triggered, the Cortex-M4 is maintained under reset after the external reset is released to prevent any system corruption during later programmation operations.

### 8.11.8 Chip erase typical procedure

The chip erase operation is triggered by writing a one in the CE bit in the Control Register (CR.CE). This clears first all volatile memories in the system and second the whole flash array. Note that the User page is not erased in this process. To ensure that the chip erase operation is completed, check the DONE bit in the Status Register (SR.DONE). Also note that the chip erase operation depends on clocks and power management features that can be altered by the CPU. It is important to ensure that it is stopped. The recommended sequence is shown below:

1. At power up, RESET_N is driven low by a debugger. The on-chip regulator holds the system in a POR state until the input supply is above the POR threshold. The system continues to be held in this static state until the internally regulated supplies have reached a safe operating.
2. PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock, and any Bus Clocks that do not have clock gate control). Internal resets are maintained due to the external reset.
   – The debug port and access ports receives a clock and leave the reset state
3. The debugger maintains a low level on TCK and release RESET_N.
   – The SMAP asserts the core_hold_reset signal
4. The Cortex-M4 core remains in reset state, meanwhile the rest of the system is released.
5. The Chip erase operation can be performed by issuing the SMAP Chip Erase command. In this case:
   – volatile memories are cleared first
   – followed by the clearing of the flash array
   – followed by the clearing of the protected state
6. After operation is completed, the chip must be restarted by either controling RESET_N or switching power off/on. Make sure that the TCK pin is high when releasing RESET_N not to halt the core.

### 8.11.9 Setting the protected state

This is done by issuing a specific flash controller command, for more information, refer to the Flash Controller chapter and to section 8.11.7Flash Programming typical procedure97. The protected state is defined by a highly secure Flash builtin mechanism. Note that for this programmation to propagate, it is required to reset the chip.

**Table 9-5.** Maximum Clock Frequencies in Power Scaling Mode 1 and RUN Mode

| Symbol | Parameter | Description | Max | Units |
|---|---|---|---|---|
| $f_{CPU}$ | CPU clock frequency | | 12 | MHz |
| $f_{PBA}$ | PBA clock frequency | | 12 | |
| $f_{PBB}$ | PBB clock frequency | | 12 | |
| $f_{PBC}$ | PBC clock frequency | | 12 | |
| $f_{PBD}$ | PBD clock frequency | | 12 | |
| $f_{GCLK0}$ | GCLK0 clock frequency | DFLLIF main reference, GCLK0 pin | 16.6 | |
| $f_{GCLK1}$ | GCLK1 clock frequency | DFLLIF dithering and SSGreference, GCLK1 pin | 16.6 | |
| $f_{GCLK2}$ | GCLK2 clock frequency | AST, GCLK2 pin | 6.6 | |
| $f_{GCLK3}$ | GCLK3 clock frequency | CATB, GCLK3 pin | 17.3 | |
| $f_{GCLK4}$ | GCLK4 clock frequency | FLO and AESA | 16.6 | |
| $f_{GCLK5}$ | GCLK5 clock frequency | GLOC, TC0 and RC32KIFB_REF | 26.6 | |
| $f_{GCLK6}$ | GCLK6 clock frequency | ABDACB and IISC | 16.6 | |
| $f_{GCLK7}$ | GCLK7 clock frequency | USBC | 16.6 | |
| $f_{GCLK8}$ | GCLK8 clock frequency | TC1 and PEVC[0] | 16.6 | |
| $f_{GCLK9}$ | GCLK9 clock frequency | PLL0 and PEVC[1] | 16.6 | |
| $f_{GCLK10}$ | GCLK10 clock frequency | ADCIFE | 16.6 | |
| $f_{GCLK11}$ | GCLK11 clock frequency | Master generic clock. Can be used as source for other generic clocks | 51.2 | |
| $f_{OSC0}$ | OSC0 output frequency | Oscillator 0 in crystal mode | 16 | |
| | | Oscillator 0 in digital clock mode | 16 | |
| $f_{PLL}$ | PLL output frequency | Phase Locked Loop | N/A | |
| $f_{DFLL}$ | DFLL output frequency | Digital Frequency Locked Loop | N/A | |
| $f_{RC80M}$ | RC80M output frequency | Internal 80MHz RC Oscillator | N/A | |

**Table 9-7.** ATSAM4L8 Current consumption and Wakeup time for power scaling mode 0 and 2

| Mode | Conditions | $T_A$ | Typical Wakeup Time | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|
| SLEEP0 | Switching mode | 25°C | 9 * Main clock cycles | 3817 | 4033 | µA |
| | | 85°C | | 4050 | 4507 | |
| SLEEP1 | Switching mode | 25°C | 9 * Main clock cycles + 500ns | 2341 | 2477 | |
| | | 85°C | | 2525 | 2832 | |
| SLEEP2 | Switching mode | 25°C | 9 * Main clock cycles + 500ns | 1758 | 1862 | |
| | | 85°C | | 1925 | 1971 | |
| SLEEP3 | Linear mode | 25°C | | 51 | 60 | |
| WAIT | OSC32K and AST running<br>Fast wake-up enable | | 1.5µs | 6.7 | | |
| | OSC32K and AST stopped<br>Fast wake-up enable | | | 5.5 | | |
| RETENTION | OSC32K running<br>AST running at 1kHz | | 1.5µs | 3.9 | | |
| | AST and OSC32K stopped | | | 3.0 | | |
| BACKUP | OSC32K running<br>AST running at 1kHz | | | 1.5 | 3.1 | |
| | AST and OSC32K stopped | | | 0.9 | 1.7 | |

1. These values are based on characterization. These values are not covered by test limits in production.

### 9.5.2 Power Scaling 1

The values in Table 34-7 are measured values of power consumption under the following conditions, except where noted:

- Operating conditions for power scaling mode 1
  - $V_{VDDIN}$ = 3.3V
- Wake up time from low power modes is measured from the edge of the wakeup signal to the first instruction fetched in flash.
- Oscillators
  - OSC0 (crystal oscillator) and OSC32K (32kHz crystal oscillator) stopped
  - RCFAST Running at 12MHz
- Clocks
  - RCFAST used as main clock source
  - CPU, AHB clocks undivided
  - APBC and APBD clocks divided by 4
  - APBA and APBB bridges off
  - The following peripheral clocks running
    - PM, SCIF, AST, FLASHCALW, APBC and APBD bridges

### 9.9.4 Analog- to Digital Converter Characteristics

**Table 9-45.** Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Temperature range | | -40 | | +85 | °C |
| | Resolution (1) | Max | | 12 | 12 (2) | Bit |
| | Sampling clock (3) | Differential modes, Gain=1X | 5 | | 300 | kHz |
| | | Unipolar modes, Gain=1X | 5 | | 250 | |
| $f_{ADC}$ | ADC clock frequency(3) | Differential modes | 0.03 | | 1.8 | MHz |
| | | Unipolar modes | 0.03 | | 1.5 | |
| $T_{SAMPLEHOLD}$ | Sampling time(3) | Differential modes | 16.5 | | 277 | µs |
| | | Unipolar modes | 16.5 | | 333 | |
| | Conversion rate(1) | 1X gain, differential | | | 300 | kSps |
| | Internal channel conversion rate(3) | $V_{VDD}$/10, Bandgap and Temperature channels | | | 125 | kSps |
| | Conversion time (latency) Differential mode (no windowing) | 1X gain, (resolution/2)+gain (4) | | | 6 | Cycles |
| | | 2X and 4X gain | | | 7 | |
| | | 8X and 16X gain | | | 8 | |
| | | 32X and 64X gain | | | 9 | |
| | | 64X gain and unipolar | | | 10 | |

1. These values are based on characterization. These values are not covered by test limits in production
2. Single ended or using divide by two max resolution: 11 bits
3. These values are based on simulation. These values are not covered by test limits in production
4. See Figure 9-5

**Figure 9-5.** Maximum input common mode voltage

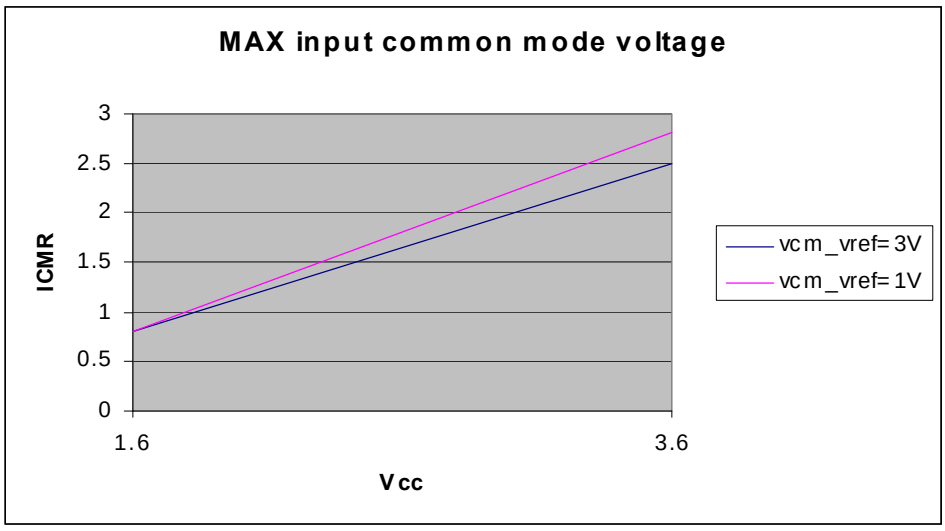


**Table 9-46.** DC Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| VDDANA | Supply voltage [1] | | 1.6 | | 3.6 | V |
| | Reference range [2] | Differential mode | 1.0 | | VDDANA -0.6 | V |
| | | Unipolar and Window modes | 1.0 | | 1.0 | |
| | | Using divide by two function (differential) | 2.0 | | VDDANA | |
| | Absolute min, max input voltage[2] | | -0,1 | | VDDANA +0.1 | V |
| | Start up time[2] | ADC with reference already enabled | | 12 | 24 | Cycles |
| | | No gain compensation Reference buffer | | | 5 | µs |
| | | Gain compensation Reference buffer | | | 60 | Cycles |
| $R_{SAMPLE}$ | Input channel source resistance[2] | | | | 0.5 | kΩ |
| $C_{SAMPLE}$ | Sampling capacitance[2] | | 2.9 | 3.6 | 4.3 | pF |
| | Reference input source resistance[2] | Gain compensation | | | 2 | kΩ |
| | | No gain compensation | | | 1 | MΩ |
| | ADC reference settling time[2] | After changing reference/mode [3] | | 5 | 60 | Cycles |

1. These values are based on characterization. These values are not covered by test limits in production
2. These values are based on simulation. These values are not covered by test limits in production
3. Requires refresh/flush otherwise conversion time (latency) + 1

**Table 9-47.** Differential mode, gain=1

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Accuracy without compensation [1] | | | 7 | | ENOB |
| | Accuracy after compensation[1] | (INL, gain and offset) | | | 11 | ENOB |
| INL | Integral Non Linearity [2] | After calibration, Gain compensation | | 1.2 | 1.7 | LSBs |
| DNL | Differential Non Linearity[2] | After calibration | | 0.7 | 1.0 | LSBs |
| | Gain error [2] | External reference | -5.0 | -1.0 | 5.0 | mV |
| | | VDDANA/1.6 | -40 | | 40 | |
| | | VDDANA/2.0 | -40 | | 40 | |
| | | Bandgap After calibration | -30 | | 30 | |
| | Gain error drift vs voltage[1] | External reference | -2 | | 2 | mV/V |
| | Gain error drift vs temperature[1] | After calibration + bandgap drift If using onchip bandgap | | | 0.08 | mV/°K |
| | Offset error [2] | External reference | -5.0 | | 5.0 | mV |
| | | VDDANA/1.6 | -10 | | 10 | |
| | | VDDANA/2.0 | -10 | | 10 | |
| | | Bandgap After calibration | -10 | | 10 | |
| | Offset error drift vs voltage[1] | | -4 | | 4 | mV/V |

**Table 9-47.** Differential mode, gain=1

| | | | | | | |
|---|---|---|---|---|---|---|
| | Offset error drift vs temperature[1] | | | | 0.04 | mV/°K |
| | Conversion range [2] | Vin-Vip | -Vref | | Vref | V |
| | ICMR[1] | | | see Figure 9-5 | | |
| | PSRR[1] | fvdd=1Hz, ext ADVREFP=3.0V $V_{VDD}$=3.6V | | 100 | | dB |
| | | fvdd=2MHz, ext ADVREFP=3.0V $V_{VDD}$=3.6 | | 50 | | |
| | DC supply current [2] | VDDANA=3.6V, ADVREFP=3.0V | | 1.2 | | mA |
| | | VDDANA=1.6V, ADVREFP=1.0V | | 0.6 | | |

1. These values are based on simulation only. These values are not covered by test limits in production or characterization
2. These values are based on characterization and not tested in production, and valid for an input voltage between 10% to 90% of reference voltage.

**Table 9-48.** Unipolar mode, gain=1

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Accuracy without compensation [1] | | | 7 | | ENOB |
| | Accuracy after compensation[1] | | | | 11 | ENOB |
| INL | Integral Non Linearity [2] | After calibration Dynamic tests No gain compensation | | | ±3 | LSBs |
| | | After calibration Dynamic tests Gain compensation | | | ±3 | |
| DNL | Differential Non Linearity[2] | After calibration | | | ±2.8 | LSBs |
| | Gain error[2] | External reference | -15 | | 15 | mV |
| | | VDDANA/1.6 | -50 | | 50 | |
| | | VDDANA/2.0 | -30 | | 30 | |
| | | Bandgap After calibration | -10 | | 10 | |
| | Gain error drift vs voltage[1] | External reference | -8 | | 8 | mV/V |
| | Gain error drift temperature[1] | + bandgap drift If using bandgap | | | 0.08 | mV/°K |
| | Offset error[2] | External reference | -15 | | 15 | mV |
| | | VDDANA/1.6 | -15 | | 15 | |
| | | VDDANA/2.0 | -15 | | 15 | |
| | | Bandgap After calibration | -10 | | 10 | |
| | Offset error drift[1] | | -4 | | 4 | mV/V |
| | Offset error drift temperature[1] | | | 0 | 0.04 | mV/°K |
| | Conversion range[1] | Vin-Vip | -Vref | | Vref | V |
| | ICMR[1] | | | see Figure 9-5 | | |

**Table 9-50.** Analog Comparator Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Hysteresis[1] | $V_{ACREFN}$ =0.1V to VDDIO-0.1V, hysteresis = 1[2] Fast mode | 10 | | 55 | mV |
| | | $V_{ACREFN}$ =0.1V to VDDIO-0.1V, hysteresis = 1[2] Low power mode | 10 | | 68 | mV |
| | | $V_{ACREFN}$ =0.1V to VDDIO-0.1V, hysteresis = 2[2] Fast mode | 26 | | 83 | mV |
| | | $V_{ACREFN}$ =0.1V to VDDIO-0.1V, hysteresis = 2[2] Low power mode | 19 | | 91 | mV |
| | | $V_{ACREFN}$ =0.1V to VDDIO-0.1V, hysteresis = 3[2] Fast mode | 43 | | 106 | mV |
| | | $V_{ACREFN}$ =0.1V to VDDIO-0.1V, hysteresis = 3[2] Low power mode | 32 | | 136 | mV |
| | Propagation delay[1] | Changes for $V_{ACM}$=VDDIO/2 100mV Overdrive Fast mode | | | 67 | ns |
| | | Changes for $V_{ACM}$=VDDIO/2 100mV Overdrive Low power mode | | | 315 | ns |
| $t_{STARTUP}$ | Startup time[1] | Enable to ready delay Fast mode | | | 1.19 | µs |
| | | Enable to ready delay Low power mode | | | 3.61 | µs |
| $I_{AC}$ | Channel current consumption [3] | Low power mode, no hysteresis | | 4.9 | 8.7 | µA |
| | | Fast mode, no hysteresis | | 63 | 127 | |

1. These values are based on characterization. These values are not covered by test limits in production
2. HYSTAC.CONFn.HYS field, refer to the Analog Comparator Interface chapter
3. These values are based on simulation. These values are not covered by test limits in production or characterization

**Table 9-65.** JTAG Timings[1]

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| JTAG0 | TCK Low Half-period | $V_{VDDIO}$ from 3.0V to 3.6V, maximum external capacitor = 40pF | 21.8 | | ns |
| JTAG1 | TCK High Half-period | | 8.6 | | |
| JTAG2 | TCK Period | | 30.3 | | |
| JTAG3 | TDI, TMS Setup before TCK High | | 2.0 | | |
| JTAG4 | TDI, TMS Hold after TCK High | | 2.3 | | |
| JTAG5 | TDO Hold Time | | 9.5 | | |
| JTAG6 | TCK Low to TDO Valid | | | 21.8 | |
| JTAG7 | Boundary Scan Inputs Setup Time | | 0.6 | | |
| JTAG8 | Boundary Scan Inputs Hold Time | | 6.9 | | |
| JTAG9 | Boundary Scan Outputs Hold Time | | 9.3 | | |
| JTAG10 | TCK to Boundary Scan Outputs Valid | | | 32.2 | |

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

### 9.10.6 SWD Timing

**Figure 9-18.** SWD Interface Signals

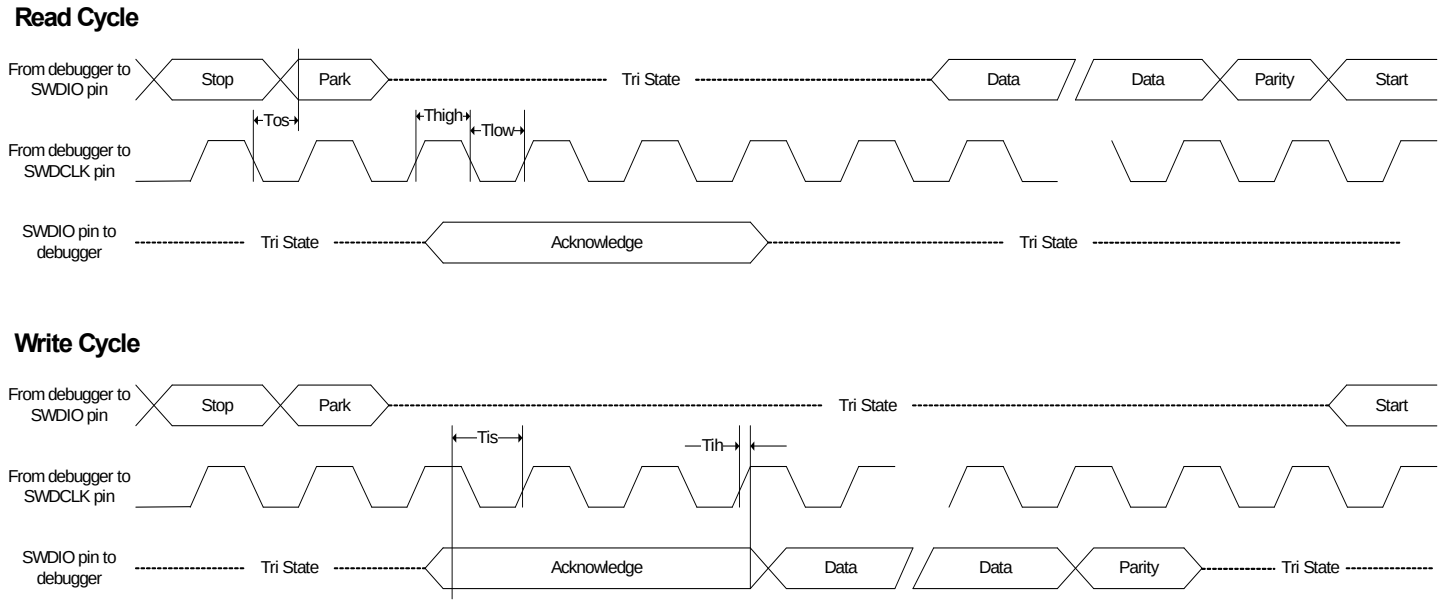


**Table 11-3.** ATSAM4LC2 Sub Serie Ordering Information

| Ordering Code | Flash (Kbytes) | RAM (Kbytes) | Package | Conditioning | Package Type | Temperature Operating Range |
|---|---|---|---|---|---|---|
| ATSAM4LC2CA-AU | 128 | 32 | TQFP100 | Tray | Green | Industrial -40°C to 85°C |
| ATSAM4LC2CA-AUR | | | | Reel | | |
| ATSAM4LC2CA-CFU | | | VFBGA100 | Tray | | |
| ATSAM4LC2CA-CFUR | | | | Reel | | |
| ATSAM4LC2BA-AU | | | TQFP64 | Tray | | |
| ATSAM4LC2BA-AUR | | | | Reel | | |
| ATSAM4LC2BA-MU | | | QFN64 | Tray | | |
| ATSAM4LC2BA-MUR | | | | Reel | | |
| ATSAM4LC2BA-UUR | | | WLCSP64 | Reel | | |
| ATSAM4LC2AA-AU | | | TQFP48 | Tray | | |
| ATSAM4LC2AA-AUR | | | | Reel | | |
| ATSAM4LC2AA-MU | | | QFN48 | Tray | | |
| ATSAM4LC2AA-MUR | | | | Reel | | |

**Table 11-4.** ATSAM4LS8 Sub Serie Ordering Information

| Ordering Code | Flash (Kbytes) | RAM (Kbytes) | Package | Conditioning | Package Type | Temperature Operating Range |
|---|---|---|---|---|---|---|
| ATSAM4LS8CA-AU | 512 | 64 | TQFP100 | Tray | Green | Industrial -40°C to 85°C |
| ATSAM4LS8CA-AUR | | | | Reel | | |
| ATSAM4LS8CA-CFU | | | VFBGA100 | Tray | | |
| ATSAM4LS8CA-CFUR | | | | Reel | | |
| ATSAM4LS8BA-AU | | | TQFP64 | Tray | | |
| ATSAM4LS8BA-AUR | | | | Reel | | |
| ATSAM4LS8BA-MU | | | QFN64 | Tray | | |
| ATSAM4LS8BA-MUR | | | | Reel | | |
| ATSAM4LS8BA-UUR | | | WLCSP64 | Reel | | |
| ATSAM4LS8AA-MU | | | QFN48 | Tray | | |
| ATSAM4LS8AA-MUR | | | | Reel | | |

### 12.1.7 FLASHCALW

**Corrupted data in flash may happen after flash page write operations.**
After a flash page write operation, reading (data read or code fetch) in flash may fail. This may lead to an expecption or to others errors derived from this corrupted read access.
**Fix/Workaround**
Before any flash page write operation, each 64-bit doublewords write in the page buffer must preceded by a 64-bit doublewords write in the page buffer with 0xFFFFFFFF_FFFFFFFF content at any address in the page. Note that special care is required when loading page buffer, refer to Section 2.5.9 ”Page Buffer Operations” on page 11.

## 13.5 Rev. E – 07/13

1. Added ATSAM4L8 derivatives and WLCSP packages for ATSAM4L4/2
2. Added operating conditions details in Electrical Characteristics Chapter
3. Fixed “Supply Rise Rates and Order”
4. Added number of USART available in sub-series
5. Fixed IO line considerations for USB pins
6. Removed useless information about CPU local bus which is not implemented
7. Removed useless information about Modem support which is not implemented
8. Added information about unsupported features in Power Scaling mode 1
9. Fixed SPI timings

## 13.6 Rev. F– 12/13

1. Fixed table 3-6 - TDI is connected to pin G3 in WLCSP package
2. Changed table 42-48 -ADCIFE Electricals in unipolar mode : PSRR & DC supply current typical values
3. Fixed SPI timing characteristics
4. Fixed BOD33 typical step size value

## 13.7 Rev. G– 03/14

1. Added WLCSP64 packages for SAM4LC8 and SAM4LS8 sub-series
2. Removed unsuppported SWAP feature in LCD module
3. Added mnimal value for ADC Reference range

## 13.8 Rev. H– 11/16

1. Fixed AESA configuration in Overview chapter for SAM4LS sub-series