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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	43
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 7x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atsam4lc2ba-mu

Table 3-2. 64-pin GPIO Controller Function Multiplexing (Sheet 3 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
QFP QFN	QFP QFN				A	B	C	D	E	F	G
	33	PA27	27	LCDA	SPI MISO	IISC ISCK	ABDACB DAC0	GLOC IN4	USART3 RTS		CATB SENSE0
	34	PA28	28	LCDA	SPI MOSI	IISC ISDI	ABDACB DACN0	GLOC IN5	USART3 CTS		CATB SENSE1
	35	PA29	29	LCDA	SPI SCK	IISC IWS	ABDACB DAC1	GLOC IN6	USART3 CLK		CATB SENSE2
	38	PA30	30	LCDA	SPI NPCS0	IISC ISDO	ABDACB DACN1	GLOC IN7	USART3 RXD		CATB SENSE3
	39	PA31	31	LCDA	SPI NPCS1	IISC IMCK	ABDACB CLK	GLOC OUT1	USART3 TXD		CATB DIS
11	11	PB00	32	VDDIN	TWIMS1 TWD	USART0 RXD					CATB SENSE21
12	12	PB01	33	VDDIN	TWIMS1 TWCK	USART0 TXD	EIC EXTINT0				CATB SENSE22
13	13	PB02	34	VDDANA	ADCIFE AD3	USART1 RTS	ABDACB DAC0	IISC ISCK	ACIFC ACBN0		CATB SENSE23
14	14	PB03	35	VDDANA	ADCIFE AD4	USART1 CLK	ABDACB DACN0	IISC ISDI	ACIFC ACBP0		CATB DIS
19	19	PB04	36	VDDANA	ADCIFE AD5	USART1 RXD	ABDACB DAC1	IISC ISDO	DACC EXT TRIG0		CATB SENSE24
20	20	PB05	37	VDDANA	ADCIFE AD6	USART1 TXD	ABDACB DACN1	IISC IMCK			CATB SENSE25
27	27	PB06	38	LCDA	USART3 RTS		GLOC IN4	IISC IWS		LCDCA SEG22	CATB SENSE26
28	28	PB07	39	LCDA	USART3 CTS		GLOC IN5	TC0 A0		LCDCA SEG21	CATB SENSE27
45	45	PB08	40	LCDA	USART3 CLK		GLOC IN6	TC0 B0		LCDCA SEG14	CATB SENSE28
46	46	PB09	41	LCDA	USART3 RXD	PEVC PAD EVT2	GLOC IN7	TC0 A1		LCDCA SEG15	CATB SENSE29
47	47	PB10	42	LCDA	USART3 TXD	PEVC PAD EVT3	GLOC OUT1	TC0 B1	SCIF GCLK0	LCDCA SEG16	CATB SENSE30
48	48	PB11	43	LCDA	USART0 CTS	SPI NPCS2		TC0 A2	SCIF GCLK1	LCDCA SEG17	CATB SENSE31
53	53	PB12	44	LCDC	USART0 RTS	SPI NPCS3	PEVC PAD EVT0	TC0 B2	SCIF GCLK2	LCDCA SEG32	CATB DIS
54	54	PB13	45	LCDC	USART0 CLK	SPI NPCS1	PEVC PAD EVT1	TC0 CLK0	SCIF GCLK3	LCDCA SEG33	CATB SENSE0
57	57	PB14	46	LCDC	USART0 RXD	SPI MISO	TWIM3 TWD	TC0 CLK1	SCIF GCLK IN0	LCDCA SEG36	CATB SENSE1
58	58	PB15	47	LCDC	USART0 TXD	SPI MOSI	TWIM3 TWCK	TC0 CLK2	SCIF GCLK IN1	LCDCA SEG37	CATB SENSE2

3.4.7 ADC Input Pins

These pins are regular I/O pins powered from the VDDANA.

sor core and NVIC provides fast execution of interrupt service routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to suspend load-multiple and store-multiple operations. Interrupt handlers do not require wrapping in assembler code, removing any code overhead from the ISRs. A tail-chain optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function enabling the entire device to be rapidly powered down while still retaining program state.

4.2 System level interface

The Cortex-M4 processor provides multiple interfaces using AMBA® technology to provide high speed, low latency memory accesses. It supports unaligned data accesses and implements atomic bit manipulation that enables faster peripheral controls, system spinlocks and thread-safe Boolean data handling.

The Cortex-M4 processor has an *memory protection unit* (MPU) that provides fine grain memory control, enabling applications to utilize multiple privilege levels, separating and protecting code, data and stack on a task-by-task basis. Such requirements are becoming critical in many embedded applications such as automotive.

4.3 Integrated configurable debug

The Cortex-M4 processor implements a complete hardware debug solution. This provides high system visibility of the processor and memory through either a traditional JTAG port or a 2-pin *Serial Wire Debug* (SWD) port that is ideal for microcontrollers and other small package devices.

For system trace the processor integrates an *Instrumentation Trace Macrocell* (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system events these generate, a *Serial Wire Viewer* (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

The *Flash Patch and Breakpoint Unit* (FPB) provides 8 hardware breakpoint comparators that debuggers can use. The comparators in the FPB also provide remap functions of up to 8 words in the program code in the CODE memory region. This enables applications stored on a non-erasable, ROM-based microcontroller to be patched if a small programmable memory, for example flash, is available in the device. During initialization, the application in ROM detects, from the programmable memory, whether a patch is required. If a patch is required, the application programs the FPB to remap a number of addresses. When those addresses are accessed, the accesses are redirected to a remap table specified in the FPB configuration, which means the program in the non-modifiable ROM can be patched.

A specific Peripheral Debug (PDBG) register is implemented in the Private Peripheral Bus address map. This register allows the user to configure the behavior of some modules in debug mode.

Figure 6-2. ATSAM4LC Power Domain Diagram

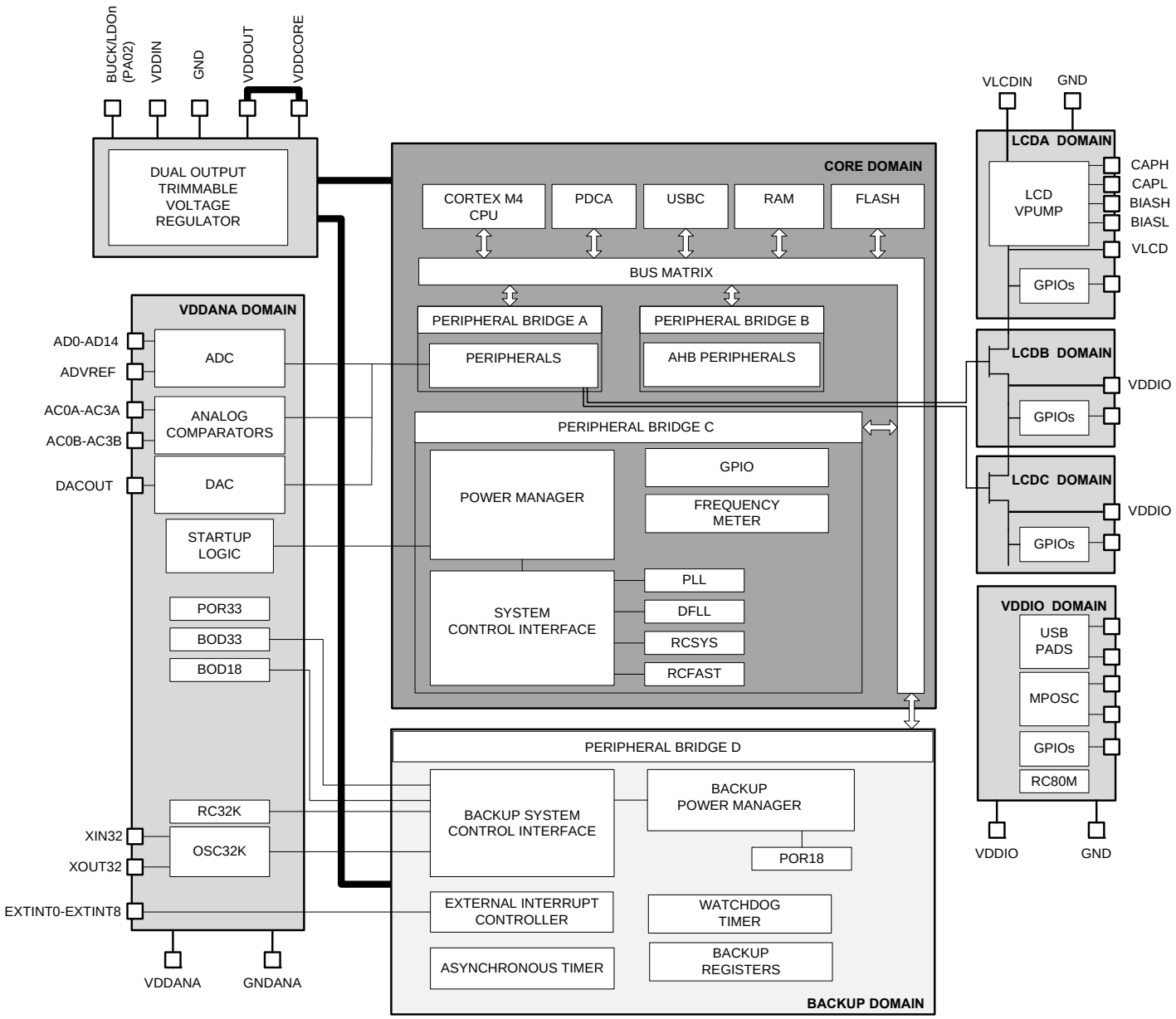
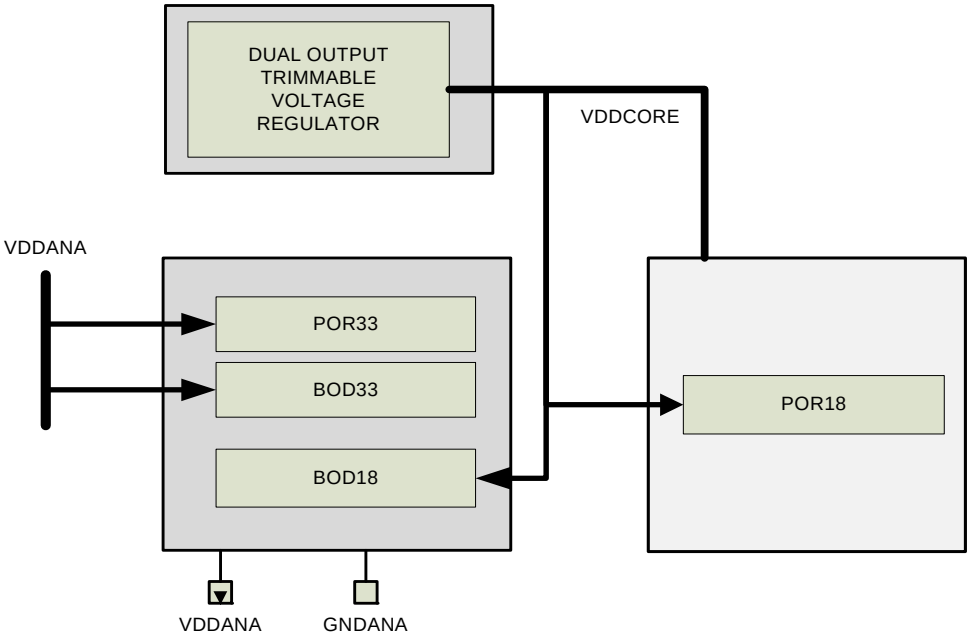


Figure 6-6. Supply Monitor Schematic



6.4.1 Power-on-Reset on VDDANA

POR33 monitors VDDANA. It is always activated and monitors voltage at startup but also during all the Power Save Mode. If VDDANA goes below the threshold voltage, the entire chip is reset.

6.4.2 Brownout Detector on VDDANA

BOD33 monitors VDDANA. Refer to Section 15. ”Backup System Control Interface (BSCIF)” on page 308to get more details.

6.4.3 Power-on-Reset on VDDCORE

POR18 monitors the internal VDDCORE. Refer to Section 15. ”Backup System Control Interface (BSCIF)” on page 308 to get more details.

6.4.4 Brownout Detector on VDDCORE

Once the device is startup, the BOD18 monitors the internal VDDCORE. Refer to Section 15. ”Backup System Control Interface (BSCIF)” on page 308 to get more details.

- Set the clock frequency to be supported in both power configurations.
- Set the high speed read mode of the FLASH to be supported in both power scaling configurations
  - Only relevant when entering or exiting BPM.PMCON.PS=2
- Configure the BPM.PMCON.PS field to the new power configuration.
- Set the BPM.PMCON.PSCREQ bit to one.
- Disable all the interrupts except the PM WCAUSE interrupt and enable only the PSOK asynchronous event in the AWEN register of PM.
- Execute the WFI instruction.
- WAIT for PM interrupt.

The new power configuration is reached when the system is waken up by the PM interrupt thanks to the PSOK event.

By default, all features are available in all Power Scaling modes. However some specific features are not available in PS1 (BPM.PMCON.PS=1) mode :

- USB
- DFLL
- PLL
- Programming/Erasing in Flash

8.9.11.1 Control Register

Name: CR

Access Type: Write-Only

Offset: 0x00

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	CE	FSPR	CRC	DIS	EN

Writing a zero to a bit in this register has no effect.

- **CE: Chip Erase**
  Writing a one to this bit triggers the FLASH Erase All (EA) operation which clears all volatile memories, the whole flash array, the general purpose fuses and the protected state. The Status register DONE field indicates the completion of the operation.
  Reading this bit always returns 0
- **FSPR: Flash User Page Read**
  Writing a one to this bit triggers a read operation in the User page. The word pointed by the ADDR register in the page is read and written to the DATA register. ADDR is post incremented allowing a burst of reads without modifying ADDR. SR.DONE must be read high prior to reading the DATA register.
  Reading this bit always returns 0
- **CRC: Cyclic Redundancy Code**
  Writing a one triggers a CRC calculation over a memory area defined by the ADDR and LENGTH registers. Reading this bit always returns 0
  Note: This feature is restricted while in protected state
- **DIS: Disable**
  Writing a one to this bit disables the module. Disabling the module resets the whole module immediately.
- **EN: Enable**
  Writing a one to this bit enables the module.

8.11.8 Chip erase typical procedure

The chip erase operation is triggered by writing a one in the CE bit in the Control Register (CR.CE). This clears first all volatile memories in the system and second the whole flash array. Note that the User page is not erased in this process. To ensure that the chip erase operation is completed, check the DONE bit in the Status Register (SR.DONE). Also note that the chip erase operation depends on clocks and power management features that can be altered by the CPU. It is important to ensure that it is stopped. The recommended sequence is shown below:

1. At power up, RESET_N is driven low by a debugger. The on-chip regulator holds the system in a POR state until the input supply is above the POR threshold. The system continues to be held in this static state until the internally regulated supplies have reached a safe operating.
2. PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock, and any Bus Clocks that do not have clock gate control). Internal resets are maintained due to the external reset.
   – The debug port and access ports receives a clock and leave the reset state
3. The debugger maintains a low level on TCK and release RESET_N.
   – The SMAP asserts the core_hold_reset signal
4. The Cortex-M4 core remains in reset state, meanwhile the rest of the system is released.
5. The Chip erase operation can be performed by issuing the SMAP Chip Erase command. In this case:
   – volatile memories are cleared first
   – followed by the clearing of the flash array
   – followed by the clearing of the protected state
6. After operation is completed, the chip must be restarted by either controling RESET_N or switching power off/on. Make sure that the TCK pin is high when releasing RESET_N not to halt the core.

8.11.9 Setting the protected state

This is done by issuing a specific flash controller command, for more information, refer to the Flash Controller chapter and to section 8.11.7Flash Programming typical procedure97. The protected state is defined by a highly secure Flash builtin mechanism. Note that for this programmation to propagate, it is required to reset the chip.

9.4 Maximum Clock Frequencies

Table 9-4. Maximum Clock Frequencies in Power Scaling Mode 0/2 and RUN Mode

Symbol	Parameter	Description	Max	Units
f_{CPU}	CPU clock frequency		48	MHz
f_{PBA}	PBA clock frequency		48	
f_{PBB}	PBB clock frequency		48	
f_{PBC}	PBC clock frequency		48	
f_{PBD}	PBD clock frequency		48	
f_{GCLK0}	GCLK0 clock frequency	DFLLIF main reference, GCLK0 pin	50	
f_{GCLK1}	GCLK1 clock frequency	DFLLIF dithering and SSG reference, GCLK1 pin	50	
f_{GCLK2}	GCLK2 clock frequency	AST, GCLK2 pin	20	
f_{GCLK3}	GCLK3 clock frequency	CATB, GCLK3 pin	50	
f_{GCLK4}	GCLK4 clock frequency	FLO and AESA	50	
f_{GCLK5}	GCLK5 clock frequency	GLOC, TC0 and RC32KIFB_REF	80	
f_{GCLK6}	GCLK6 clock frequency	ABDACB and IISC	50	
f_{GCLK7}	GCLK7 clock frequency	USBC	50	
f_{GCLK8}	GCLK8 clock frequency	TC1 and PEVC[0]	50	
f_{GCLK9}	GCLK9 clock frequency	PLL0 and PEVC[1]	50	
f_{GCLK10}	GCLK10 clock frequency	ADCIFE	50	
f_{GCLK11}	GCLK11 clock frequency	Master generic clock. Can be used as source for other generic clocks	150	
f_{OSC0}	OSC0 output frequency	Oscillator 0 in crystal mode	30	
		Oscillator 0 in digital clock mode	50	
f_{PLL}	PLL output frequency	Phase Locked Loop	240	
f_{DFLL}	DFLL output frequency	Digital Frequency Locked Loop	220	
f_{RC80M}	RC80M output frequency	Internal 80MHz RC Oscillator	80	

Table 9-11. Typical Current Consumption by Peripheral in Power Scaling Mode 0 and 2 (1)

Peripheral	Typ Consumption Active	Unit
IISC	1.0	µA/MHz
SPI	1.9	
TC	6.3	
TWIM	1.5	
TWIS	1.2	
USART	8.5	
ADCIFE(2)	3.1	
DACC	1.3	
ACIFC (2)	3.1	
GLOC	0.4	
ABDACB	0.7	
TRNG	0.9	
PARC	0.7	
CATB	3.0	
LCDCA	4.4	
PDCA	1.0	
CRCCU	0.3	
USBC	1.5	
PEVC	5.6	
CHIPID	0.1	
SCIF	6.4	
FREQM	0.5	
GPIO	7.1	
BPM	0.9	
BSCIF	4.6	
AST	1.5	
WDT	1.4	
EIC	0.6	
PICOUART	0.3	

1. These numbers are valid for the measured condition only and must not be extrapolated to other frequencies
2. Includes the current consumption on VDDANA and ADVREFP.

9.5.4 .Peripheral Power Consumption in Power Scaling mode 1

The values in Table 9-13 are measured values of power consumption under the following conditions:

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-35. Flash Endurance and Data Retention [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{FARRAY}	Array endurance (write/page)	f_{CLK_AHB} > 10MHz	100k			cycles
N_{FFUSE}	General Purpose fuses endurance (write/bit)	f_{CLK_AHB} > 10MHz	10k			
t_{RET}	Data retention		15			years

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.9 Analog Characteristics

9.9.1 Voltage Regulator Characteristics

Table 9-36. VREG Electrical Characteristics in Linear and Switching Modes

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	DC output current (1) Power scaling mode 0 & 2	Low power mode (WAIT)	2000	3600	5600	µA
		Ultra Low power mode (RETENTION)	100	180	300	
	DC output current(1) Power scaling mode 1	Low power mode (WAIT)	4000	7000	10000	
		Ultra Low power mode (RETENTION)	200	350	600	
$V_{VDDCORE}$	DC output voltage	All modes			1.9	V

1. These values are based on simulation. These values are not covered by test limits in production.

Table 9-37. VREG Electrical Characteristics in Linear mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VDDIN}	Input voltage range	I_{OUT}=10mA	1.68		3.6	V
		I_{OUT}=50mA	1.8		3.6	
$V_{VDDCORE}$	DC output voltage (1) Power scaling mode 0 & 2	I_{OUT} = 0 mA	1.777	1.814	1.854	
		I_{OUT} = 50 mA	1.75	1.79	1.83	
I_{OUT}	DC output current(1)	$V_{VDDCORE}$ > 1.65V			100	mA
	Output DC load regulation(1) Transient load regulation	I_{OUT} = 0 to 80mA, V_{VDDIN} = 3V	-34	-27	-19	mV
	Output DC regulation(1)	I_{OUT} = 80 mA, V_{VDDIN} = 2V to 3.6V	10	28	48	mV
I_Q	Quescient current(1)	I_{OUT} = 0 mA RUN and SLEEPx modes	88	107	128	µA

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-38. External components requirements in Linear Mode

Symbol	Parameter	Technology	Typ	Units
C_{IN1}	Input regulator capacitor 1		33	nF
C_{IN2}	Input regulator capacitor 2		100	
C_{IN3}	Input regulator capacitor 3		10	µF
C_{OUT1}	Output regulator capacitor 1		100	nF
C_{OUT2}	Output regulator capacitor 2	Tantalum or MLCC 0.5<ESR<10Ω	4.7	µF

Table 9-39. VREG Electrical Characteristics in Switching mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VDDIN}	Input voltage range	$V_{VDDCORE}$ = 1.65V, I_{OUT}=50mA	2.0		3.6	V
$V_{VDDCORE}$	DC output voltage (1) Power scaling mode 0 & 2	I_{OUT} = 0 mA	1.75	1.82	1.87	
		I_{OUT} = 50 mA	1.66	1.71	1.79	

Table 9-39. VREG Electrical Characteristics in Switching mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	DC output current(1)	$V_{VDDCORE}$ > 1.65V			55	mA
	Output DC load regulation(1) Transient load regulation	I_{OUT} = 0 to 50mA, V_{VDDIN} = 3V	-136	-101	-82	mV
	Output DC regulation(1)	I_{OUT} = 50 mA, V_{VDDIN} = 2V to 3.6V	-20	38	99	mV
I_Q	Quescient current(1)	V_{VDDIN} = 2V, I_{OUT} = 0 mA	97	186	546	µA
		V_{VDDIN} > 2.2V, I_{OUT} = 0 mA	97	111	147	
P_{EFF}	Power efficiency(1)	I_{OUT} = 5mA, 50mA Reference power not included	82.7	88.3	95	%

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-40. Decoupling Requirements in Switching Mode

Symbol	Parameter	Technology	Typ	Units
C_{IN1}	Input regulator capacitor 1		33	nF
C_{IN2}	Input regulator capacitor 2		100	
C_{IN3}	Input regulator capacitor 3		10	µF
C_{OUT1}	Output regulator capacitor 1	X7R MLCC	100	nF
C_{OUT2}	Output regulator capacitor 2	X7R MLCC (ex : GRM31CR71A475)	4.7	µF
L_{EXT}	External inductance	(ex: Murata LQH3NPN220MJ0)	22	µH
R_{DCLEXT}	Serial resistance of L_{EXT}		0.7	Ω
$ISAT_{LEXT}$	Saturation current of L_{EXT}		300	mA

Note: 1. Refer to Section 6. on page 46.

Table 9-47. Differential mode, gain=1

	Offset error drift vs temperature[1]				0.04	mV/°K
	Conversion range [2]	Vin-Vip	-Vref		Vref	V
	ICMR[1]			see Figure 9-5		
	PSRR[1]	fvdd=1Hz, ext ADVREFP=3.0V V_{VDD}=3.6V		100		dB
		fvdd=2MHz, ext ADVREFP=3.0V V_{VDD}=3.6		50		
	DC supply current [2]	VDDANA=3.6V, ADVREFP=3.0V		1.2		mA
		VDDANA=1.6V, ADVREFP=1.0V		0.6		

1. These values are based on simulation only. These values are not covered by test limits in production or characterization
2. These values are based on characterization and not tested in production, and valid for an input voltage between 10% to 90% of reference voltage.

Table 9-48. Unipolar mode, gain=1

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Accuracy without compensation [1]			7		ENOB
	Accuracy after compensation[1]				11	ENOB
INL	Integral Non Linearity [2]	After calibration Dynamic tests No gain compensation			±3	LSBs
		After calibration Dynamic tests Gain compensation			±3	
DNL	Differential Non Linearity[2]	After calibration			±2.8	LSBs
	Gain error[2]	External reference	-15		15	mV
		VDDANA/1.6	-50		50	
		VDDANA/2.0	-30		30	
		Bandgap After calibration	-10		10	
	Gain error drift vs voltage[1]	External reference	-8		8	mV/V
	Gain error drift temperature[1]	+ bandgap drift If using bandgap			0.08	mV/°K
	Offset error[2]	External reference	-15		15	mV
		VDDANA/1.6	-15		15	
		VDDANA/2.0	-15		15	
		Bandgap After calibration	-10		10	
	Offset error drift[1]		-4		4	mV/V
	Offset error drift temperature[1]			0	0.04	mV/°K
	Conversion range[1]	Vin-Vip	-Vref		Vref	V
	ICMR[1]			see Figure 9-5		

9.10 Timing Characteristics

9.10.1 RESET_N Timing

Table 9-53. RESET_N Waveform Parameters [1]

Symbol	Parameter	Conditions	Min	Max	Units
t_{RESET}	RESET_N minimum pulse length		10		ns

1. These values are based on simulation. These values are not covered by test limits in production.

9.10.2 USART in SPI Mode Timing

9.10.2.1 Master mode

Figure 9-7. USART in SPI Master Mode with (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

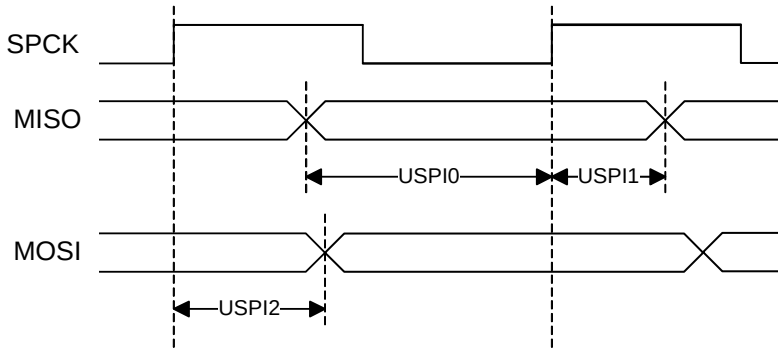


Figure 9-8. USART in SPI Master Mode with (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

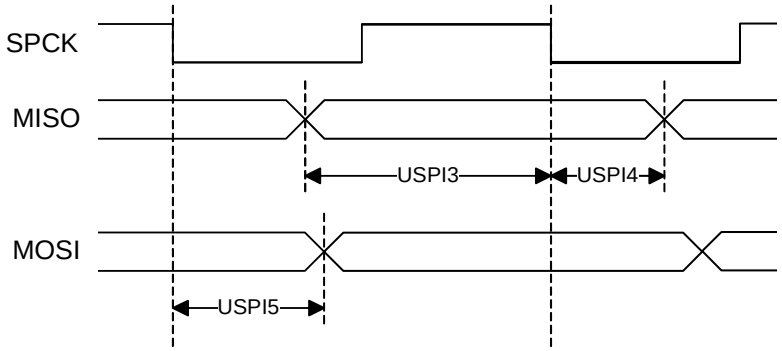


Table 9-59. USART1 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		373.58	ns
USPI7	MOSI setup time before SPCK rises		4.16 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		46.69 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			373.54	
USPI10	MOSI setup time before SPCK falls		4.16 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		46.69 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		200.43		
USPI13	NSS hold time after SPCK falls		-16.5		
USPI14	NSS setup time before SPCK falls		200.43		
USPI15	NSS hold time after SPCK rises		-16.5		

Table 9-60. USART2 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		770.02	ns
USPI7	MOSI setup time before SPCK rises		136.56 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		47.9 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			570.19	
USPI10	MOSI setup time before SPCK falls		136.73 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		47.9 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		519.87		
USPI13	NSS hold time after SPCK falls		-1.83		
USPI14	NSS setup time before SPCK falls		519.87		
USPI15	NSS hold time after SPCK rises		-1.83		

Table 9-61. USART3 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		593.9	ns
USPI7	MOSI setup time before SPCK rises		45.93 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		47.03 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			593.38	
USPI10	MOSI setup time before SPCK falls		45.93 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		47.03 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		237.5		
USPI13	NSS hold time after SPCK falls		-1.81		
USPI14	NSS setup time before SPCK falls		237.5		
USPI15	NSS hold time after SPCK rises		-1.81		

Notes: 1. These values are based on simulation. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left(\left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor + \frac{1}{2}\right) \times t_{CLKUSART}$

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, USPI7 + USPI8 or USPI10 + USPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

Where $SPIn$ is the MISO delay, USPI6 or USPI9 depending on CPOL and NCPHA. T_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for T_{SETUP} . f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

Figure 9-16. SPI Slave Mode, NPCS Timing

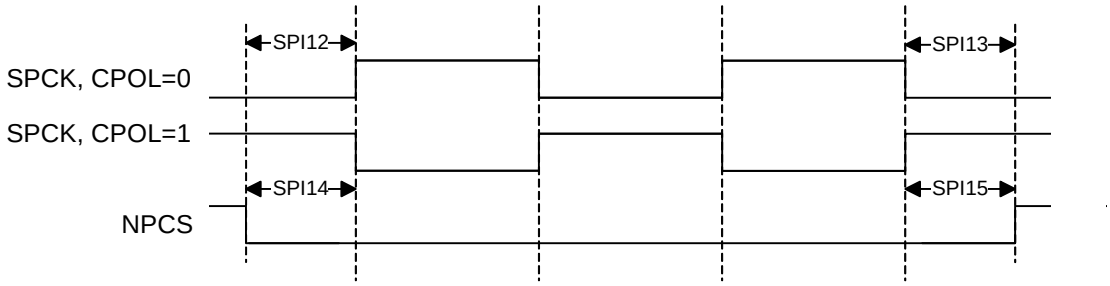


Table 9-63. SPI Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
SPI6	SPCK falling to MISO delay	V_{VDDIO} from 2.85V to 3.6V, maximum external capacitor = 40pF	19	47	ns
SPI7	MOSI setup time before SPCK rises		0		
SPI8	MOSI hold time after SPCK rises		5.4		
SPI9	SPCK rising to MISO delay		19	46	
SPI10	MOSI setup time before SPCK falls		0		
SPI11	MOSI hold time after SPCK falls		5.3		
SPI12	NPCS setup time before SPCK rises		4		
SPI13	NPCS hold time after SPCK falls		2.5		
SPI14	NPCS setup time before SPCK falls		6		
SPI15	NPCS hold time after SPCK rises		1.1		

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{CLKSPI}, \frac{1}{SPIn})$$

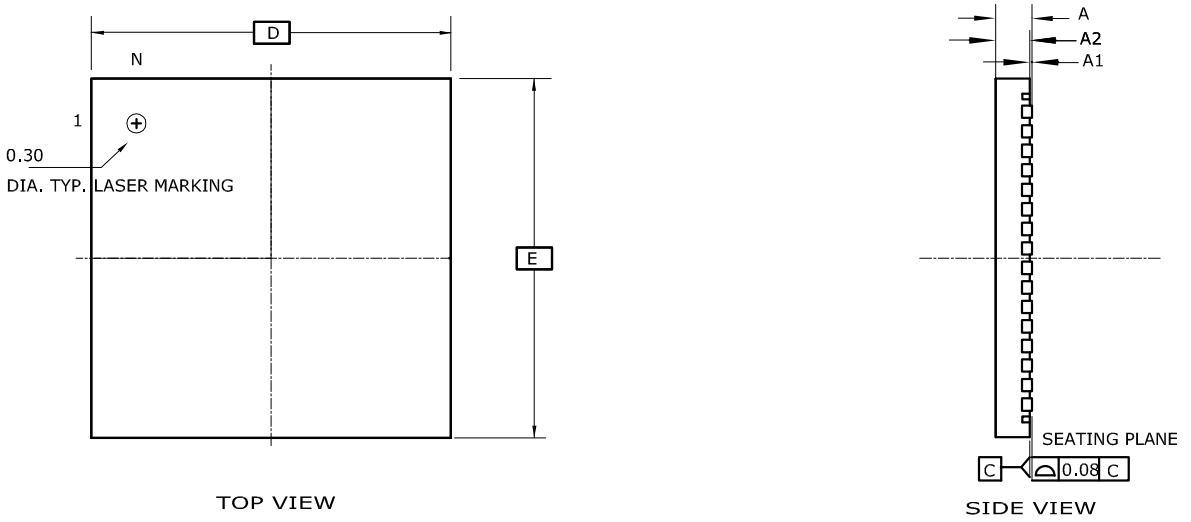
Where $SPIn$ is the MOSI setup and hold time, SPI7 + SPI8 or SPI10 + SPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

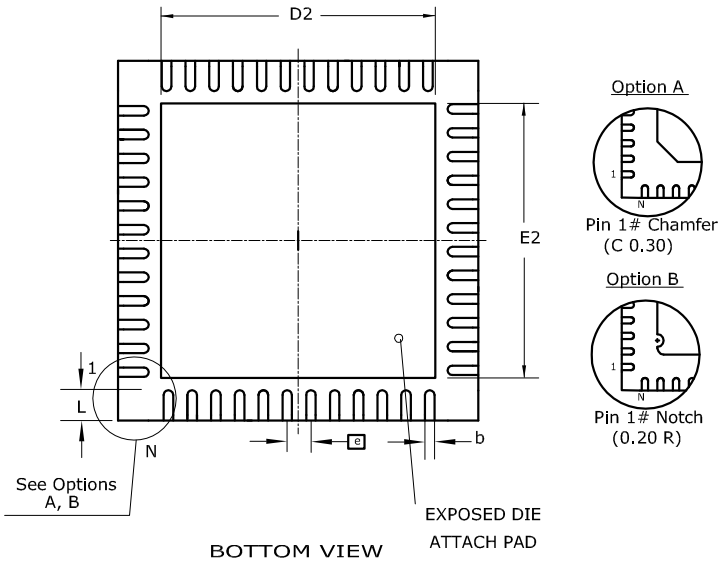
Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

Figure 10-11. QFN-48 Package Drawing for ATSAM4LC8 and ATSAM4LS8





COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A2	0.75	-----	1.00	
D/E		7 BSC		
D2/E2	5.50	5.60	5.70	
L	0.30	0.40	0.50	
b	0.17	-----	0.30	2
e		0.50 BSC		
n		48		

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 10-32. Device and Package Maximum Weight

140	mg

Table 10-33. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-34. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

Table 11-5. ATSAM4LS4 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LS4CA-AU-ES	256	32	TQFP100	ES	Green	N/A
ATSAM4LS4CA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LS4CA-AUR				Reel		
ATSAM4LS4CA-CFU			VFBGA100	Tray		Industrial -40°C to 85°C
ATSAM4LS4CA-CFUR				Reel		
ATSAM4LS4BA-AU-ES			TQFP64	ES		N/A
ATSAM4LS4BA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LS4BA-AUR				Reel		
ATSAM4LS4BA-MU-ES			QFN64	ES		N/A
ATSAM4LS4BA-MU				Tray		Industrial -40°C to 85°C
ATSAM4LS4BA-MUR				Reel		
ATSAM4LS4BA-UUR			WLCSP64	Reel		Industrial -40°C to 85°C
ATSAM4LS4AA-AU-ES			TQFP48	ES		N/A
ATSAM4LS4AA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LS4AA-AUR				Reel		
ATSAM4LS4AA-MU-ES			QFN48	ES		N/A
ATSAM4LS4AA-MU				Tray		Industrial -40°C to 85°C
ATSAM4LS4AA-MUR				Reel		

Table 11-6. ATSAM4LS2 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LS2CA-AU	128	32	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS2CA-AUR				Reel		
ATSAM4LS2CA-CFU			VFBGA100	Tray		
ATSAM4LS2CA-CFUR				Reel		
ATSAM4LS2BA-AU			TQFP64	Tray		
ATSAM4LS2BA-AUR				Reel		
ATSAM4LS2BA-MU			QFN64	Tray		
ATSAM4LS2BA-MUR				Reel		
ATSAM4LS2BA-UUR			WLCSP64	Reel		
ATSAM4LS2AA-AU			TQFP48	Tray		
ATSAM4LS2AA-AUR				Reel		
ATSAM4LS2AA-MU			QFN48	Tray		
ATSAM4LS2AA-MUR				Reel		