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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4lc2ca-au

events, even in sleep modes where the module clock is stopped. Power monitoring is supported by on-chip Power-on Reset (POR18, POR33), Brown-out Detectors (BOD18, BOD33). The device features several oscillators, such as Phase Locked Loop (PLL), Digital Frequency Locked Loop (DFLL), Oscillator 0 (OSC0), Internal RC 4,8,12MHz oscillator (RCFAST), system RC oscillator (RCSYS), Internal RC 80MHz, Internal 32kHz RC and 32kHz Crystal Oscillator. Either of these oscillators can be used as source for the system clock. The DFLL is a programmable internal oscillator from 40 to 150MHz. It can be tuned to a high accuracy if an accurate reference clock is running, e.g. the 32kHz crystal oscillator.

The Watchdog Timer (WDT) will reset the device unless it is periodically serviced by the software. This allows the device to recover from a condition that has caused the system to be unstable.

The Asynchronous Timer (AST) combined with the 32kHz crystal oscillator supports powerful real-time clock capabilities, with a maximum timeout of up to 136 years. The AST can operate in counter or calendar mode.

The Frequency Meter (FREQM) allows accurate measuring of a clock frequency by comparing it to a known reference clock.

The Full-speed USB 2.0 device and embedded host interface (USBC) supports several USB classes at the same time utilizing the rich end-point configuration.

The device includes six identical 16-bit Timer/Counter (TC) channels. Each channel can be independently programmed to perform frequency measurement, event counting, interval measurement, pulse generation, delay timing, and pulse width modulation.

The ATSAM4L8/L4/L2 also features many communication interfaces, like USART, SPI, or TWI, for communication intensive applications. The USART supports different communication modes, like SPI Mode and LIN Mode.

A general purpose 16-channel ADC is provided, as well as four analog comparators (ACIFC). The ADC can operate in 12-bit mode at full speed. The analog comparators can be paired to detect when the sensing voltage is within or outside the defined reference window.

Atmel offers the QTouch Library for embedding capacitive touch buttons, sliders, and wheels functionality. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys as well as Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop, and debug your own touch applications.

The Audio Bitstream DAC (ABDACB) converts a 16-bit sample value to a digital bitstream with an average value proportional to the sample value. Two channels are supported, making the ABDAC particularly suitable for stereo audio.

The Inter-IC Sound Controller (IISC) provides a 5-bit wide, bidirectional, synchronous, digital audio link with external audio devices. The controller is compliant with the Inter-IC Sound (I2S) bus specification.

Figure 3-2. ATSAM4LC VFBGA100 Pinout

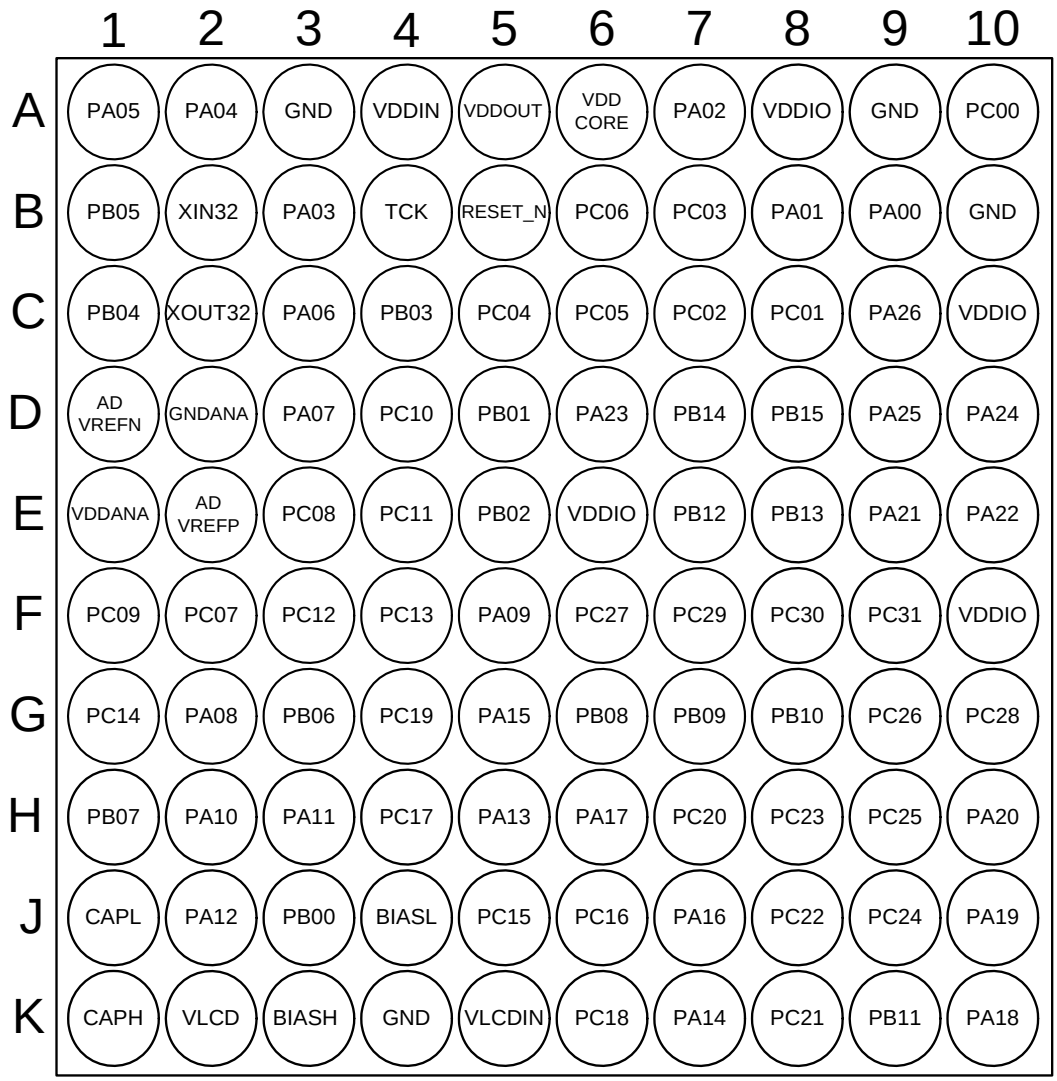


Table 3-1. 100-pin GPIO Controller Function Multiplexing (Sheet 4 of 4)

ATSAM4LC		ATSAM4LS		Pin	GPIO	Supply	GPIO Functions						
QFN	VFBGA	QFN	VFBGA				A	B	C	D	E	F	G
59	J6	59	J6	PC16	80	LCDA	TC1 B0			GLOC IN5		LCDCA SEG1	CATB SENSE17
60	H4	60	H4	PC17	81	LCDA	TC1 A1			GLOC IN6		LCDCA SEG2	CATB SENSE18
61	K6	61	K6	PC18	82	LCDA	TC1 B1			GLOC IN7		LCDCA SEG3	CATB SENSE19
62	G4	62	G4	PC19	83	LCDA	TC1 A2			GLOC OUT1		LCDCA SEG4	CATB SENSE20
68	H7	68	H7	PC20	84	LCDA	TC1 B2					LCDCA SEG10	CATB SENSE21
69	K8	69	K8	PC21	85	LCDA	TC1 CLK0			PARC PCCK		LCDCA SEG11	CATB SENSE22
70	J8	70	J8	PC22	86	LCDA	TC1 CLK1			PARC PCEN1		LCDCA SEG12	CATB SENSE23
71	H8	71	H8	PC23	87	LCDA	TC1 CLK2			PARC PCEN2		LCDCA SEG13	CATB DIS
79	J9	79	J9	PC24	88	LCDB	USART1 RTS	EIC EXTINT1	PEVC PAD EVT0	PARC PCDATA0		LCDCA SEG24	CATB SENSE24
80	H9	80	H9	PC25	89	LCDB	USART1 CLK	EIC EXTINT2	PEVC PAD EVT1	PARC PCDATA1		LCDCA SEG25	CATB SENSE25
81	G9	81	G9	PC26	90	LCDB	USART1 RXD	EIC EXTINT3	PEVC PAD EVT2	PARC PCDATA2	SCIF GCLK0	LCDCA SEG26	CATB SENSE26
82	F6	82	F6	PC27	91	LCDB	USART1 TXD	EIC EXTINT4	PEVC PAD EVT3	PARC PCDATA3	SCIF GCLK1	LCDCA SEG27	CATB SENSE27
83	G10	83	G10	PC28	92	LCDB	USART3 RXD	SPI MISO	GLOC IN4	PARC PCDATA4	SCIF GCLK2	LCDCA SEG28	CATB SENSE28
84	F7	84	F7	PC29	93	LCDB	USART3 TXD	SPI MOSI	GLOC IN5	PARC PCDATA5	SCIF GCLK3	LCDCA SEG29	CATB SENSE29
85	F8	85	F8	PC30	94	LCDB	USART3 RTS	SPI SCK	GLOC IN6	PARC PCDATA6	SCIF GCLK IN0	LCDCA SEG30	CATB SENSE30
86	F9	86	F9	PC31	95	LCDB	USART3 CLK	SPI NPCS0	GLOC OUT1	PARC PCDATA7	SCIF GCLK IN1	LCDCA SEG31	CATB SENSE31

Table 3-2. 64-pin GPIO Controller Function Multiplexing (Sheet 1 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
QFP QFN	QFP QFN				A	B	C	D	E	F	G
1	1	PA00	0	VDDIO							
2	2	PA01	1	VDDIO							
3	3	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
10	10	PA03	3	VDDIN		SPI MISO					

Table 3-3. 64-pin GPIO Controller Function Multiplexing for WLCSP package (Sheet 3 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
WLCSP	WLCSP				A	B	C	D	E	F	G
E5	E5	PB13	45	LCDC	USART0 CLK	SPI NPCS1	PEVC PAD EVT1	TC0 CLK0	SCIF GCLK3	LCDCA SEG33	CATB SENSE0
F4	F4	PB14	46	LCDC	USART0 RXD	SPI MISO	TWIM3 TWD	TC0 CLK1	SCIF GCLK IN0	LCDCA SEG36	CATB SENSE1
H4	H4	PB15	47	LCDC	USART0 TXD	SPI MOSI	TWIM3 TWCK	TC0 CLK2	SCIF GCLK IN1	LCDCA SEG37	CATB SENSE2

3.3 Signals Description

The following table gives details on signal names classified by peripheral.

Table 3-8. Signal Descriptions List (Sheet 1 of 4)

Signal Name	Function	Type	Active Level	Comments
Audio Bitstream DAC - ABDACB				
CLK	D/A clock output	Output		
DAC1 - DAC0	D/A bitstream outputs	Output		
DACN1 - DACN0	D/A inverted bitstream outputs	Output		
Analog Comparator Interface - ACIFC				
ACAN1 - ACAN0	Analog Comparator A negative references	Analog		
ACAP1 - ACAP0	Analog Comparator A positive references	Analog		
ACBN1 - ACBN0	Analog Comparator B negative references	Analog		
ACBP1 - ACBP0	Analog Comparator B positive references	Analog		
ADC controller interface - ADCIFE				
AD14 - AD0	Analog inputs	Analog		
ADVREFP	Positive voltage reference	Analog		
TRIGGER	External trigger	Input		
Backup System Control Interface - BSCIF				
XIN32	32 kHz Crystal Oscillator Input	Analog/ Digital		
XOUT32	32 kHz Crystal Oscillator Output	Analog		
Capacitive Touch Module B - CATB				
DIS	Capacitive discharge line	Output		
SENSE31 - SENSE0	Capacitive sense lines	I/O		
DAC Controller - DACC				
DAC external trigger	DAC external trigger	Input		
DAC voltage output	DAC voltage output	Analog		
Enhanced Debug Port For ARM Products - EDP				
TCK/SWCLK	JTAG / SW Debug Clock	Input		
TDI	JTAG Debug Data In	Input		
TDO/TRACESWO	JTAG Debug Data Out / SW Trace Out	Output		
TMS/SWDIO	JTAG Debug Mode Select / SW Data	I/O		
External Interrupt Controller - EIC				
EXTINT8 - EXTINT0	External interrupts	Input		
Glue Logic Controller - GLOC				
IN7 - IN0	Lookup Tables Inputs	Input		
OUT1 - OUT0	Lookup Tables Outputs	Output		

6.2.4 Power-up Sequence

6.2.4.1 Maximum Rise Rate

To avoid risk of latch-up, the rise rate of the power supplies must not exceed the values described in Table 9-3 on page 100.

6.2.4.2 Minimum Rise Rate

The integrated Power-on Reset (POR33) circuitry monitoring the VDDIN powering supply requires a minimum rise rate for the VDDIN power supply.

See Table 9-3 on page 100 for the minimum rise rate value.

If the application can not ensure that the minimum rise rate condition for the VDDIN power supply is met, the following configuration can be used:

- A logic “0” value is applied during power-up on pin RESET_N until VDDIN rises above 1.6 V.

6.3 Startup Considerations

This section summarizes the boot sequence of the ATSAM4L8/L4/L2. The behavior after power-up is controlled by the Power Manager. For specific details, refer to Section 9. ”Power Manager (PM)” on page 677.

6.3.1 Starting of Clocks

After power-up, the device will be held in a reset state by the power-up circuitry for a short time to allow the power to stabilize throughout the device. After reset, the device will use the System RC Oscillator (RCSYS) as clock source. Refer to Section 9. ”Electrical Characteristics” on page 99 for the frequency for this oscillator.

On system start-up, the DFLL and the PLLs are disabled. Only the necessary clocks are active allowing software execution. Refer to Section 3-6 ”Maskable Module Clocks in AT32UC3B.” on page 24 to know the list of peripheral clock running.. No clocks have a divided frequency; all parts of the system receive a clock with the same frequency as the System RC Oscillator.

6.3.2 Fetching of Initial Instructions

After reset has been released, the Cortex M4 CPU starts fetching PC and SP values from the reset address, which is 0x00000000. Refer to the ARM Architecture Reference Manual for more information on CPU startup. This address points to the first address in the internal Flash.

The code read from the internal flash is free to configure the clock system and clock sources.

6.4 Power-on-Reset, Brownout and Supply Monitor

The SAM4L embeds four features to monitor, warm, and/or reset the device:

- POR33: Power-on-Reset on VDDANA
- BOD33: Brownout detector on VDDANA
- POR18: Power-on-Reset on VDDCORE
- BOD18: Brownout detector on VDDCORE

7.1.3 BACKUP Mode

The BACKUP mode allows achieving the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time.

The Core domain is powered-off. The internal SRAM and register contents of the Core domain are lost. The Backup domain is kept powered-on. The 32kHz clock (RC32K or OSC32K) is kept running if enabled to feed modules that require clocking.

In BACKUP mode, the configuration of the I/O lines is preserved. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677 to have more details.

7.1.3.1 Entering BACKUP Mode

The Backup mode is entered by using the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 1.

7.1.3.2 Exiting BACKUP Mode

Exit from BACKUP mode happens if a reset occurs or if an enabled wake up event occurs.

The reset sources are:

- BOD33 reset
- BOD18 reset
- WDT reset
- External reset in RESET_N pin

The wake up sources are:

- EIC lines (level transition only)
- BOD33 interrupt
- BOD18 interrupt
- AST alarm, periodic, overflow
- WDT interrupt

The RC32K or OSC32K should be used as clock source for modules if required. The PMCON.CK32S is used to select one of these two 32kHz clock sources.

Exiting the BACKUP mode is triggered by:

- a reset source: an internal reset sequence is performed according to the reset source. Once VDDCORE is stable and has the correct value according to RUN0 mode, the internal reset is released and program execution starts. The corresponding reset source is flagged in the Reset Cause register (RCAUSE) of the PM.
- a wake up source: the Backup domain is not reset. An internal reset is generated to the Core domain, and the system switches back to the previous RUN mode. Once VDDCORE is stable and has the correct value, the internal reset in the Core domain is released and program execution starts. The BKUP bit is set in the Reset Cause register (RCAUSE) of the PM. It allows the user to discriminate between the reset cause and a wake up cause from the BACKUP mode. The wake up cause can be found in the Backup Wake up Cause register (BPM.BKUPWCAUSE).

7.1.5 Power Save Mode Summary Table

The following table shows a summary of the main Power Save modes:

Table 7-2. Power Save mode Configuration Summary

Mode	Mode Entry	Wake up sources	Core domain	Backup domain
SLEEP	WFI SCR.SLEEPDEEP bit = 0 BPM.PMCON.BKUP bit = 0	Any interrupt	CPU clock OFF Other clocks OFF depending on the BPM.PMCON.SLEEP field see "SLEEP mode" on page 56	Clocks OFF depending on the BPM.PMCON.SLEEP field see "SLEEP mode" on page 56
WAIT	WFI SCR.SLEEPDEEP bit = 1 BPM.PMCON.RET bit = 0 BPM.PMCON.BKUP bit = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running
RETENTION	WFI SCR.SLEEPDEEP bit = 1 BPM.PMCON.RET bit = 1 BPM.PMCON.BKUP bit = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running
BACKUP	WFI + SCR.SLEEPDEEP bit = 1 + BPM.PMCON.BKUP bit = 1	EIC interrupt BOD33, BOD18 interrupt and reset AST alarm, periodic, overflow WDT interrupt and reset external reset on RESET_N pin	OFF (not powered)	All clocks are OFF except RC32K or OSC32K if running

7.2 Power Scaling

The Power Scaling technique consists of adjusting the internal regulator output voltage (voltage scaling) to reduce the power consumption. According to the requirements in terms of performance, operating modes, and current consumption, the user can select the Power Scaling configuration that fits the best with its application.

The Power Scaling configuration field (PMCON.PS) is provided in the Backup Power Manager (BPM) module.

In RUN mode, the user can adjust on the fly the Power Scaling configuration

The Figure 7.1 summarizes the different combination of the Power Scaling configuration which can be applied according to the Power Save Mode.

Power scaling from a current power configuration to a new power configuration is done by halting the CPU execution

Power scaling occurs after a WFI instruction. The system is halted until the new power configuration is stabilized. After handling the PM interrupt, the system resumes from WFI.

To scale the power, the following sequence is required:

- Check the BPM.SR.PSOK bit to make sure the current power configuration is stabilized.

8.7.5 Product Dependencies

8.7.5.1 I/O Lines

The TCK pin is dedicated to the EDP. The other debug port pins default after reset to their GPIO functionality and are automatically reassigned to the JTAG functionalities on detection of a debugger. In serial wire mode, TDI and TDO can be used as GPIO functions. Note that in serial wire mode TDO can be used as a single pin trace output.

8.7.5.2 Power Management

When a debugger is present, the connection is kept alive allowing debug operations. As a side effect, the power is never turned off. The hot plugging functionality is always available except when the system is in BACKUP Power Save Mode.

8.7.5.3 Clocks

The SWJ-DP uses the external TCK pin as its clock source. This clock must be provided by the external JTAG master device.

Some of the JTAG Instructions are used to access an Access Port (SMAP or AHB-AP). These instructions require the CPU clock to be running.

If the CPU clock is not present because the CPU is in a Power Save Mode where this clock is not provided, the Power Manager(PM) will automatically restore the CPU clock on detection of a debug access.

The RCSYS clock is used as CPU clock when the external reset is applied to ensure correct Access Port operations.

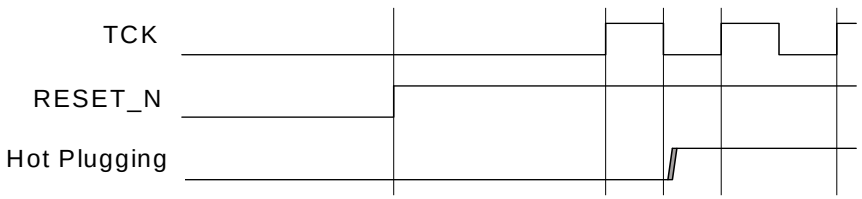
8.7.6 Module Initialization

This module is enabled as soon as a TCK falling edge is detected when RESET_N is not asserted (refer to Section 8.7.7 below). Moreover, the module is synchronously reseted as long as the TAP machine is in the TEST_LOGIC_RESET (TLR) state. It is advised asserting TMS at least 5 TCK clock periods after the debugger has been detected to ensure the module is in the TLR state prior to any operation. This module also has the ability to maintain the Cortex-M4 under reset (refer to the Section 8.7.8 ”SMAP Core Reset Request Source” on page 70).

8.7.7 Debugger Hot Plugging

The TCK pin is dedicated to the EDP. After reset has been released, the EDP detects that a debugger has been attached when a TCK falling edge arises.

Figure 8-4. Debugger Hot Plugging Detection Timings Diagram



8.7.12 JTAG Instructions Summary

The implemented JTAG instructions are shown in the table below.

Table 8-2. Implemented JTAG instructions list

IR instruction value	Instruction	Description	availability when protected	Component
b0000	EXTEST	Select boundary-scan chain as data register for testing circuitry external to the device.	yes	BSCAN-TAP
b0001	SAMPLE_PRELOAD	Take a snapshot of external pin values without affecting system operation.	yes	
b0100	INTEST	Select boundary-scan chain for internal testing of the device.	yes	
b0101	CLAMP	Bypass device through Bypass register, while driving outputs from boundary-scan register.	yes	
b1000	ABORT	ARM JTAG-DP Instruction	yes	SWJ-DP (in JTAG mode)
b1010	DPACC	ARM JTAG-DP Instruction	yes	
b1011	APACC	ARM JTAG-DP Instruction	yes	
b1100	-	Reserved	yes	
b1101	-	Reserved	yes	
b1110	IDCODE	ARM JTAG-DP Instruction	yes	
b1111	BYPASS	Bypass this device through the bypass register.	yes	

8.9 System Manager Access Port (SMAP)

Rev.: 1.0.0.0

8.9.1 Features

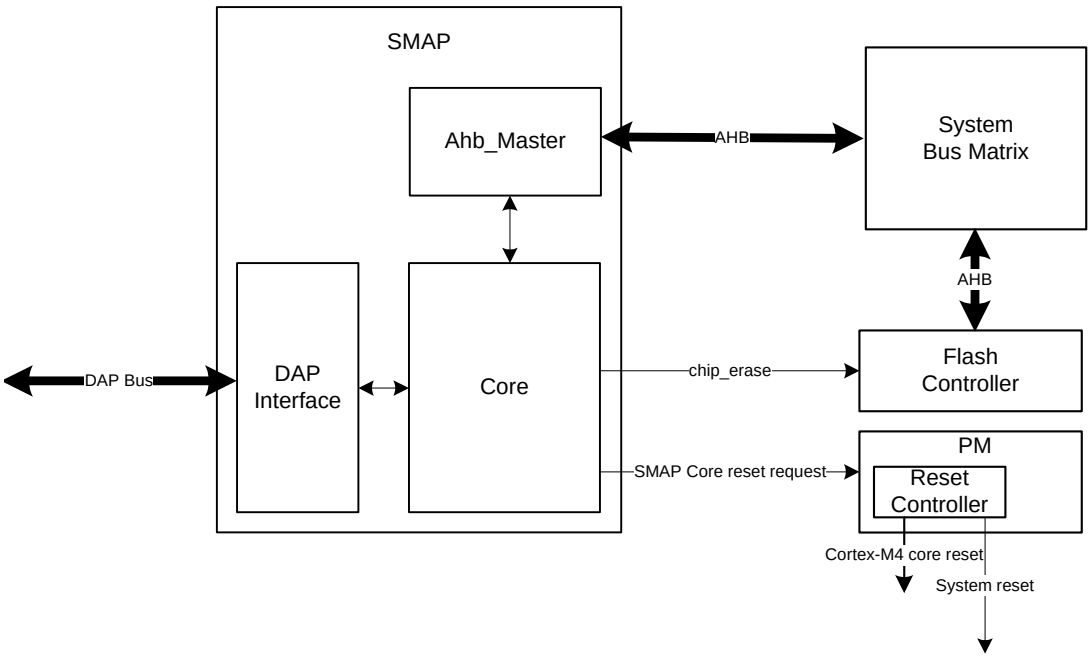
- **Chip Erase command and status**
- **Cortex-M4 core reset source**
- **32-bit Cyclic Redundancy check of any memory accessible through the bus matrix**
- **Unlimited Flash User page read access**
- **Chip identification register**

8.9.2 Overview

The SMAP provides memory-related services and also Cortex-M4 core reset control to a debugger through the Debug Port. This makes possible to halt the CPU and program the device after reset.

8.9.3 Block Diagram

Figure 8-7. SMAP Block Diagram



8.9.4 Initializing the Module

The SMAP can be accessed only if the CPU clock is running and the SWJ-DP has been activated by issuing a CDBGPWRUP request. For more details, refer to the ARM Debug Interface v5.1 Architecture Specification.

Then it must be enabled by writing a one to the EN bit of the CR register (CR.EN) before writing or reading other registers. If the SMAP is not enabled it will discard any read or write operation.

8.9.5 Stopping the Module

To stop the module, the user must write a one to the DIS bit of the CR register (CR.DIS). All the user interface and internal registers will be cleared and the internal clock will be stopped.

8.9.11.1 Control Register

Name: CR

Access Type: Write-Only

Offset: 0x00

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	CE	FSPR	CRC	DIS	EN

Writing a zero to a bit in this register has no effect.

- **CE: Chip Erase**
  Writing a one to this bit triggers the FLASH Erase All (EA) operation which clears all volatile memories, the whole flash array, the general purpose fuses and the protected state. The Status register DONE field indicates the completion of the operation.
  Reading this bit always returns 0
- **FSPR: Flash User Page Read**
  Writing a one to this bit triggers a read operation in the User page. The word pointed by the ADDR register in the page is read and written to the DATA register. ADDR is post incremented allowing a burst of reads without modifying ADDR. SR.DONE must be read high prior to reading the DATA register.
  Reading this bit always returns 0
- **CRC: Cyclic Redundancy Code**
  Writing a one triggers a CRC calculation over a memory area defined by the ADDR and LENGTH registers. Reading this bit always returns 0
  Note: This feature is restricted while in protected state
- **DIS: Disable**
  Writing a one to this bit disables the module. Disabling the module resets the whole module immediately.
- **EN: Enable**
  Writing a one to this bit enables the module.

instruction for the first time. SAMPLE/PRELOAD can also be used for taking a snapshot of the external pins during normal operation of the part.

When using the JTAG interface for Boundary-Scan, the JTAG TCK clock is independent of the internal chip clock, which is not required to run.

NOTE: For pins connected to 5V lines care should be taken to not drive the pins to a logic one using boundary scan, as this will create a current flowing from the 3,3V driver to the 5V pullup on the line. Optionally a series resistor can be added between the line and the pin to reduce the current.

8.11.7 Flash Programming typical procedure

Flash programming is performed by operating Flash controller commands. The Flash controller is connected to the system bus matrix and is then controllable from the AHP-AP. The AHB-AP cannot write the FLASH page buffer while the core_hold_reset is asserted. The AHB-AP cannot be accessed when the device is in protected state. It is important to ensure that the CPU is halted prior to operating any flash programming operation to prevent it from corrupting the system configuration. The recommended sequence is shown below:

1. At power up, RESET_N is driven low by a debugger. The on-chip regulator holds the system in a POR state until the input supply is above the POR threshold. The system continues to be held in this static state until the internally regulated supplies have reached a safe operating.
2. PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock, and any Bus Clocks that do not have clock gate control). Internal resets are maintained due to the external reset.
   – The Debug Port (DP) and Access Ports (AP) receives a clock and leave the reset state,
3. The debugger maintains a low level on TCK and release RESET_N.
   – The SMAP asserts the core_hold_reset signal
4. The Cortex-M4 core remains in reset state, meanwhile the rest of the system is released.
5. The debugger then configures the NVIC to catch the Cortex-M4 core reset vector fetch. For more information on how to program the NVIC, refer to the ARMv7-M Architecture Reference Manual.
6. The debugger writes a one in the SMAP SCR.HCR to release the Cortex-M4 core reset to make the system bus matrix accessible from the AHB-AP.
7. The Cortex-M4 core initializes the SP, then read the exception vector and stalls
8. Programming is available through the AHB-AP
9. After operation is completed, the chip can be restarted either by asserting RESET_N or switching power off/on or clearing SCR.HCR. Make sure that the TCK pin is high when releasing RESET_N not to halt the core.

8.11.8 Chip erase typical procedure

The chip erase operation is triggered by writing a one in the CE bit in the Control Register (CR.CE). This clears first all volatile memories in the system and second the whole flash array. Note that the User page is not erased in this process. To ensure that the chip erase operation is completed, check the DONE bit in the Status Register (SR.DONE). Also note that the chip erase operation depends on clocks and power management features that can be altered by the CPU. It is important to ensure that it is stopped. The recommended sequence is shown below:

1. At power up, RESET_N is driven low by a debugger. The on-chip regulator holds the system in a POR state until the input supply is above the POR threshold. The system continues to be held in this static state until the internally regulated supplies have reached a safe operating.
2. PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock, and any Bus Clocks that do not have clock gate control). Internal resets are maintained due to the external reset.
   – The debug port and access ports receives a clock and leave the reset state
3. The debugger maintains a low level on TCK and release RESET_N.
   – The SMAP asserts the core_hold_reset signal
4. The Cortex-M4 core remains in reset state, meanwhile the rest of the system is released.
5. The Chip erase operation can be performed by issuing the SMAP Chip Erase command. In this case:
   – volatile memories are cleared first
   – followed by the clearing of the flash array
   – followed by the clearing of the protected state
6. After operation is completed, the chip must be restarted by either controling RESET_N or switching power off/on. Make sure that the TCK pin is high when releasing RESET_N not to halt the core.

8.11.9 Setting the protected state

This is done by issuing a specific flash controller command, for more information, refer to the Flash Controller chapter and to section 8.11.7Flash Programming typical procedure97. The protected state is defined by a highly secure Flash builtin mechanism. Note that for this programmation to propagate, it is required to reset the chip.

Table 9-11. Typical Current Consumption by Peripheral in Power Scaling Mode 0 and 2 (1)

Peripheral	Typ Consumption Active	Unit
IISC	1.0	µA/MHz
SPI	1.9	
TC	6.3	
TWIM	1.5	
TWIS	1.2	
USART	8.5	
ADCIFE(2)	3.1	
DACC	1.3	
ACIFC (2)	3.1	
GLOC	0.4	
ABDACB	0.7	
TRNG	0.9	
PARC	0.7	
CATB	3.0	
LCDCA	4.4	
PDCA	1.0	
CRCCU	0.3	
USBC	1.5	
PEVC	5.6	
CHIPID	0.1	
SCIF	6.4	
FREQM	0.5	
GPIO	7.1	
BPM	0.9	
BSCIF	4.6	
AST	1.5	
WDT	1.4	
EIC	0.6	
PICOUART	0.3	

1. These numbers are valid for the measured condition only and must not be extrapolated to other frequencies
2. Includes the current consumption on VDDANA and ADVREFP.

9.5.4 .Peripheral Power Consumption in Power Scaling mode 1

The values in Table 9-13 are measured values of power consumption under the following conditions:

9.9.4 Analog- to Digital Converter Characteristics

Table 9-45. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Temperature range		-40		+85	°C
	Resolution (1)	Max		12	12 (2)	Bit
	Sampling clock (3)	Differential modes, Gain=1X	5		300	kHz
		Unipolar modes, Gain=1X	5		250	
f_{ADC}	ADC clock frequency(3)	Differential modes	0.03		1.8	MHz
		Unipolar modes	0.03		1.5	
$T_{SAMPLEHOLD}$	Sampling time(3)	Differential modes	16.5		277	µs
		Unipolar modes	16.5		333	
	Conversion rate(1)	1X gain, differential			300	kSps
	Internal channel conversion rate(3)	V_{VDD}/10, Bandgap and Temperature channels			125	kSps
	Conversion time (latency) Differential mode (no windowing)	1X gain, (resolution/2)+gain (4)			6	Cycles
		2X and 4X gain			7	
		8X and 16X gain			8	
		32X and 64X gain			9	
		64X gain and unipolar			10	

1. These values are based on characterization. These values are not covered by test limits in production
2. Single ended or using divide by two max resolution: 11 bits
3. These values are based on simulation. These values are not covered by test limits in production
4. See Figure 9-5

Figure 9-5. Maximum input common mode voltage

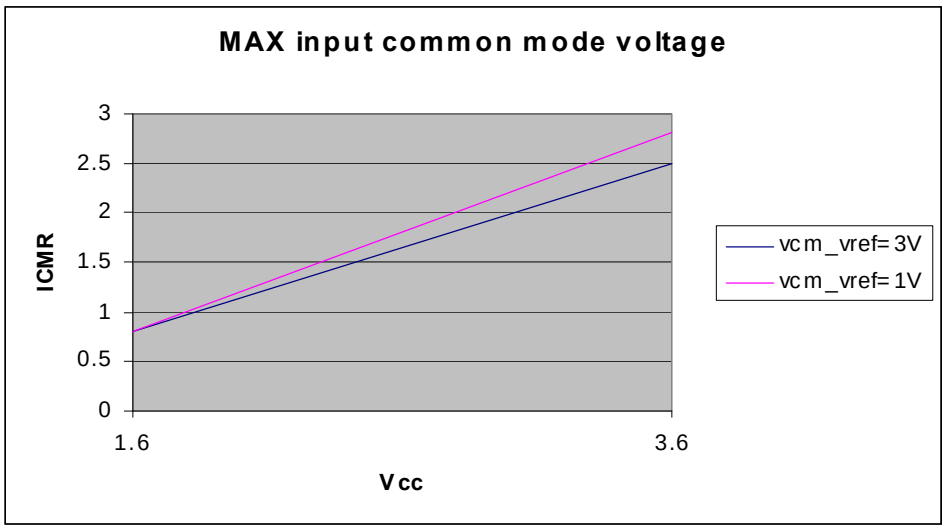


Table 9-50. Analog Comparator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Hysteresis[1]	V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 1[2] Fast mode	10		55	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 1[2] Low power mode	10		68	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 2[2] Fast mode	26		83	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 2[2] Low power mode	19		91	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 3[2] Fast mode	43		106	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 3[2] Low power mode	32		136	mV
	Propagation delay[1]	Changes for V_{ACM}=VDDIO/2 100mV Overdrive Fast mode			67	ns
		Changes for V_{ACM}=VDDIO/2 100mV Overdrive Low power mode			315	ns
$t_{STARTUP}$	Startup time[1]	Enable to ready delay Fast mode			1.19	µs
		Enable to ready delay Low power mode			3.61	µs
I_{AC}	Channel current consumption [3]	Low power mode, no hysteresis		4.9	8.7	µA
		Fast mode, no hysteresis		63	127	

1. These values are based on characterization. These values are not covered by test limits in production
2. HYSTAC.CONFn.HYS field, refer to the Analog Comparator Interface chapter
3. These values are based on simulation. These values are not covered by test limits in production or characterization

Figure 9-16. SPI Slave Mode, NPCS Timing

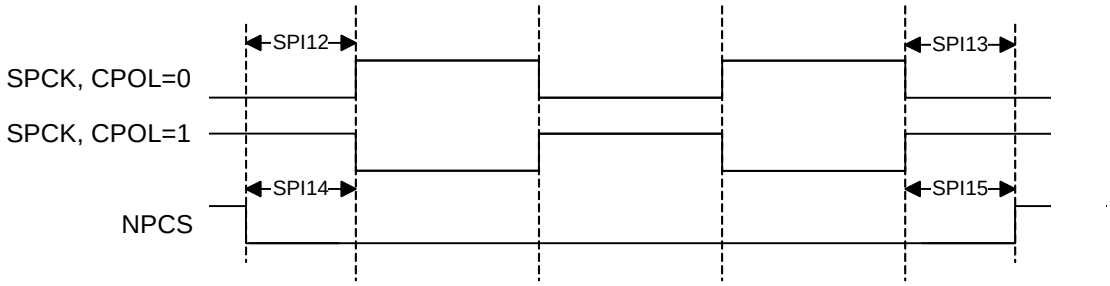


Table 9-63. SPI Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
SPI6	SPCK falling to MISO delay	V_{VDDIO} from 2.85V to 3.6V, maximum external capacitor = 40pF	19	47	ns
SPI7	MOSI setup time before SPCK rises		0		
SPI8	MOSI hold time after SPCK rises		5.4		
SPI9	SPCK rising to MISO delay		19	46	
SPI10	MOSI setup time before SPCK falls		0		
SPI11	MOSI hold time after SPCK falls		5.3		
SPI12	NPCS setup time before SPCK rises		4		
SPI13	NPCS hold time after SPCK falls		2.5		
SPI14	NPCS setup time before SPCK falls		6		
SPI15	NPCS hold time after SPCK rises		1.1		

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{CLKSPI}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, SPI7 + SPI8 or SPI10 + SPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

12. Errata

12.1 ATSAM4L4 /2 Rev. B & ATSAM4L8 Rev. A

12.1.1 General

PS2 mode is not supported by Engineering Samples
PS2 mode support is supported only by parts with calibration version higher than 0.
Fix/Workaround
The calibration version can be checked by reading a 32-bit word at address 0x0080020C. The calibration version bitfield is 4-bit wide and located from bit 4 to bit 7 in this word. Any value higher than 0 ensures that the part supports the PS2 mode

12.1.2 SCIF

PLLCOUNT value larger than zero can cause PLLEN glitch
Initializing the PLLCOUNT with a value greater than zero creates a glitch on the PLLEN signal during asynchronous wake up.
Fix/Workaround
The lock-masking mechanism for the PLL should not be used.
The PLLCOUNT field of the PLL Control Register should always be written to zero.

12.1.3 WDT

WDT Control Register does not have synchronization feedback
When writing to the Timeout Prescale Select (PSEL), Time Ban Prescale Select (TBAN), Enable (EN), or WDT Mode (MODE) fieldss of the WDT Control Register (CTRL), a synchronizer is started to propagate the values to the WDT clcok domain. This synchronization takes a finite amount of time, but only the status of the synchronization of the EN bit is reflected back to the user. Writing to the synchronized fields during synchronization can lead to undefined behavior.
Fix/Workaround
-When writing to the affected fields, the user must ensure a wait corresponding to 2 clock cycles of both the WDT peripheral bus clock and the selected WDT clock source.
-When doing writes that changes the EN bit, the EN bit can be read back until it reflects the written value.

12.1.4 SPI

SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0
When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
Fix/Workaround
Disable mode fault detection by writing a one to MR.MODFDIS.

SPI disable does not work in SLAVE mode
SPI disable does not work in SLAVE mode.

13. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

13.1 Rev. A – 09/12

1. Initial revision.

13.2 Rev. B – 10/12

1. Fixed ordering code
2. Changed BOD18CTRL and BOD33CTRL ACTION field from “Reserved” to ‘No action”

13.3 Rev. C – 02/13

1. Fixed ball pitch for VFBGA100 package
2. Added VFBGA100 and WLCSP64 pinouts
3. Added Power Scaling Mode 2 for high frequency support
4. Minor update on several modules chapters
5. Major update on Electrical characteristics
6. Updated errata
7. Fixed GPIO multiplexing pin numbers

13.4 Rev. D – 03/13

1. Removed WLCSP package information
2. Added errata text for detecting whether a part supports PS2 mode or not
3. Removed temperature sensor feature (not supported by production flow)
4. Fixed MUX selection on Positive ADC input channel table
5. Added information about TWI instances capabilities
6. Added some details on errata Corrupted data in flash may happen after flash page write operations.171