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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 27 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.68V ~ 3.6V |
| Data Converters | A/D 3x12b; D/A 1x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/atmel/atsam4lc4aa-au |

**Table 3-2.** 64-pin GPIO Controller Function Multiplexing (Sheet 2 of 3)

| ATSAM4LC | ATSAM4LS | Pin | GPIO | Supply | GPIO Functions | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| QFP QFN | QFP QFN | | | | A | B | C | D | E | F | G |
| 15 | 15 | PA04 | 4 | VDDANA | ADCIFE AD0 | USART0 CLK | EIC EXTINT2 | GLOC IN1 | | | CATB SENSE0 |
| 16 | 16 | PA05 | 5 | VDDANA | ADCIFE AD1 | USART0 RXD | EIC EXTINT3 | GLOC IN2 | ADCIFE TRIGGER | | CATB SENSE1 |
| 21 | 21 | PA06 | 6 | VDDANA | DACC VOUT | USART0 RTS | EIC EXTINT1 | GLOC IN0 | ACIFC ACAN0 | | CATB SENSE2 |
| 22 | 22 | PA07 | 7 | VDDANA | ADCIFE AD2 | USART0 TXD | EIC EXTINT4 | GLOC IN3 | ACIFC ACAP0 | | CATB SENSE3 |
| 26 | 26 | PA08 | 8 | LCDA | USART0 RTS | TC0 A0 | PEVC PAD EVT0 | GLOC OUT0 | | LCDCA SEG23 | CATB SENSE4 |
| 29 | 29 | PA09 | 9 | LCDA | USART0 CTS | TC0 B0 | PEVC PAD EVT1 | PARC PCDATA0 | | LCDCA COM3 | CATB SENSE5 |
| 30 | 30 | PA10 | 10 | LCDA | USART0 CLK | TC0 A1 | PEVC PAD EVT2 | PARC PCDATA1 | | LCDCA COM2 | CATB SENSE6 |
| 31 | 31 | PA11 | 11 | LCDA | USART0 RXD | TC0 B1 | PEVC PAD EVT3 | PARC PCDATA2 | | LCDCA COM1 | CATB SENSE7 |
| 32 | 32 | PA12 | 12 | LCDA | USART0 TXD | TC0 A2 | | PARC PCDATA3 | | LCDCA COM0 | CATB DIS |
| 40 | 40 | PA13 | 13 | LCDA | USART1 RTS | TC0 B2 | SPI NPCS1 | PARC PCDATA4 | | LCDCA SEG5 | CATB SENSE8 |
| 41 | 41 | PA14 | 14 | LCDA | USART1 CLK | TC0 CLK0 | SPI NPCS2 | PARC PCDATA5 | | LCDCA SEG6 | CATB SENSE9 |
| 42 | 42 | PA15 | 15 | LCDA | USART1 RXD | TC0 CLK1 | SPI NPCS3 | PARC PCDATA6 | | LCDCA SEG7 | CATB SENSE10 |
| 43 | 43 | PA16 | 16 | LCDA | USART1 TXD | TC0 CLK2 | EIC EXTINT1 | PARC PCDATA7 | | LCDCA SEG8 | CATB SENSE11 |
| 44 | 44 | PA17 | 17 | LCDA | USART2 RTS | ABDACB DAC0 | EIC EXTINT2 | PARC PCCK | | LCDCA SEG9 | CATB SENSE12 |
| 49 | 49 | PA18 | 18 | LCDA | USART2 CLK | ABDACB DACN0 | EIC EXTINT3 | PARC PCEN1 | | LCDCA SEG18 | CATB SENSE13 |
| 50 | 50 | PA19 | 19 | LCDA | USART2 RXD | ABDACB DAC1 | EIC EXTINT4 | PARC PCEN2 | SCIF GCLK0 | LCDCA SEG19 | CATB SENSE14 |
| 51 | 51 | PA20 | 20 | LCDA | USART2 TXD | ABDACB DACN1 | EIC EXTINT5 | GLOC IN0 | SCIF GCLK1 | LCDCA SEG20 | CATB SENSE15 |
| 55 | 55 | PA21 | 21 | LCDC | SPI MISO | USART1 CTS | EIC EXTINT6 | GLOC IN1 | TWIM2 TWD | LCDCA SEG34 | CATB SENSE16 |
| 56 | 56 | PA22 | 22 | LCDC | SPI MOSI | USART2 CTS | EIC EXTINT7 | GLOC IN2 | TWIM2 TWCK | LCDCA SEG35 | CATB SENSE17 |
| 59 | 59 | PA23 | 23 | LCDC | SPI SCK | TWIMS0 TWD | EIC EXTINT8 | GLOC IN3 | SCIF GCLK IN0 | LCDCA SEG38 | CATB DIS |
| 60 | 60 | PA24 | 24 | LCDC | SPI NPCS0 | TWIMS0 TWCK | | GLOC OUT0 | SCIF GCLK IN1 | LCDCA SEG39 | CATB SENSE18 |
| 62 | 62 | PA25 | 25 | VDDIO | USBC DM | USART2 RXD | | | | | CATB SENSE19 |
| 63 | 63 | PA26 | 26 | VDDIO | USBC DP | USART2 TXD | | | | | CATB SENSE20 |

**Table 3-8.** Signal Descriptions List (Sheet 4 of 4)

| Signal Name | Function | Type | Active Level | Comments |
|---|---|---|---|---|
| PA31 - PA00 | Parallel I/O Controller I/O Port A | I/O | | |
| PB15 - PB00 | Parallel I/O Controller I/O Port B | I/O | | |
| PC31 - PC00 | Parallel I/O Controller I/O Port C | I/O | | |

Note: 1. See "Power and Startup Considerations" section.

## 3.4 I/O Line Considerations

### 3.4.1 SW/JTAG Pins

The JTAG pins switch to the JTAG functions if a rising edge is detected on TCK low after the RESET_N pin has been released. The TMS, and TDI pins have pull-up resistors when used as JTAG pins. The TCK pin always has pull-up enabled during reset. The JTAG pins can be used as GPIO pins and multiplexed with peripherals when the JTAG is disabled. Refer to Section 3.2.3 "JTAG Port Connections" on page 29 for the JTAG port connections.

For more details, refer to Section 1.1 "Enhanced Debug Port (EDP)" on page 3.

### 3.4.2 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIN. As the product integrates a power-on reset detector, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

### 3.4.3 TWI Pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and-inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as GPIO pins.

### 3.4.4 GPIO Pins

All the I/O lines integrate a pull-up/pull-down resistor and slew rate controller. Programming these features is performed independently for each I/O line through the GPIO Controllers. After reset, I/O lines default as inputs with pull-up and pull-down resistors disabled and slew rate enabled.

### 3.4.5 High-drive Pins

The six pins PA02, PB00, PB01, PC04, PC05 and PC06 have high-drive output capabilities. Refer to Section 9.6.2 "High-drive I/O Pin : PA02, PC04, PC05, PC06" on page 115 for electrical characteristics.

### 3.4.6 USB Pins

When these pins are used for USB, the pins are behaving according to the USB specification. When used as GPIO pins or used for other peripherals, the pins have the same behavior as other normal I/O pins, but the characteristics are different. Refer to Section 9.6.3 "USB I/O Pin : PA25, PA26" on page 116 for electrical characteristics.

These pins are compliant to USB standard only when VDDIO power supply is 3.3V nominal.

## 4.6 Cortex-M4 implementations options

This table provides the specific configuration options implemented in the SAM4L series

| Option | Implementation |
|---|---|
| Inclusion of MPU | yes |
| Inclusion of FPU | No |
| Number of interrupts | 80 |
| Number of priority bits | 4 |
| Inclusion of the WIC | No |
| Embedded Trace Macrocell | No |
| Sleep mode instruction | Only WFI supported |
| Endianness | Little Endian |
| Bit-banding | No |
| SysTick timer | Yes |
| Register reset values | No |

**Table 4-1.** Cortex-M4 implementation options

## 4.7 Cortex-M4 Interrupts map

The table below shows how the interrupt request signals are connected to the NVIC.

**Table 4-2.** Interrupt Request Signal Map (Sheet 1 of 3)

| Line | Module | Signal |
|---|---|---|
| 0 | Flash Controller | HFLASHC |
| 1 | Peripheral DMA Controller | PDCA 0 |
| 2 | Peripheral DMA Controller | PDCA 1 |
| 3 | Peripheral DMA Controller | PDCA 2 |
| 4 | Peripheral DMA Controller | PDCA 3 |
| 5 | Peripheral DMA Controller | PDCA 4 |
| 6 | Peripheral DMA Controller | PDCA 5 |
| 7 | Peripheral DMA Controller | PDCA 6 |
| 8 | Peripheral DMA Controller | PDCA 7 |
| 9 | Peripheral DMA Controller | PDCA 8 |
| 10 | Peripheral DMA Controller | PDCA 9 |
| 11 | Peripheral DMA Controller | PDCA 10 |

**Table 4-2.** Interrupt Request Signal Map (Sheet 3 of 3)

| Line | Module | Signal |
|---|---|---|
| 48 | External Interrupt Controller | EIC 4 |
| 49 | External Interrupt Controller | EIC 5 |
| 50 | External Interrupt Controller | EIC 6 |
| 51 | External Interrupt Controller | EIC 7 |
| 52 | External Interrupt Controller | EIC 8 |
| 53 | Inter-IC Sound (I2S) Controller | IISC |
| 54 | Serial Peripheral Interface | SPI |
| 55 | Timer/Counter | TC00 |
| 56 | Timer/Counter | TC01 |
| 57 | Timer/Counter | TC02 |
| 58 | Timer/Counter | TC10 |
| 59 | Timer/Counter | TC11 |
| 60 | Timer/Counter | TC12 |
| 61 | Two-wire Master Interface | TWIM0 |
| 62 | Two-wire Slave Interface | TWIS0 |
| 63 | Two-wire Master Interface | TWIM1 |
| 64 | Two-wire Slave Interface | TWIS1 |
| 65 | Universal Synchronous Asynchronous Receiver Transmitter | USART0 |
| 66 | Universal Synchronous Asynchronous Receiver Transmitter | USART1 |
| 67 | Universal Synchronous Asynchronous Receiver Transmitter | USART2 |
| 68 | Universal Synchronous Asynchronous Receiver Transmitter | USART3 |
| 69 | ADC controller interface | ADCIFE |
| 70 | DAC Controller | DACC |
| 71 | Analog Comparator Interface | ACIFC |
| 72 | Audio Bitstream DAC | ABDACB |
| 73 | True Random Number Generator | TRNG |
| 74 | Parallel Capture | PARC |
| 75 | Capacitive Touch Module B | CATB |
| 77 | Two-wire Master Interface | TWIM2 |
| 78 | Two-wire Master Interface | TWIM3 |
| 79 | LCD Controller A | LCDCA |

## 5.2 Embedded Memories

- **Internal high-speed flash**
  - **512Kbytes (ATSAM4Lx8)**
  - **256Kbytes (ATSAM4Lx4)**
  - **128Kbytes (ATSAM4Lx2)**
    - **Pipelined flash architecture, allowing burst reads from sequential flash locations, hiding penalty of 1 wait state access**
    - **Pipelined flash architecture typically reduces the cycle penalty of 1 wait state operation compared to 0 wait state operation**
    - **100 000 write cycles, 15-year data retention capability**
    - **Sector lock capabilities, bootloader protection, security bit**
    - **32 fuses, erased during chip erase**
    - **User page for data to be preserved during chip erase**
- **Internal high-speed SRAM, single-cycle access at full speed**
  - **64Kbytes (ATSAM4Lx8)**
  - **32Kbytes (ATSAM4Lx4, ATSAM4Lx2)**

## 5.3 Physical Memory Map

The system bus is implemented as a bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even during boot. The 32-bit physical address space is mapped as follows:

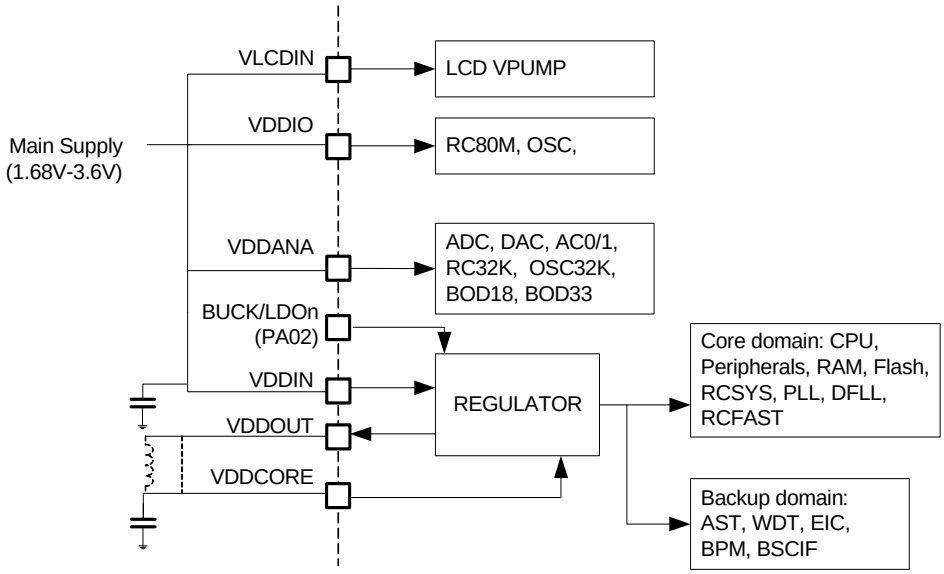
**Table 5-1.** ATSAM4L8/L4/L2 Physical Memory Map

| Memory | Start Address | Size | Size |
|---|---|---|---|
| | | ATSAM4Lx4 | ATSAM4Lx2 |
| Embedded Flash | 0x00000000 | 256Kbytes | 128Kbytes |
| Embedded SRAM | 0x20000000 | 32Kbytes | 32Kbytes |
| Cache SRAM | 0x21000000 | 4Kbytes | 4Kbytes |
| Peripheral Bridge A | 0x40000000 | 64Kbytes | 64Kbytes |
| Peripheral Bridge B | 0x400A0000 | 64Kbytes | 64Kbytes |
| AESA | 0x400B0000 | 256 bytes | 256 bytes |
| Peripheral Bridge C | 0x400E0000 | 64Kbytes | 64Kbytes |
| Peripheral Bridge D | 0x400F0000 | 64Kbytes | 64Kbytes |

| Memory | Start Address | Size |
|---|---|---|
| | | ATSAM4Lx8 |
| Embedded Flash | 0x00000000 | 512Kbytes |
| Embedded SRAM | 0x20000000 | 64Kbytes |
| Cache SRAM | 0x21000000 | 4Kbytes |
| Peripheral Bridge A | 0x40000000 | 64Kbytes |
| Peripheral Bridge B | 0x400A0000 | 64Kbytes |

The internal regulator is connected to the VDDIN pin and its output VDDOUT feeds VDDCORE in linear mode or through an inductor in switching mode. Figure 6-4 shows the power schematics to be used. All I/O lines will be powered by the same power ($V_{VDDIN}$=$V_{VDDIO}$=$V_{VDDANA}$).

**Figure 6-4.** Single Supply Mode




### 6.2.3 LCD Power Modes

#### *6.2.3.1 Principle*

LCD lines is powered using the device internal voltage sources provided by the LCDPWR block. When enabled, the LCDPWR blocks will generate the VLCD, BIASL, BIASH voltages.

LCD pads are splitted into three clusters that can be powered independently namely clusters A, B and C. A cluster can either be in GPIO mode or in LCD mode.

When a cluster is in GPIO mode, its VDDIO pin must be powered externally. None of its GPIO pin can be used as a LCD line

When a cluster is in LCD mode, each clusters VDDIO pin can be either forced externally (1.8-3.6V) or unconnected (nc). GPIOs in a cluster are not available when it is in LCD mode. A cluster is set in LCD mode by the LCDCA controller when it is enabled depending on the number of segments configured. The LCDPWR block is powered by the VLCDIN pin inside cluster A

When LCD feature is not used, VLCDIN must be always powered (1.8-3.6V). VLCD, CAPH, CAPL, BIASH, BIASL can be left unconnected in this case

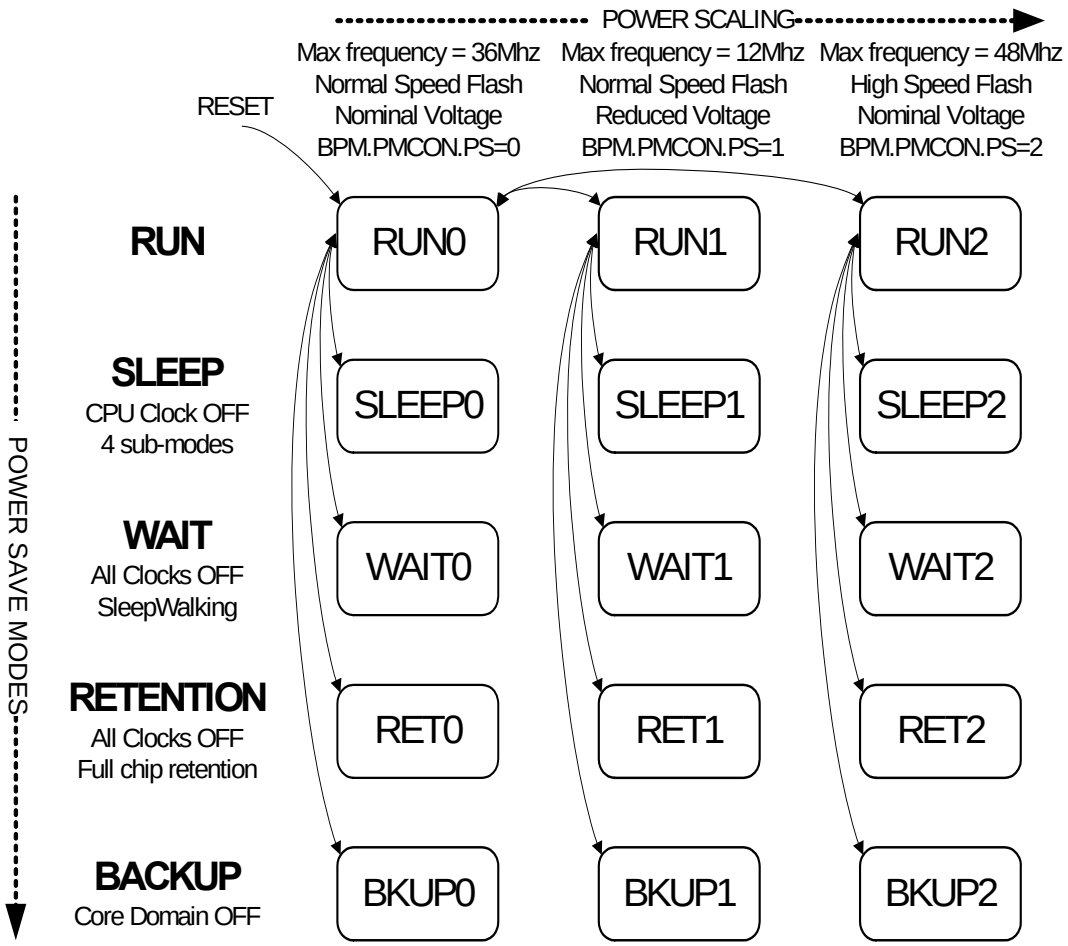
# 7. Low Power Techniques

The ATSAM4L8/L4/L2 supports multiple power configurations to allow the user to optimize its power consumption in different use cases. The Backup Power Manager (BPM) implements different solutions to reduce the power consumption:

- The Power Save modes intended to reduce the logic activity and to adapt the power configuration. See "Power Save Modes" on page 55.
- The Power Scaling intended to scale the power configuration (voltage scaling of the regulator). See "Power Scaling" on page 60.

These two techniques can be combined together.

**Figure 7-1.** Power Scaling and Power Save Mode Overview




## 7.1 Power Save Modes

Refer to Section 6. "Power and Startup Considerations" on page 46 to get definition of the core and the backup domains.

### 7.1.3 BACKUP Mode

The BACKUP mode allows achieving the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time.

The Core domain is powered-off. The internal SRAM and register contents of the Core domain are lost. The Backup domain is kept powered-on. The 32kHz clock (RC32K or OSC32K) is kept running if enabled to feed modules that require clocking.

In BACKUP mode, the configuration of the I/O lines is preserved. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677 to have more details.

#### *7.1.3.1 Entering BACKUP Mode*

The Backup mode is entered by using the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 1.

#### *7.1.3.2 Exiting BACKUP Mode*

Exit from BACKUP mode happens if a reset occurs or if an enabled wake up event occurs.

The reset sources are:

- BOD33 reset
- BOD18 reset
- WDT reset
- External reset in RESET_N pin

The wake up sources are:

- EIC lines (level transition only)
- BOD33 interrupt
- BOD18 interrupt
- AST alarm, periodic, overflow
- WDT interrupt

The RC32K or OSC32K should be used as clock source for modules if required. The PMCON.CK32S is used to select one of these two 32kHz clock sources.

Exiting the BACKUP mode is triggered by:

- a reset source: an internal reset sequence is performed according to the reset source. Once VDDCORE is stable and has the correct value according to RUN0 mode, the internal reset is released and program execution starts. The corresponding reset source is flagged in the Reset Cause register (RCAUSE) of the PM.
- a wake up source: the Backup domain is not reset. An internal reset is generated to the Core domain, and the system switches back to the previous RUN mode. Once VDDCORE is stable and has the correct value, the internal reset in the Core domain is released and program execution starts. The BKUP bit is set in the Reset Cause register (RCAUSE) of the PM. It allows the user to discriminate between the reset cause and a wake up cause from the BACKUP mode. The wake up cause can be found in the Backup Wake up Cause register (BPM.BKUPWCAUSE).

### 8.9.6 Security Considerations

In protected state this module may access sensible information located in the device memories. To avoid any risk of sensible data extraction from the module registers, all operations are non interruptible except by a disable command triggered by writing a one to CR.DIS. Issuing this command clears all the interface and internal registers.

Some registers have some special protection:

- It is not possible to read or write the LENGTH register when the part is protected.
- In addition, when the part is protected and an operation is ongoing, it is not possible to read the ADDR and DATA registers. Once an operation has started, the user has to wait until it has terminated by polling the DONE field in the Status Register (SR.DONE).

### 8.9.7 Chip Erase

The Chip erase operation consists in:

1. clearing all the volatile memories in the system
2. clearing the whole flash array
3. clearing the protected state

No proprietary or sensitive information is left in volatile memories once the protected state is disabled.

This feature is operated by writing a one to the CE bit of the Control Register (CR.CE). When the operation completes, SR.DONE is asserted.

### 8.9.8 Cortex-M4 Core Reset Source

The SMAP processes the EDP Core hold reset requests (Refer to Section 1.1.8 ”SMAP Core Reset Request Source” on page 6). When requested, it instructs the Power Manager to hold the Cortex-M4 core under reset.

The SMAP can de-assert the core reset request if a one is written to the Hold Core Reset bit in the Status Clear Register (SCR.HCR). This has the effect of releasing the CPU from its reset state. To assert again this signal, a new reset sequence with TCK tied low must be issued.

Note that clearing HCR with this module is only possible when it is enabled, for more information refer to Section 8.9.4 ”Initializing the Module” on page 78. Also note that asserting RESET_N automatically clears HCR.

*8.9.11.8 Chip Identification Register*

**Name:** CIDR

**Access Type:** Read-Only

**Offset:** 0xF0

**Reset Value:** -

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| EXT | NVPTYP | | | ARCH | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| ARCH | | | | SRAMSIZ | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| NVPSIZ2 | | | | NVPSIZ | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EPROC | | | | VERSION | | | |

Note: Refer to section CHIPID for more information on this register.

### 8.9.11.9 *Chip Identification Extension Register*

**Name:** EXID

**Access Type:** Read-Only

**Offset:** 0xF4

**Reset Value:** -

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---|---|---|---|---|---|---|---|
| EXID | | | | | | | |

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| EXID | | | | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| EXID | | | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EXID | | | | | | | |

Note: Refer to section CHIPID for more information on this register.

**Table 9-6.** ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 0 and 2

| Mode | Conditions | $T_A$ | Typical Wakeup Time | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|
| SLEEP0 | Switching mode | 25°C | 9 * Main clock cycles | 3817 | 4033 | µA |
| | | 85°C | | 3934 | 4174 | |
| SLEEP1 | Switching mode | 25°C | 9 * Main clock cycles + 500ns | 2341 | 2477 | |
| | | 85°C | | 2437 | 2585 | |
| SLEEP2 | Switching mode | 25°C | 9 * Main clock cycles + 500ns | 1758 | 1862 | |
| | | 85°C | | 1847 | 1971 | |
| SLEEP3 | Linear mode | 25°C | | 51 | 60 | |
| WAIT | OSC32K and AST running<br>Fast wake-up enable | | 1.5µs | 5.9 | 8.7 | |
| | OSC32K and AST stopped<br>Fast wake-up enable | | | 4.7 | 7.6 | |
| RETENTION | OSC32K running<br>AST running at 1kHz | | 1.5µs | 3.1 | 5.1 | |
| | AST and OSC32K stopped | | | 2.2 | 4.2 | |
| BACKUP | OSC32K running<br>AST running at 1kHz | | | 1.5 | 3.1 | |
| | AST and OSC32K stopped | | | 0.9 | 1.7 | |

1. These values are based on characterization. These values are not covered by test limits in production.

**Table 9-7.** ATSAM4L8 Current consumption and Wakeup time for power scaling mode 0 and 2

| Mode | Conditions | $T_A$ | Typical Wakeup Time | Typ | Max (1) | Unit |
|---|---|---|---|---|---|---|
| RUN | CPU running a Fibonacci algorithm<br>Linear mode | 25°C | N/A | 319 | 343 | µA/MHz |
| | | 85°C | | 326 | 350 | |
| | CPU running a CoreMark algorithm<br>Linear mode | 25°C | N/A | 343 | 387 | |
| | | 85°C | | 351 | 416 | |
| | CPU running a Fibonacci algorithm<br>Switching mode | 25°C | N/A | 181 | 198 | |
| | | 85°C | | 186 | 203 | |
| | CPU running a CoreMark algorithm<br>Switching mode | 25°C | N/A | 192 | 232 | |
| | | 85°C | | 202 | 239 | |

### 9.5.3 Peripheral Power Consumption in Power Scaling mode 0 and 2

The values in Table 9-11 are measured values of power consumption under the following conditions:

- Operating conditions, internal core supply (Figure 9-2)
  - $V_{VDDIN}$ = 3.3V
  - $V_{VDDCORE}$ supplied by the internal regulator in switching mode
- $T_A$ = 25°C
- Oscillators
  - OSC0 (crystal oscillator) stopped
  - OSC32K (32KHz crystal oscillator) running with external 32KHz crystal
  - DFLL running at 48MHz with OSC32K as reference clock
- Clocks
  - DFLL used as main clock source
  - CPU, AHB, and PB clocks undivided
- I/Os are inactive with internal pull-up
- Flash enabled in high speed mode
- CPU in SLEEP0 mode
- BOD18 and BOD33 disabled

Consumption active is the added current consumption when the module clock is turned on.

### 9.6.5 High Drive TWI Pin : PB00, PB01

**Table 9-19.** High Drive TWI Pin Characteristics in TWI configuration (1)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $R_{PULLUP}$ | Pull-up resistance (2) | PB00, PB01 | | | 40 | | kΩ |
| $R_{PULLDOWN}$ | Pull-down resistance(2) | | | | 40 | | kΩ |
| $V_{IL}$ | Input low-level voltage | | | -0.3 | | 0.3 * $V_{VDD}$ | V |
| $V_{IH}$ | Input high-level voltage | | | 0.7 * $V_{VDD}$ | | $V_{VDD}$ + 0.3 | |
| $V_{OL}$ | Output low-level voltage | | | | | 0.4 | |
| $V_{OH}$ | Output high-level voltage | | | $V_{VDD}$ - 0.4 | | | |
| $I_{OL}$ | Output low-level current (3) | DRIVEL=0 | | | | 0.5 | mA |
| | | DRIVEL=1 | | | | 1.0 | |
| | | DRIVEL=2 | | | | 1.6 | |
| | | DRIVEL=3 | | | | 3.1 | |
| | | DRIVEL=4 | | | | 6.2 | |
| | | DRIVEL=5 | | | | 9.3 | |
| | | DRIVEL=6 | | | | 15.5 | |
| | | DRIVEL=7 | | | | 21.8 | |
| $I_{CS}$ | Current Source(2) | DRIVEH=0 | | | 0.5 | | mA |
| | | DRIVEH=1 | | | 1 | | |
| | | DRIVEH=2 | | | 1.5 | | |
| | | DRIVEH=3 | | | 3 | | |
| $f_{MAX}$ | Max frequency(2) | HsMode with Current source; DRIVEx=3, SLEW=0 Cbus = 400pF, $V_{VDD}$ = 1.68V | | 3.5 | 6.4 | | MHz |
| $t_{RISE}$ | Rise time(2) | HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, $V_{VDD}$ = 1.68V | | | 28 | 38 | ns |
| $t_{FALL}$ | Fall time(2) | Standard Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, $V_{VDD}$ = 1.68V | | | 50 | 95 | ns |
| | | HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, $V_{VDD}$ = 1.68V | | | 50 | 95 | |

1. $V_{VDD}$ corresponds to either $V_{VDDIN}$ or $V_{VDDIO}$, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

## 9.10 Timing Characteristics

### 9.10.1 RESET_N Timing

**Table 9-53.** RESET_N Waveform Parameters [1]

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $t_{RESET}$ | RESET_N minimum pulse length | | 10 | | ns |

1. These values are based on simulation. These values are not covered by test limits in production.

### 9.10.2 USART in SPI Mode Timing

#### *9.10.2.1 Master mode*

**Figure 9-7.** USART in SPI Master Mode with (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

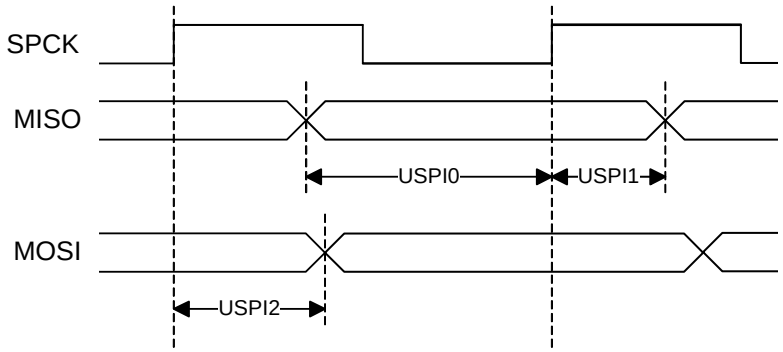



**Figure 9-8.** USART in SPI Master Mode with (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

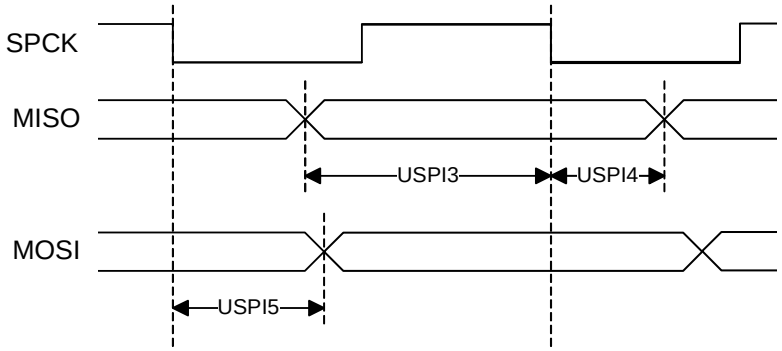


**Table 9-59.** USART1 in SPI mode Timing, Slave Mode[1]

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| USPI6 | SPCK falling to MISO delay | $V_{VDDIO}$ from 3.0V to 3.6V, maximum external capacitor = 40pF | | 373.58 | ns |
| USPI7 | MOSI setup time before SPCK rises | | 4.16 + $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ | | |
| USPI8 | MOSI hold time after SPCK rises | | 46.69 -( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI9 | SPCK rising to MISO delay | | | 373.54 | |
| USPI10 | MOSI setup time before SPCK falls | | 4.16 +( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI11 | MOSI hold time after SPCK falls | | 46.69 -( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI12 | NSS setup time before SPCK rises | | 200.43 | | |
| USPI13 | NSS hold time after SPCK falls | | -16.5 | | |
| USPI14 | NSS setup time before SPCK falls | | 200.43 | | |
| USPI15 | NSS hold time after SPCK rises | | -16.5 | | |

**Table 9-60.** USART2 in SPI mode Timing, Slave Mode[1]

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| USPI6 | SPCK falling to MISO delay | $V_{VDDIO}$ from 3.0V to 3.6V, maximum external capacitor = 40pF | | 770.02 | ns |
| USPI7 | MOSI setup time before SPCK rises | | 136.56 + $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ | | |
| USPI8 | MOSI hold time after SPCK rises | | 47.9 -( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI9 | SPCK rising to MISO delay | | | 570.19 | |
| USPI10 | MOSI setup time before SPCK falls | | 136.73 +( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI11 | MOSI hold time after SPCK falls | | 47.9 -( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI12 | NSS setup time before SPCK rises | | 519.87 | | |
| USPI13 | NSS hold time after SPCK falls | | -1.83 | | |
| USPI14 | NSS setup time before SPCK falls | | 519.87 | | |
| USPI15 | NSS hold time after SPCK rises | | -1.83 | | |

**Table 9-61.** USART3 in SPI mode Timing, Slave Mode[1]

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| USPI6 | SPCK falling to MISO delay | $V_{VDDIO}$ from 3.0V to 3.6V, maximum external capacitor = 40pF | | 593.9 | ns |
| USPI7 | MOSI setup time before SPCK rises | | 45.93 + $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ | | |
| USPI8 | MOSI hold time after SPCK rises | | 47.03 -( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI9 | SPCK rising to MISO delay | | | 593.38 | |
| USPI10 | MOSI setup time before SPCK falls | | 45.93 +( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI11 | MOSI hold time after SPCK falls | | 47.03 -( $t_{SAMPLE}$[2] + $t_{CLK\_USART}$ ) | | |
| USPI12 | NSS setup time before SPCK rises | | 237.5 | | |
| USPI13 | NSS hold time after SPCK falls | | -1.81 | | |
| USPI14 | NSS setup time before SPCK falls | | 237.5 | | |
| USPI15 | NSS hold time after SPCK rises | | -1.81 | | |

Notes: 1. These values are based on simulation. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left(\left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor + \frac{1}{2}\right) \times t_{CLKUSART}$

### Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, USPI7 + USPI8 or USPI10 + USPI11 depending on CPOL and NCPHA. $f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

### Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

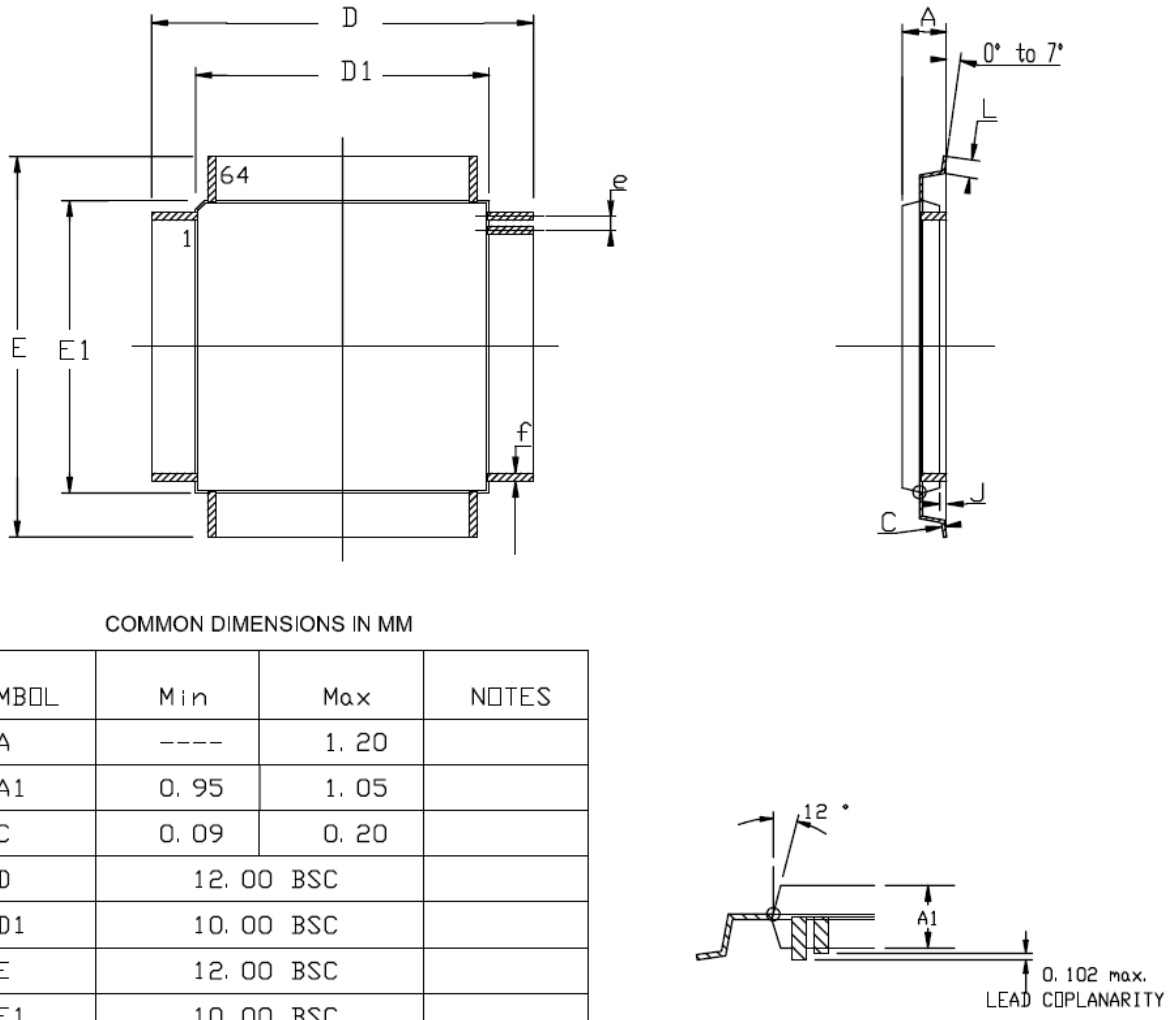
Where $SPIn$ is the MISO delay, USPI6 or USPI9 depending on CPOL and NCPHA. $T_{SETUP}$ is the SPI master setup time. refer to the SPI master datasheet for $T_{SETUP}$ . $f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock. $f_{PINMAX}$ is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

**Table 9-66.** SWD Timings[1]

| Symbol | Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Thigh | SWDCLK High period | $V_{VDDIO}$ from 3.0 V to 3.6 V, maximum external capacitor = 40 pF | 10 | 500 000 | ns |
| Tlow | SWDCLK Low period | | 10 | 500 000 | |
| Tos | SWDIO output skew to falling edge SWDCLK | | -5 | 5 | |
| Tis | Input Setup time required between SWDIO | | 4 | - | |
| Tih | Input Hold time required between SWDIO and rising edge SWDCLK | | 1 | - | |

Note: 1. These values are based on simulation. These values are not covered by test limits in production or characterization.

**Figure 10-7.** TQFP-64 Package Drawing




COMMON DIMENSIONS IN MM

| SYMBOL | Min | Max | NOTES |
|---|---|---|---|
| A | ---- | 1.20 | |
| A1 | 0.95 | 1.05 | |
| C | 0.09 | 0.20 | |
| D | 12.00 BSC | | |
| D1 | 10.00 BSC | | |
| E | 12.00 BSC | | |
| E1 | 10.00 BSC | | |
| J | 0.05 | 0.15 | |
| L | 0.45 | 0.75 | |
| e | 0.50 BSC | | |
| f | 0.17 | 0.27 | |

**Table 10-20.** Device and Package Maximum Weight

| | |
|---|---|
| 300 | mg |

**Table 10-21.** Package Characteristics

| | |
|---|---|
| Moisture Sensitivity Level | MSL3 |

**Table 10-22.** Package Reference

| | |
|---|---|
| JEDEC Drawing Reference | MS-026 |
| JESD97 Classification | E3 |

# 11. Ordering Information

**Table 11-1.** ATSAM4LC8 Sub Serie Ordering Information

| Ordering Code | Flash (Kbytes) | RAM (Kbytes) | Package | Conditioning | Package Type | Temperature Operating Range |
|---|---|---|---|---|---|---|
| ATSAM4LC8CA-AU | 512 | 64 | TQFP100 | Tray | Green | Industrial -40°C to 85°C |
| ATSAM4LC8CA-AUR | | | | Reel | | |
| ATSAM4LC8CA-CFU | | | VFBGA100 | Tray | | |
| ATSAM4LC8CA-CFUR | | | | Reel | | |
| ATSAM4LC8BA-AU | | | TQFP64 | Tray | | |
| ATSAM4LC8BA-AUR | | | | Reel | | |
| ATSAM4LC8BA-MU | | | QFN64 | Tray | | |
| ATSAM4LC8BA-MUR | | | | Reel | | |
| ATSAM4LC8BA-UUR | | | WLCSP64 | Reel | | |
| ATSAM4LC8AA-MU | | | QFN48 | Tray | | |
| ATSAM4LC8AA-MUR | | | | Reel | | |

**Table 11-2.** ATSAM4LC4 Sub Serie Ordering Information

| Ordering Code | Flash (Kbytes) | RAM (Kbytes) | Package | Conditioning | Package Type | Temperature Operating Range |
|---|---|---|---|---|---|---|
| ATSAM4LC4CA-AU-ES | 256 | 32 | TQFP100 | ES | Green | N/A |
| ATSAM4LC4CA-AU | | | | Tray | | Industrial -40°C to 85°C |
| ATSAM4LC4CA-AUR | | | | Reel | | |
| ATSAM4LC4CA-CFU | | | VFBGA100 | Tray | | Industrial -40°C to 85°C |
| ATSAM4LC4CA-CFUR | | | | Reel | | |
| ATSAM4LC4BA-AU-ES | | | TQFP64 | ES | | N/A |
| ATSAM4LC4BA-AU | | | | Tray | | Industrial -40°C to 85°C |
| ATSAM4LC4BA-AUR | | | | Reel | | |
| ATSAM4LC4BA-MU-ES | | | QFN64 | ES | | N/A |
| ATSAM4LC4BA-MU | | | | Tray | | Industrial -40°C to 85°C |
| ATSAM4LC4BA-MUR | | | | Reel | | |
| ATSAM4LC4BA-UUR | | | WLCSP64 | Reel | | Industrial -40°C to 85°C |
| ATSAM4LC4AA-AU-ES | | | TQFP48 | ES | | N/A |
| ATSAM4LC4AA-AU | | | | Tray | | Industrial -40°C to 85°C |
| ATSAM4LC4AA-AUR | | | | Reel | | |
| ATSAM4LC4AA-MU-ES | | | QFN48 | ES | | N/A |
| ATSAM4LC4AA-MU | | | | Tray | | Industrial -40°C to 85°C |
| ATSAM4LC4AA-MUR | | | | Reel | | |