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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	75
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4lc8ca-au

3.3 Signals Description

The following table gives details on signal names classified by peripheral.

Table 3-8. Signal Descriptions List (Sheet 1 of 4)

Signal Name	Function	Type	Active Level	Comments
Audio Bitstream DAC - ABDACB				
CLK	D/A clock output	Output		
DAC1 - DAC0	D/A bitstream outputs	Output		
DACN1 - DACN0	D/A inverted bitstream outputs	Output		
Analog Comparator Interface - ACIFC				
ACAN1 - ACAN0	Analog Comparator A negative references	Analog		
ACAP1 - ACAP0	Analog Comparator A positive references	Analog		
ACBN1 - ACBN0	Analog Comparator B negative references	Analog		
ACBP1 - ACBP0	Analog Comparator B positive references	Analog		
ADC controller interface - ADCIFE				
AD14 - AD0	Analog inputs	Analog		
ADVREFP	Positive voltage reference	Analog		
TRIGGER	External trigger	Input		
Backup System Control Interface - BSCIF				
XIN32	32 kHz Crystal Oscillator Input	Analog/ Digital		
XOUT32	32 kHz Crystal Oscillator Output	Analog		
Capacitive Touch Module B - CATB				
DIS	Capacitive discharge line	Output		
SENSE31 - SENSE0	Capacitive sense lines	I/O		
DAC Controller - DACC				
DAC external trigger	DAC external trigger	Input		
DAC voltage output	DAC voltage output	Analog		
Enhanced Debug Port For ARM Products - EDP				
TCK/SWCLK	JTAG / SW Debug Clock	Input		
TDI	JTAG Debug Data In	Input		
TDO/TRACESWO	JTAG Debug Data Out / SW Trace Out	Output		
TMS/SWDIO	JTAG Debug Mode Select / SW Data	I/O		
External Interrupt Controller - EIC				
EXTINT8 - EXTINT0	External interrupts	Input		
Glue Logic Controller - GLOC				
IN7 - IN0	Lookup Tables Inputs	Input		
OUT1 - OUT0	Lookup Tables Outputs	Output		

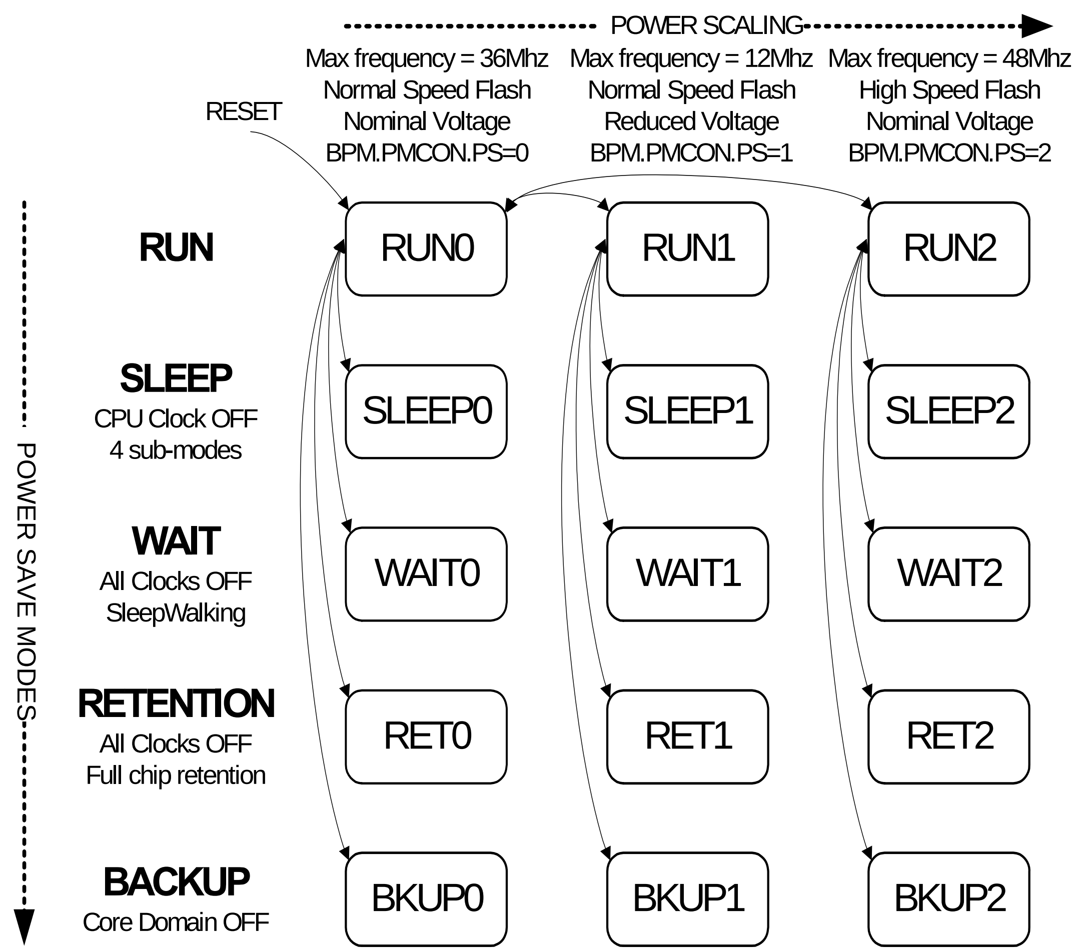
7. Low Power Techniques

The ATSAM4L8/L4/L2 supports multiple power configurations to allow the user to optimize its power consumption in different use cases. The Backup Power Manager (BPM) implements different solutions to reduce the power consumption:

- The Power Save modes intended to reduce the logic activity and to adapt the power configuration. See "Power Save Modes" on page 55.
- The Power Scaling intended to scale the power configuration (voltage scaling of the regulator). See "Power Scaling" on page 60.

These two techniques can be combined together.

Figure 7-1. Power Scaling and Power Save Mode Overview

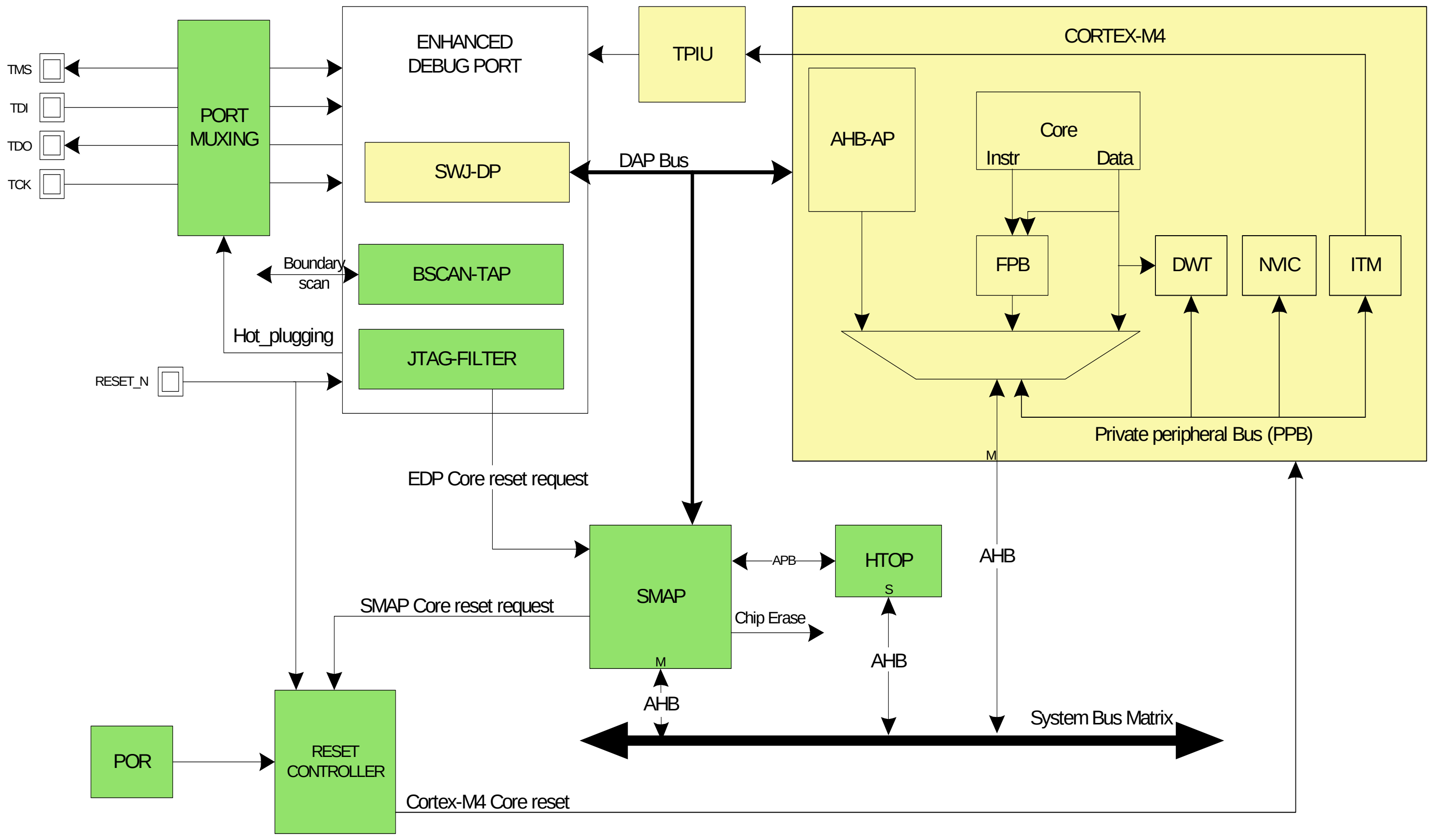


7.1 Power Save Modes

Refer to Section 6. "Power and Startup Considerations" on page 46 to get definition of the core and the backup domains.

8.3 Block diagram

Figure 8-1. Debug and Test Block Diagram



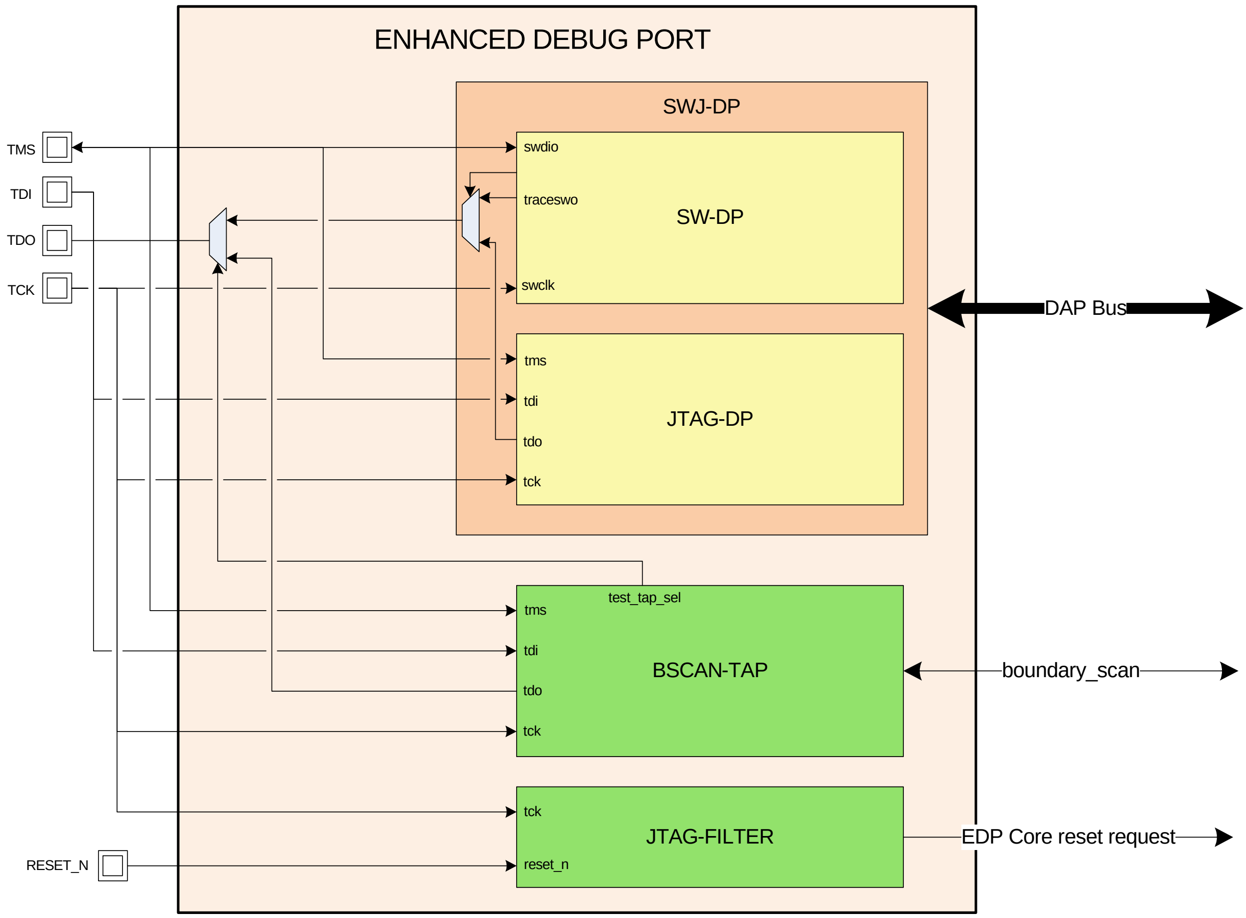
note: Boxes with a plain corner are SAM4L specific.

8.4 I/O Lines Description

Refer to Section 1.1.4 "I/O Lines Description" on page 4.

8.7.3 Block Diagram

Figure 8-3. Enhanced Debug Port Block Diagram



8.7.4 I/O Lines Description

Table 8-1. I/O Lines Description

Name	JTAG Debug Port		SWD Debug Port	
	Type	Description	Type	Description
TCK/SWCLK	I	Debug Clock	I	Serial Wire Clock
TDI	I	Debug Data in	-	NA
TDO/TRACESWO	O	Debug Data Out	O	Trace asynchronous Data Out
TMS/SWDIO	I	Debug Mode Select	I/O	Serial Wire Input/Output
RESET_N	I	Reset	I	Reset

8.9.11.5 Length Register

Name: LENGTH

Access Type: Read/Write

Offset: 0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
LENGTH							

23	22	21	20	19	18	17	16
LENGTH							

15	14	13	12	11	10	9	8
LENGTH							

7	6	5	4	3	2	1	0
LENGTH						-	-

- **LENGTH: Length Value, Bits 1-0 are always zero**

8.9.11.6 Data Register

Name: DATA

Access Type: Read/Write

Offset: 0x14

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DATA							

23	22	21	20	19	18	17	16
DATA							

15	14	13	12	11	10	9	8
DATA							

7	6	5	4	3	2	1	0
DATA							

- **DATA: Generic data register**

9. Electrical Characteristics

9.1 Absolute Maximum Ratings*

Table 9-1. Absolute Maximum Ratings

Operating temperature	-40°C to +85°C
Storage temperature	-60°C to +150°C
Voltage on input pins with respect to ground	-0.3V to V_{VDD} [(1)]+0.3V
Total DC output current on all I/O pins VDDIO	120 mA
Total DC output current on all I/O pins VDDIN	100 mA
Total DC output current on all I/O pins VDDANA	50 mA
Maximum operating voltage VDDIO, VDDIN	3.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details

9.2 Operating Conditions

All the electrical characteristics are applicable to the following conditions unless otherwise specified :

– operating voltage range 1,68V to 3,6V for VDDIN, VDDIO & VDDANA

– Power Scaling 0 and 2 modes

– operating temperature range: TA = -40°C to 85°C and for a junction temperature up to TJ = 100°C.

Typical values are base on TA = 25°c and VDDIN,VDDIO,VDDANA = 3,3V unless otherwise specified

9.3 Supply Characteristics

Table 9-2. Supply Characteristics

Symbol	Conditions	Voltage		
		Min	Max	Unit
V_{VDDIO}, V_{VDDIN}, V_{VDDANA}	PS1 (FCPU<=12MHz) Linear mode	1.68	3.6	V
	PS0 & PS2 (FCPU>12MHz) Linear mode	1.8		
	Switching mode	2.0 [(1)]		

1. Below 2.3V, linear mode is more power efficient than switching mode.

Refer to Section 6. "Power and Startup Considerations" on page 46 for details about Power Supply

9.4 Maximum Clock Frequencies

Table 9-4. Maximum Clock Frequencies in Power Scaling Mode 0/2 and RUN Mode

Symbol	Parameter	Description	Max	Units
f_{CPU}	CPU clock frequency		48	MHz
f_{PBA}	PBA clock frequency		48	
f_{PBB}	PBB clock frequency		48	
f_{PBC}	PBC clock frequency		48	
f_{PBD}	PBD clock frequency		48	
f_{GCLK0}	GCLK0 clock frequency	DFLLIF main reference, GCLK0 pin	50	
f_{GCLK1}	GCLK1 clock frequency	DFLLIF dithering and SSG reference, GCLK1 pin	50	
f_{GCLK2}	GCLK2 clock frequency	AST, GCLK2 pin	20	
f_{GCLK3}	GCLK3 clock frequency	CATB, GCLK3 pin	50	
f_{GCLK4}	GCLK4 clock frequency	FLO and AESA	50	
f_{GCLK5}	GCLK5 clock frequency	GLOC, TC0 and RC32KIFB_REF	80	
f_{GCLK6}	GCLK6 clock frequency	ABDACB and IISC	50	
f_{GCLK7}	GCLK7 clock frequency	USBC	50	
f_{GCLK8}	GCLK8 clock frequency	TC1 and PEVC[0]	50	
f_{GCLK9}	GCLK9 clock frequency	PLL0 and PEVC[1]	50	
f_{GCLK10}	GCLK10 clock frequency	ADCIFE	50	
f_{GCLK11}	GCLK11 clock frequency	Master generic clock. Can be used as source for other generic clocks	150	
f_{OSC0}	OSC0 output frequency	Oscillator 0 in crystal mode	30	
		Oscillator 0 in digital clock mode	50	
f_{PLL}	PLL output frequency	Phase Locked Loop	240	
f_{DFLL}	DFLL output frequency	Digital Frequency Locked Loop	220	
f_{RC80M}	RC80M output frequency	Internal 80MHz RC Oscillator	80	

9.5 Power Consumption

9.5.1 Power Scaling 0 and 2

The values in Table 9-6 are measured values of power consumption under the following conditions, except where noted:

- Operating conditions for power scaling mode 0 and 2
  - V_{VDDIN} = 3.3V
  - Power Scaling mode 0 is used for CPU frequencies under 36MHz
  - Power Scaling mode 2 is used for CPU frequencies above 36MHz
- Wake up time from low power modes is measured from the edge of the wakeup signal to the first instruction fetched in flash.
- Oscillators
  - OSC0 (crystal oscillator) stopped
  - OSC32K (32kHz crystal oscillator) running with external 32kHz crystal
  - DFLL using OSC32K as reference and running at 48MHz
- Clocks
  - DFLL used as main clock source
  - CPU, AHB clocks undivided
  - APBC and APBD clocks divided by 4
  - APBA and APBB bridges off
  - The following peripheral clocks running
  - • PM, SCIF, AST, FLASHCALW, APBC and APBD bridges
  - All other peripheral clocks stopped
- I/Os are inactive with internal pull-up
- CPU is running on flash with 1 wait state
- Low power cache enabled
- BOD18 and BOD33 disabled

Table 9-6. ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max [1]	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	296	326	µA/MHz
		85°C		300	332	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	320	377	
		85°C		326	380	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	177	198	
		85°C		179	200	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	186	232	
		85°C		195	239	

Table 9-10. Typical Power Consumption running CoreMark on CPU clock sources [1]

RCSYS (MCSEL = 0)	Power scaling mode 1	Switching Mode	0.115	978	µA/MHz
OSC0 (MCSEL = 1)	Power scaling mode 1		0.5	354	
			12	114	
	Power scaling mode 0		12	228	
			30	219	
OSC0 (MCSEL = 1) External Clock (MODE=0)	Power scaling mode 1		0.6	292	
			12	111	
	Power scaling mode 0		12	193	
	Power scaling mode 2		50	194	
PLL (MCSEL = 2)	Power scaling mode 2 Input Freq = 4MHz from OSC0		40	188	
			50	185	
DFLL (MCSEL = 3)	Power scaling mode 0 Input Freq = 32kHz from OSC32K		20	214	
	Power scaling mode 2 Input Freq = 32kHz from OSC32K		50	195	
RC1M (MCSEL = 4)	Power scaling mode 1		1	267	
RCFAST (MCSEL = 5)	Power scaling mode 1 RCFAST frequency is configurable from 4 to 12MHz		4	153	
			12	114	
RC80M (MCSEL = 6)	Power scaling mode 2 f_{CPU} = RC80M / 2 = 40MHz		40	211	

1. These values are based on characterization. These values are not covered by test limits in production.

9.6 I/O Pin Characteristics

9.6.1 Normal I/O Pin

Table 9-13. Normal I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			V
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			0.8	mA
			2.7V<V_{VDD}<3.6V			1.6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			0.8	mA
			2.7V<V_{VDD}<3.6V			1.6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, load = 25pF			35	ns
		OSRR0=1				45	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, load = 25pF			19	ns
		OSRR0=1				23	
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, load = 25pF			36	ns
		OSRR0=1				47	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, load = 25pF			20	ns
		OSRR0=1				24	
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			17	MHz
		OSRR0=1				15	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			27	MHz
		OSRR0=1				23	MHz
I_{LEAK}	Input leakage current(3)		Pull-up resistors disabled		0.01	1	µA
C_{IN}	Input capacitance(2)				5		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization

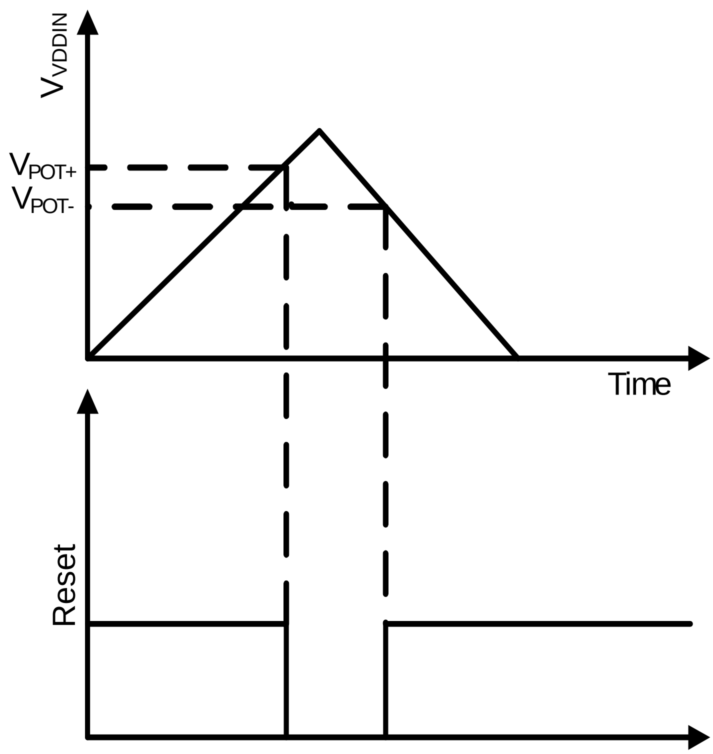
9.9.2 Power-on Reset 33 Characteristics

Table 9-41. POR33 Characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{POT+}	Voltage threshold on V_{VDDIN} rising		1.25		1.55	V
V_{POT-}	Voltage threshold on V_{VDDIN} falling		0.95		1.30	

1. These values are based on characterization. These values are not covered by test limits in production.

Figure 9-4. POR33 Operating Principle



9.9.3 Brown Out Detectors Characteristics

Table 9-42. BOD18 Characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Step size, between adjacent values in BSCIF.BOD18LEVEL[1]			10.1		mV
V_{HYST}	BOD hysteresis[1]	T = 25°C	3		40	
t_{DET}	Detection time[1]	Time with $V_{VDDCORE}$ < BOD18.LEVEL necessary to generate a reset signal	1.2			µs
I_{BOD}	Current consumption[1]	on VDDIN		7.4	14	µA
		on VDDCORE			7	
$t_{STARTUP}$	Startup time[1]				4.5	µs

9.9.4 Analog- to Digital Converter Characteristics

Table 9-45. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Temperature range		-40		+85	°C
	Resolution [1]	Max		12	12 [2]	Bit
	Sampling clock [3]	Differential modes, Gain=1X	5		300	kHz
		Unipolar modes, Gain=1X	5		250	
f_{ADC}	ADC clock frequency[3]	Differential modes	0.03		1.8	MHz
		Unipolar modes	0.03		1.5	
$T_{SAMPLEHOLD}$	Sampling time[3]	Differential modes	16.5		277	µs
		Unipolar modes	16.5		333	
	Conversion rate[1]	1X gain, differential			300	kSps
	Internal channel conversion rate[3]	V_{VDD}/10, Bandgap and Temperature channels			125	kSps
	Conversion time (latency) Differential mode (no windowing)	1X gain, (resolution/2)+gain [4]			6	Cycles
		2X and 4X gain			7	
		8X and 16X gain			8	
		32X and 64X gain			9	
		64X gain and unipolar			10	

1. These values are based on characterization. These values are not covered by test limits in production
2. Single ended or using divide by two max resolution: 11 bits
3. These values are based on simulation. These values are not covered by test limits in production
4. See Figure 9-5

Figure 9-5. Maximum input common mode voltage

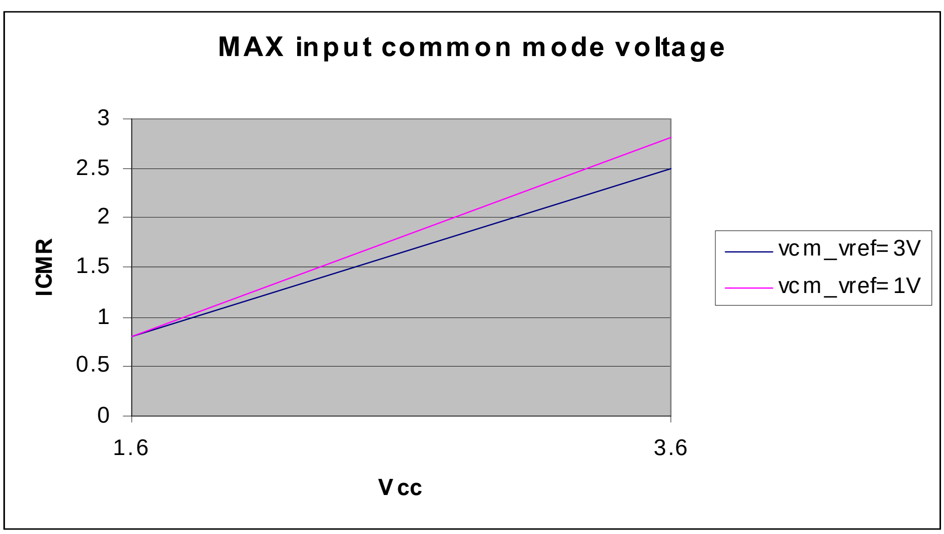


Table 9-46. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDDANA	Supply voltage (1)		1.6		3.6	V
	Reference range (2)	Differential mode	1.0		VDDANA -0.6	V
		Unipolar and Window modes	1.0		1.0	
		Using divide by two function (differential)	2.0		VDDANA	
	Absolute min, max input voltage(2)		-0,1		VDDANA +0.1	V
	Start up time(2)	ADC with reference already enabled		12	24	Cycles
		No gain compensation Reference buffer			5	µs
		Gain compensation Reference buffer			60	Cycles
R_{SAMPLE}	Input channel source resistance(2)				0.5	kΩ
C_{SAMPLE}	Sampling capacitance(2)		2.9	3.6	4.3	pF
	Reference input source resistance(2)	Gain compensation			2	kΩ
		No gain compensation			1	MΩ
	ADC reference settling time(2)	After changing reference/mode (3)		5	60	Cycles

1. These values are based on characterization. These values are not covered by test limits in production
2. These values are based on simulation. These values are not covered by test limits in production
3. Requires refresh/flush otherwise conversion time (latency) + 1

Table 9-47. Differential mode, gain=1

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Accuracy without compensation (1)			7		ENOB
	Accuracy after compensation(1)	(INL, gain and offset)			11	ENOB
INL	Integral Non Linearity (2)	After calibration, Gain compensation		1.2	1.7	LSBs
DNL	Differential Non Linearity(2)	After calibration		0.7	1.0	LSBs
	Gain error (2)	External reference	-5.0	-1.0	5.0	mV
		VDDANA/1.6	-40		40	
		VDDANA/2.0	-40		40	
		Bandgap After calibration	-30		30	
	Gain error drift vs voltage(1)	External reference	-2		2	mV/V
	Gain error drift vs temperature(1)	After calibration + bandgap drift If using onchip bandgap			0.08	mV/°K
	Offset error (2)	External reference	-5.0		5.0	mV
		VDDANA/1.6	-10		10	
		VDDANA/2.0	-10		10	
		Bandgap After calibration	-10		10	
	Offset error drift vs voltage(1)		-4		4	mV/V

9.10 Timing Characteristics

9.10.1 RESET_N Timing

Table 9-53. RESET_N Waveform Parameters [(1)]

Symbol	Parameter	Conditions	Min	Max	Units
t_{RESET}	RESET_N minimum pulse length		10		ns

1. These values are based on simulation. These values are not covered by test limits in production.

9.10.2 USART in SPI Mode Timing

9.10.2.1 Master mode

Figure 9-7. USART in SPI Master Mode with (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

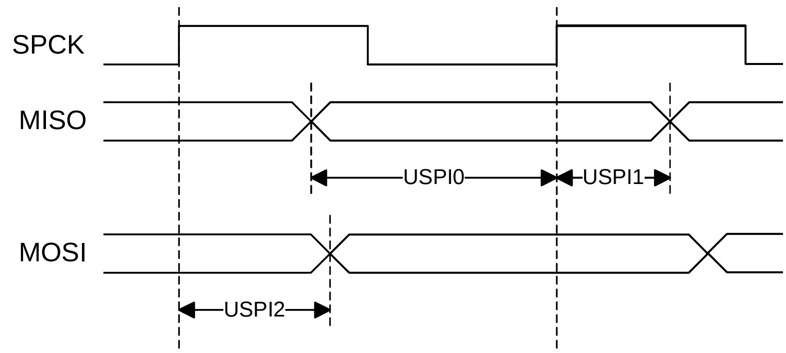


Figure 9-8. USART in SPI Master Mode with (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

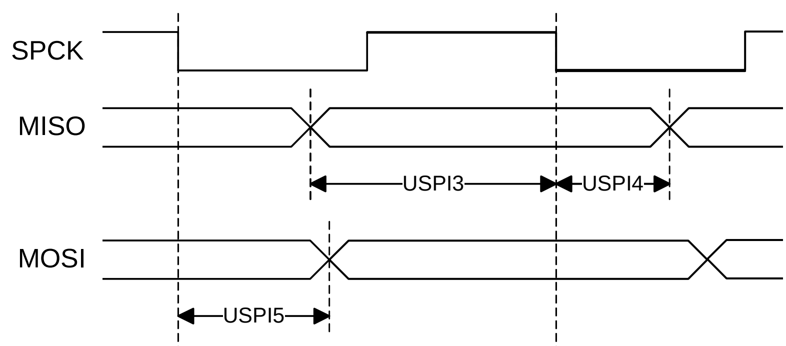


Table 9-54. USART0 in SPI Mode Timing, Master Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI0	MISO setup time before SPCK rises	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF	123.2 + t_{SAMPLE}[2]		ns
USPI1	MISO hold time after SPCK rises		24.74 -t_{SAMPLE}[2]		
USPI2	SPCK rising to MOSI delay			513.56	
USPI3	MISO setup time before SPCK falls		125.99 + t_{SAMPLE}[2]		
USPI4	MISO hold time after SPCK falls		24.74 -t_{SAMPLE}[2]		
USPI5	SPCK falling to MOSI delay			516.55	

Table 9-55. USART1 in SPI Mode Timing, Master Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI0	MISO setup time before SPCK rises	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF	69.28 + t_{SAMPLE}[2]		ns
USPI1	MISO hold time after SPCK rises		25.75 -t_{SAMPLE}[2]		
USPI2	SPCK rising to MOSI delay			99.66	
USPI3	MISO setup time before SPCK falls		73.12 + t_{SAMPLE}[2]		
USPI4	MISO hold time after SPCK falls		28.10 -t_{SAMPLE}[2]		
USPI5	SPCK falling to MOSI delay			102.01	

Table 9-56. USART2 in SPI Mode Timing, Master Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI0	MISO setup time before SPCK rises	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF	69.09 + t_{SAMPLE}[2]		ns
USPI1	MISO hold time after SPCK rises		26.52 -t_{SAMPLE}[2]		
USPI2	SPCK rising to MOSI delay			542.96	
USPI3	MISO setup time before SPCK falls		72.55 + t_{SAMPLE}[2]		
USPI4	MISO hold time after SPCK falls		28.37 -t_{SAMPLE}[2]		
USPI5	SPCK falling to MOSI delay			544.80	

Table 9-57. USART3 in SPI Mode Timing, Master Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI0	MISO setup time before SPCK rises	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF	147.24 + t_{SAMPLE}[2]		ns
USPI1	MISO hold time after SPCK rises		25.80 -t_{SAMPLE}[2]		
USPI2	SPCK rising to MOSI delay			88.23	
USPI3	MISO setup time before SPCK falls		154.9 + t_{SAMPLE}[2]		
USPI4	MISO hold time after SPCK falls		26.89 -t_{SAMPLE}[2]		
USPI5	SPCK falling to MOSI delay			89.32	

Notes:
1. These values are based on simulation. These values are not covered by test limits in production.
2. Where: $t_{SAMPLE} = t_{SPCK} - \left(\left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor \frac{1}{2} \right) \times t_{CLKUSART}$

Figure 9-10. USART in SPI Slave Mode with (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

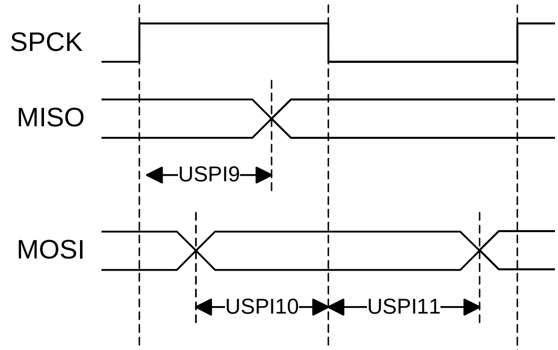


Figure 9-11. USART in SPI Slave Mode, NPCS Timing

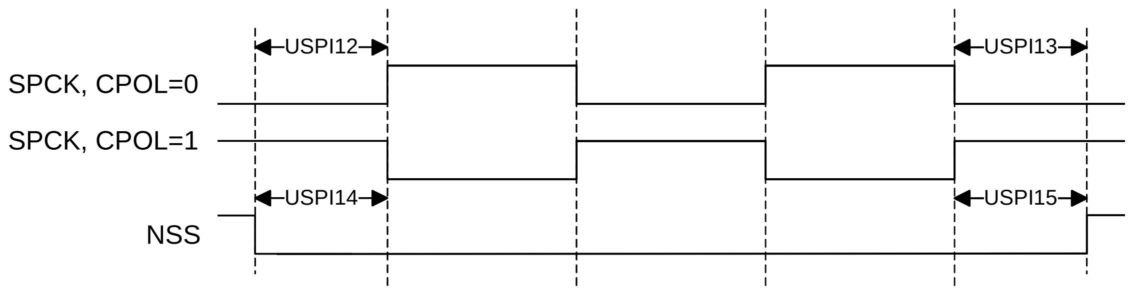


Table 9-58. USART0 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		740.67	ns
USPI7	MOSI setup time before SPCK rises		$56.73 + t_{SAMPLE}$[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		45.18 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			670.18	
USPI10	MOSI setup time before SPCK falls		56.73 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		45.18 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		688.71		
USPI13	NSS hold time after SPCK falls		-2.25		
USPI14	NSS setup time before SPCK falls		688.71		
USPI15	NSS hold time after SPCK rises		-2.25		

10. Mechanical Characteristics

10.1 Thermal Considerations

10.1.1 Thermal Data

Table 10-1 summarizes the thermal resistance data depending on the package.

Table 10-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP100	48.1	·C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP100	13.3	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	VFBGA100	31.1	·C/W
θ_{JC}	Junction-to-case thermal resistance		VFBGA100	6.9	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	WLCSP64	26.9	·C/W
θ_{JC}	Junction-to-case thermal resistance		WLCSP64	0.2	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP64	49.6	·C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP64	13.5	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN64	22.0	·C/W
θ_{JC}	Junction-to-case thermal resistance		QFN64	1.3	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP48	51.1	·C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP48	13.7	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN48	24.9	·C/W
θ_{JC}	Junction-to-case thermal resistance		QFN48	1.3	

10.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

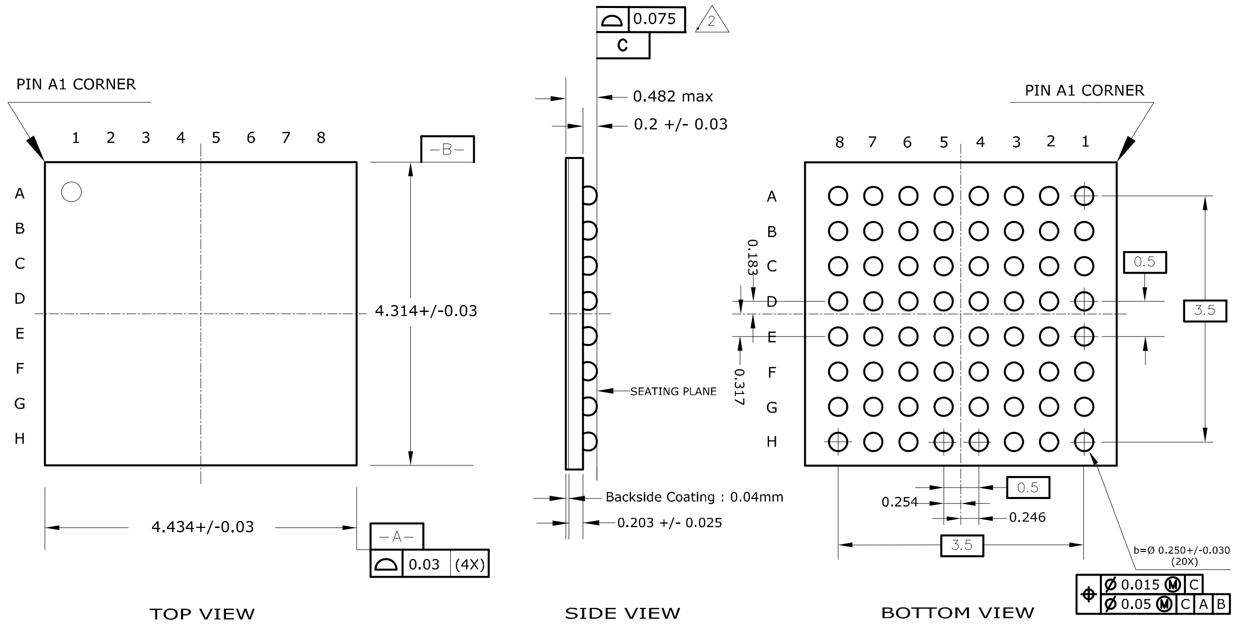
1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 10-1.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 10-1.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in Section 9.5 on page 103.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Figure 10-4. WLCSP64 SAM4LS4/2 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.746	1.683
A2	GNDANA	1.246	1.683
A3	ADVREFP	0.746	1.683
A4	VDDANA	0.246	1.683
A5	PA09	-0.254	1.683
A6	PA28	-0.754	1.683
A7	PA27	-1.254	1.683
A8	PA12	-1.754	1.683
B1	PB03	1.746	1.183
B2	XIN32	1.246	1.183
B3	XOUT32	0.746	1.183
B4	PA08	0.246	1.183
B5	PB06	-0.254	1.183
B6	PA10	-0.754	1.183
B7	PA11	-1.254	1.183
B8	PA29	-1.754	1.183
C1	VDDIN	1.746	0.683
C2	PB01	1.246	0.683
C3	PA05	0.746	0.683
C4	PA06	0.246	0.683
C5	PA07	-0.254	0.683
C6	PB07	-0.754	0.683

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	-1.254	0.683
C8	GNDIO0	-1.754	0.683
D1	VDDOUT	1.746	0.183
D2	PB00	1.246	0.183
D3	PA04	0.746	0.183
D4	PB05	0.246	0.183
D5	PB12	-0.254	0.183
D6	PB08	-0.754	0.183
D7	PA14	-1.254	0.183
D8	VLCDIN	-1.754	0.183
E1	GNDIN	1.746	-0.317
E2	PA03	1.246	-0.317
E3	PB02	0.746	-0.317
E4	RESET_N	0.246	-0.317
E5	PB13	-0.254	-0.317
E6	PB09	-0.754	-0.317
E7	PA15	-1.254	-0.317
E8	PA30	-1.754	-0.317
F1	VDDCORE	1.746	-0.817
F2	TCK	1.246	-0.817
F3	PA02	0.746	-0.817
F4	PB14	0.246	-0.817

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.254	-0.817
F6	PB10	-0.754	-0.817
F7	PA16	-1.254	-0.817
F8	PA31	-1.754	-0.817
G1	GNDIO1	1.746	-1.317
G2	PA26	1.246	-1.317
G3	PA24	0.746	-1.317
G4	PA00	0.246	-1.317
G5	PA01	-0.254	-1.317
G6	PA19	-0.754	-1.317
G7	PA18	-1.254	-1.317
G8	PA17	-1.754	-1.317
H1	VDDIO1	1.746	-1.817
H2	PA25	1.246	-1.817
H3	PA23	0.746	-1.817
H4	PB15	0.246	-1.817
H5	PA21	-0.254	-1.817
H6	VDDIO0	-0.754	-1.817
H7	PA20	-1.254	-1.817
H8	PB11	-1.754	-1.817

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-11. Device and Package Maximum Weight

14.8	mg

Table 10-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

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