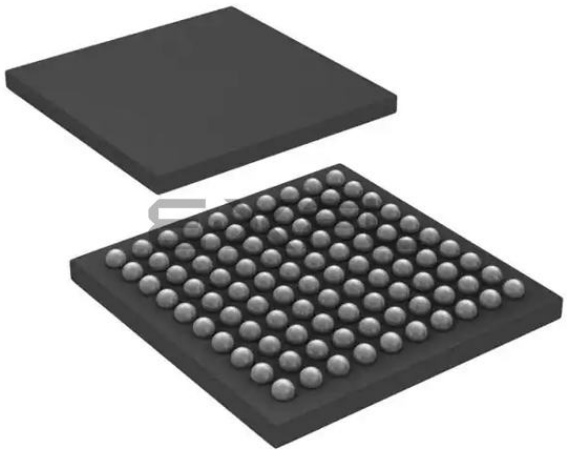

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	75
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4lc8ca-cfu

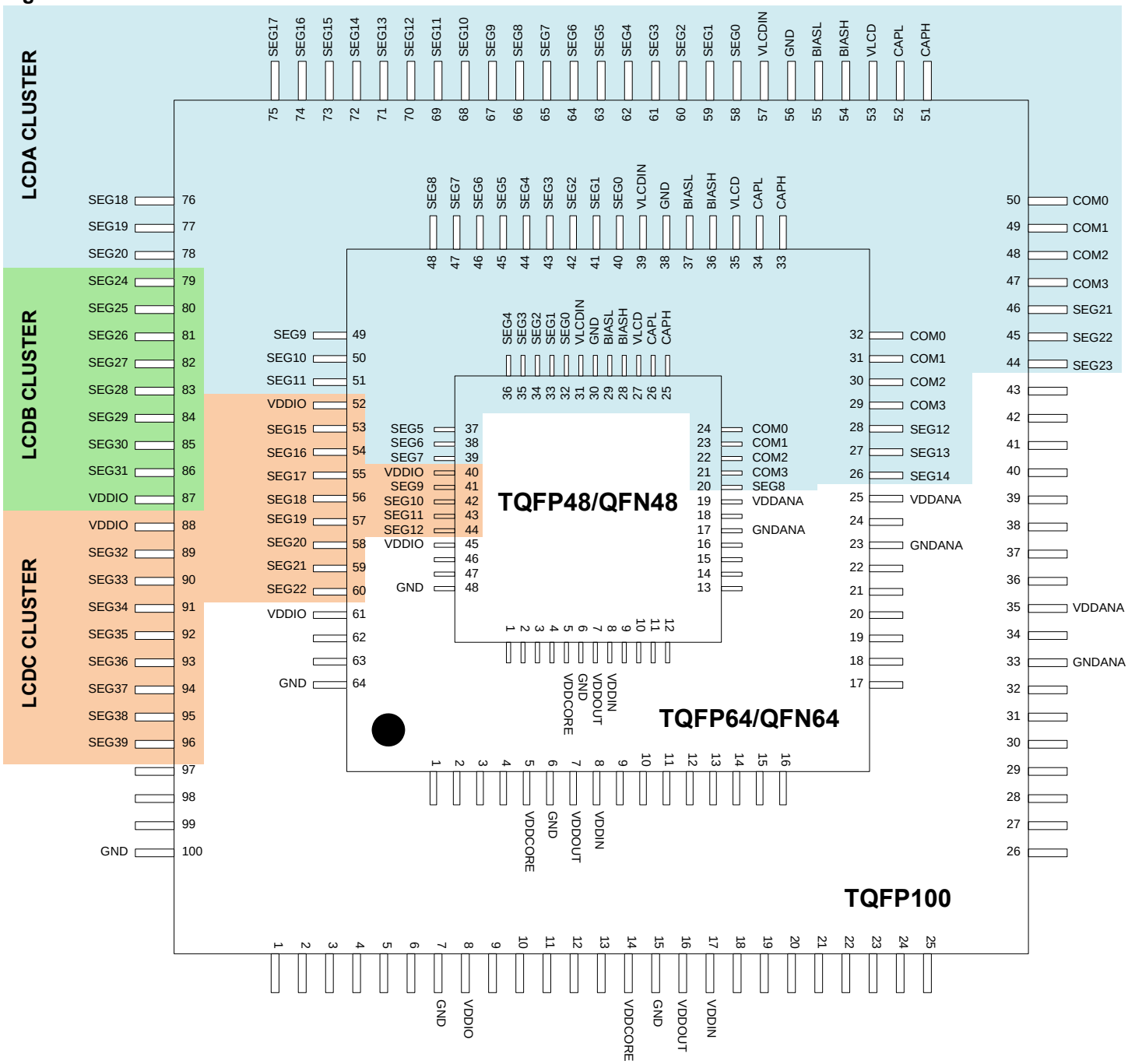
Table 3-1. 100-pin GPIO Controller Function Multiplexing (Sheet 3 of 4)

ATSAM4LC		ATSAM4LS		Pin	GPIO	Supply	GPIO Functions						
QFN	VFBGA	QFN	VFBGA				A	B	C	D	E	F	G
72	G6	72	G6	PB08	40	LCDA	USART3 CLK		GLOC IN6	TC0 B0		LCDCA SEG14	CATB SENSE28
73	G7	73	G7	PB09	41	LCDA	USART3 RXD	PEVC PAD EVT2	GLOC IN7	TC0 A1		LCDCA SEG15	CATB SENSE29
74	G8	74	G8	PB10	42	LCDA	USART3 TXD	PEVC PAD EVT3	GLOC OUT1	TC0 B1	SCIF GCLK0	LCDCA SEG16	CATB SENSE30
75	K9	75	K9	PB11	43	LCDA	USART0 CTS	SPI NPCS2		TC0 A2	SCIF GCLK1	LCDCA SEG17	CATB SENSE31
89	E7	89	E7	PB12	44	LCDC	USART0 RTS	SPI NPCS3	PEVC PAD EVT0	TC0 B2	SCIF GCLK2	LCDCA SEG32	CATB DIS
90	E8	90	E8	PB13	45	LCDC	USART0 CLK	SPI NPCS1	PEVC PAD EVT1	TC0 CLK0	SCIF GCLK3	LCDCA SEG33	CATB SENSE0
93	D7	93	D7	PB14	46	LCDC	USART0 RXD	SPI MISO	TWIM3 TWD	TC0 CLK1	SCIF GCLK IN0	LCDCA SEG36	CATB SENSE1
94	D8	94	D8	PB15	47	LCDC	USART0 TXD	SPI MOSI	TWIM3 TWCK	TC0 CLK2	SCIF GCLK IN1	LCDCA SEG37	CATB SENSE2
1	A10	1	A10	PC00	64	VDDIO	SPI NPCS2	USART0 CLK		TC1 A0			CATB SENSE3
2	C8	2	C8	PC01	65	VDDIO	SPI NPCS3	USART0 RTS		TC1 B0			CATB SENSE4
3	C7	3	C7	PC02	66	VDDIO	SPI NPCS1	USART0 CTS	USART0 RXD	TC1 A1			CATB SENSE5
4	B7	4	B7	PC03	67	VDDIO	SPI NPCS0	EIC EXTINT5	USART0 TXD	TC1 B1			CATB SENSE6
9	C5	9	C5	PC04	68	VDDIO	SPI MISO	EIC EXTINT6		TC1 A2			CATB SENSE7
10	C6	10	C6	PC05	69	VDDIO	SPI MOSI	EIC EXTINT7		TC1 B2			CATB DIS
11	B6	11	B6	PC06	70	VDDIO	SPI SCK	EIC EXTINT8		TC1 CLK0			CATB SENSE8
36	F2	36	F2	PC07	71	VDDANA	ADCIFE AD7	USART2 RTS	PEVC PAD EVT0	TC1 CLK1			CATB SENSE9
37	E3	37	E3	PC08	72	VDDANA	ADCIFE AD8	USART2 CLK	PEVC PAD EVT1	TC1 CLK2	USART2 CTS		CATB SENSE10
38	F1	38	F1	PC09	73	VDDANA	ADCIFE AD9	USART3 RXD	ABDACB DAC0	IISC ISCK	ACIFC ACAN1		CATB SENSE11
39	D4	39	D4	PC10	74	VDDANA	ADCIFE AD10	USART3 TXD	ABDACB DACN0	IISC ISDI	ACIFC ACAP1		CATB SENSE12
40	E4	40	E4	PC11	75	VDDANA	ADCIFE AD11	USART2 RXD	PEVC PAD EVT2				CATB SENSE13
41	F3	41	F3	PC12	76	VDDANA	ADCIFE AD12	USART2 TXD	ABDACB CLK	IISC IWS			CATB SENSE14
42	F4	42	F4	PC13	77	VDDANA	ADCIFE AD13	USART3 RTS	ABDACB DAC1	IISC ISDO	ACIFC ACBN1		CATB SENSE15
43	G1	43	G1	PC14	78	VDDANA	ADCIFE AD14	USART3 CLK	ABDACB DACN1	IISC IMCK	ACIFC ACBP1		CATB DIS
58	J5	58	J5	PC15	79	LCDA	TC1 A0			GLOC IN4		LCDCA SEG0	CATB SENSE16

Table 3-8. Signal Descriptions List (Sheet 2 of 4)

Signal Name	Function	Type	Active Level	Comments
Inter-IC Sound (I2S) Controller - IISC				
IMCK	I2S Master Clock	Output		
ISCK	I2S Serial Clock	I/O		
ISDI	I2S Serial Data In	Input		
ISDO	I2S Serial Data Out	Output		
IWS	I2S Word Select	I/O		
LCD Controller - LCDCA				
BIASL	Bias voltage (1/3 VLCD)	Analog		
BIASH	Bias voltage (2/3 VLCD)	Analog		
CAPH	High voltage end of flying capacitor	Analog		
CAPL	Low voltage end of flying capacitor	Analog		
COM3 - COM0	Common terminals	Analog		
SEG39 - SEG0	Segment terminals	Analog		
VLCD	Bias voltage	Analog		
Parallel Capture - PARC				
PCCK	Clock	Input		
PCDATA7 - PCDATA0	Data lines	Input		
PCEN1	Data enable 1	Input		
PCEN2	Data enable 2	Input		
Peripheral Event Controller - PEVC				
PAD_EVT3 - PAD_EVT0	Event Inputs	Input		
Power Manager - PM				
RESET_N	Reset	Input	Low	
System Control Interface - SCIF				
GCLK3 - GCLK0	Generic Clock Outputs	Output		
GCLK_IN1 - GCLK_IN0	Generic Clock Inputs	Input		
XIN0	Crystal 0 Input	Analog/ Digital		
XOUT0	Crystal 0 Output	Analog		
Serial Peripheral Interface - SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS3 - NPCS0	SPI Peripheral Chip Selects	I/O	Low	
SCK	Clock	I/O		
Timer/Counter - TC0, TC1				

Figure 6-5. LCD clusters in the device

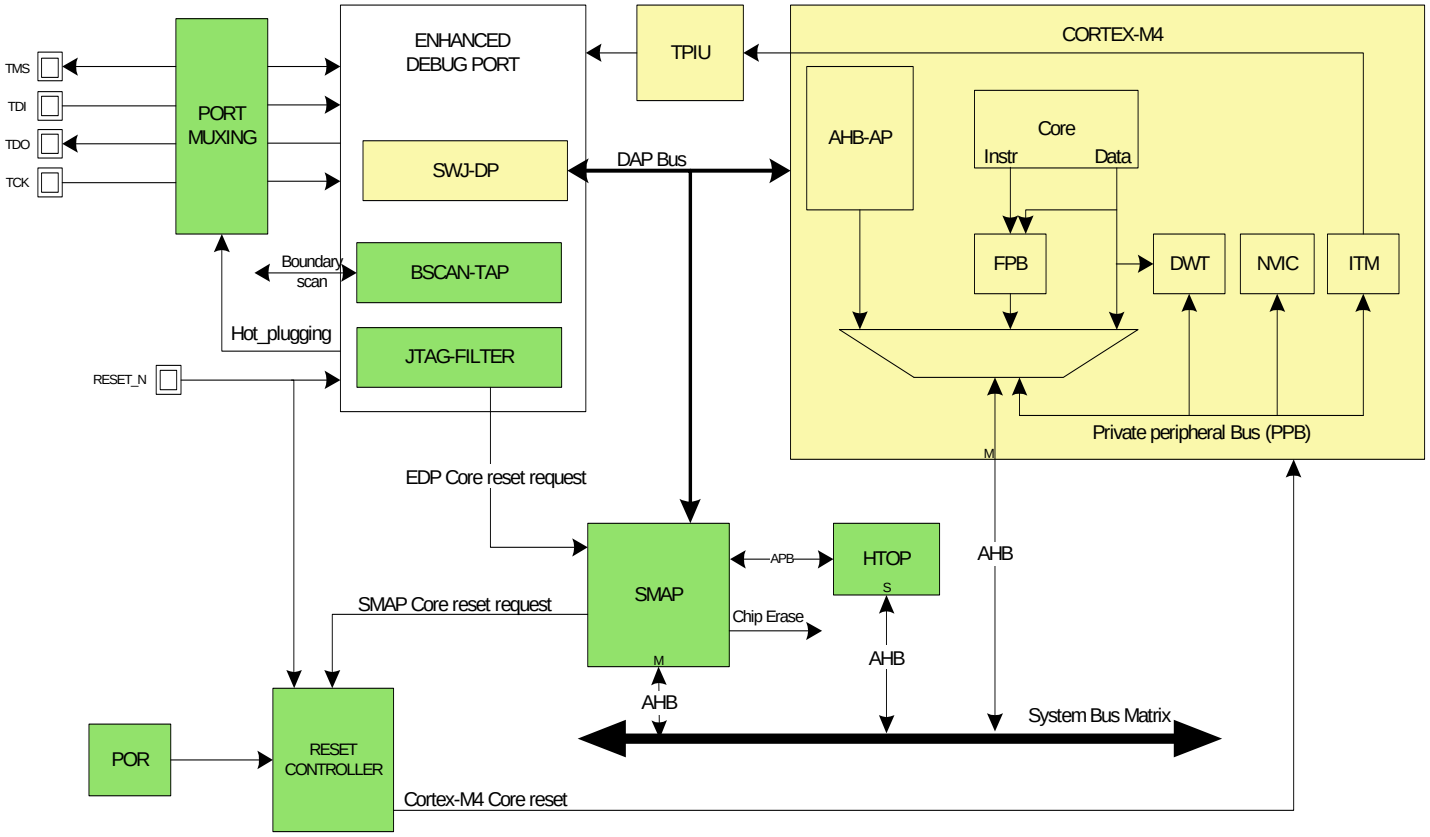


6.2.3.2 *Internal LCD Voltage*

In this mode the LCD voltages are internally generated. Depending of the number of segments required by the application, LCDB and LDCC clusters VDDIO pin must be unconnected (nc) or

8.3 Block diagram

Figure 8-1. Debug and Test Block Diagram



note: Boxes with a plain corner are SAM4L specific.

8.4 I/O Lines Description

Refer to Section 1.1.4 ”I/O Lines Description” on page 4.

  - Fix the ATB ID to 1
- Write 0x1 into the Trace Enable Register:
  - Enable the Stimulus port 0
- Write 0x1 into the Trace Privilege Register:
  - Stimulus port 0 only accessed in privileged mode (Clearing a bit in this register will result in the corresponding stimulus port being accessible in user mode.)
- Write into the Stimulus port 0 register: TPIU (Trace Port Interface Unit)

  The TPIU acts as a bridge between the on-chip trace data and the Instruction Trace Macrocell (ITM).

  The TPIU formats and transmits trace data off-chip at frequencies asynchronous to the core.

Asynchronous Mode:

The TPIU is configured in asynchronous mode, trace data are output using the single TRACESWO pin. The TRACESWO signal is multiplexed with the TDO signal of the JTAG Debug Port. As a consequence, asynchronous trace mode is only available when the Serial Wire Debug mode is selected since TDO signal is used in JTAG debug mode.

Two encoding formats are available for the single pin output:

- Manchester encoded stream. This is the reset value.
- NRZ_based UART byte structure

5.4.3. How to Configure the TPIU

This example only concerns the asynchronous trace mode.

- Set the TRCENA bit to 1 into the Debug Exception and Monitor Register (0xE000EDFC) to enable the use of trace and debug blocks.
- Write 0x2 into the Selected Pin Protocol Register
  - Select the Serial Wire Output – NRZ
- Write 0x100 into the Formatter and Flush Control Register
- Set the suitable clock prescaler value into the Async Clock Prescaler Register to scale the baud rate of the asynchronous output (this can be done automatically by the debugging tool).

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. Return to Run-Test/Idle.
5. Select the DR Scan path.
6. In Capture-DR: The Data on the external pins are sampled into the boundary-scan chain.
7. In Shift-DR: The boundary-scan chain is shifted by the TCK input.
8. Return to Run-Test/Idle.

Table 8-6. SAMPLE_PRELOAD Details

Instructions	Details
IR input value	**0001** (0x1)
IR output value	p00s
DR Size	Depending on boundary-scan chain, see BSDL-file.
DR input value	Depending on boundary-scan chain, see BSDL-file.
DR output value	Depending on boundary-scan chain, see BSDL-file.

8.7.14.3 INTEST

This instruction selects the boundary-scan chain as Data Register for testing internal logic in the device. The logic inputs are determined by the boundary-scan chain, and the logic outputs are captured by the boundary-scan chain. The device output pins are driven from the boundary-scan chain.

Starting in Run-Test/Idle, the INTEST instruction is accessed the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. In Update-IR: The data from the boundary-scan chain is applied to the internal logic inputs.
5. Return to Run-Test/Idle.
6. Select the DR Scan path.
7. In Capture-DR: The data on the internal logic is sampled into the boundary-scan chain.
8. In Shift-DR: The boundary-scan chain is shifted by the TCK input.
9. In Update-DR: The data from the boundary-scan chain is applied to internal logic inputs.
10. Return to Run-Test/Idle.

Table 8-7. INTEST Details

Instructions	Details
IR input value	**0100** (0x4)
IR output value	p001
DR Size	Depending on boundary-scan chain, see BSDL-file.
DR input value	Depending on boundary-scan chain, see BSDL-file.
DR output value	Depending on boundary-scan chain, see BSDL-file.

8.9.11.3 Status Clear Register

Name: SCR

Access Type: Write-Only

Offset: 0x08

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	LCK	FAIL	BERR	HCR	DONE

Writing a zero to a bit in this register has no effect.
Writing a one to a bit clears the corresponding SR bit

Note: *Writing a one to bit HCR while the chip is in protected state has no effect*

8.9.11.4 Address Register

Name: ADDR

Access Type: Read/Write

Offset: 0x0C

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
ADDR							

23	22	21	20	19	18	17	16
ADDR							

15	14	13	12	11	10	9	8
ADDR							

7	6	5	4	3	2	1	0
ADDR						-	-

- **ADDR: Address Value**
  Addess values are always world aligned

8.9.11.6 Data Register

Name: DATA

Access Type: Read/Write

Offset: 0x14

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DATA							

23	22	21	20	19	18	17	16
DATA							

15	14	13	12	11	10	9	8
DATA							

7	6	5	4	3	2	1	0
DATA							

- **DATA: Generic data register**

8.9.11.10 Identification Register

Name: IDR

Access Type: Read-Only

Offset: 0xFC

Reset Value: -

31	30	29	28	27	26	25	24
REVISION				CC			

23	22	21	20	19	18	17	16
IC							CLSS

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
APID				APIDV			

- **REVISION: Revision**
- **CC: JEP-106 Continuation Code**
  Atmel continuation code is 0x0
- **IC: JEP-106 Identity Code**
  Atmel identification code is 0x1F
- **CLSS: Class**
  0: This AP is not a Memory Access Port
  1: This AP is a Memory Access Port
- **APID: AP Identification**
- **APIDV: AP Identification Variant**

For more information about this register, refer to the ARM Debug Interface v5.1 Architecture Specification document.

Table 9-7. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
SLEEP0	Switching mode	25°C	9 * Main clock cycles	3817	4033	µA
		85°C		4050	4507	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	2341	2477	
		85°C		2525	2832	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	1758	1862	
		85°C		1925	1971	
SLEEP3	Linear mode	25°C		51	60	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	6.7		
	OSC32K and AST stopped Fast wake-up enable			5.5		
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.9		
	AST and OSC32K stopped			3.0		
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

9.5.2 Power Scaling 1

The values in Table 34-7 are measured values of power consumption under the following conditions, except where noted:

- Operating conditions for power scaling mode 1
  - V_{VDDIN} = 3.3V
- Wake up time from low power modes is measured from the edge of the wakeup signal to the first instruction fetched in flash.
- Oscillators
  - OSC0 (crystal oscillator) and OSC32K (32kHz crystal oscillator) stopped
  - RCFAST Running at 12MHz
- Clocks
  - RCFAST used as main clock source
  - CPU, AHB clocks undivided
  - APBC and APBD clocks divided by 4
  - APBA and APBB bridges off
  - The following peripheral clocks running
    - PM, SCIF, AST, FLASHCALW, APBC and APBD bridges

9.5.3 Peripheral Power Consumption in Power Scaling mode 0 and 2

The values in Table 9-11 are measured values of power consumption under the following conditions:

- Operating conditions, internal core supply (Figure 9-2)
  - V_{VDDIN} = 3.3V
  - $V_{VDDCORE}$ supplied by the internal regulator in switching mode
- T_A = 25°C
- Oscillators
  - OSC0 (crystal oscillator) stopped
  - OSC32K (32KHz crystal oscillator) running with external 32KHz crystal
  - DFLL running at 48MHz with OSC32K as reference clock
- Clocks
  - DFLL used as main clock source
  - CPU, AHB, and PB clocks undivided
- I/Os are inactive with internal pull-up
- Flash enabled in high speed mode
- CPU in SLEEP0 mode
- BOD18 and BOD33 disabled

Consumption active is the added current consumption when the module clock is turned on.

3. These values are based on characterization. These values are not covered by test limits in production

9.6.2 High-drive I/O Pin : PA02, PC04, PC05, PC06

Table 9-14. High-drive I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.8	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			22	MHz
		OSRR0=1				17	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			35	MHz
		OSRR0=1				26	MHz
I_{LEAK}	Input leakage current(3)	Pull-up resistors disabled			0.01	2	µA
C_{IN}	Input capacitance(2)				10		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.6.5 High Drive TWI Pin : PB00, PB01

Table 9-19. High Drive TWI Pin Characteristics in TWI configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)	PB00, PB01			40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.3 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.7 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	DRIVEL=0				0.5	mA
		DRIVEL=1				1.0	
		DRIVEL=2				1.6	
		DRIVEL=3				3.1	
		DRIVEL=4				6.2	
		DRIVEL=5				9.3	
		DRIVEL=6				15.5	
		DRIVEL=7				21.8	
I_{CS}	Current Source(2)	DRIVEH=0			0.5		mA
		DRIVEH=1			1		
		DRIVEH=2			1.5		
		DRIVEH=3			3		
f_{MAX}	Max frequency(2)	HsMode with Current source; DRIVEx=3, SLEW=0 Cbus = 400pF, V_{VDD} = 1.68V		3.5	6.4		MHz
t_{RISE}	Rise time(2)	HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			28	38	ns
t_{FALL}	Fall time(2)	Standard Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	ns
		HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.7 Oscillator Characteristics

9.7.1 Oscillator 0 (OSC0) Characteristics

9.7.1.1 Digital Clock Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN.

Table 9-22. Digital Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CPXIN}	XIN clock frequency (1)				50	MHz
t_{CPXIN}	XIN clock duty cycle(1)		40		60	%
$t_{STARTUP}$	Startup time			N/A		cycles

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.7.1.2 Crystal Oscillator Characteristics

The following table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT as shown in Figure 9-3. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can be found in the crystal datasheet. The capacitance of the external capacitors (C_{LEXT}) can then be computed as follows:

$$C_{LEXT} = 2(C_L - C_{STRAY} - C_{SHUNT})$$

where C_{STRAY} is the capacitance of the pins and PCB, C_{SHUNT} is the shunt capacitance of the crystal.

Table 9-23. Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Crystal oscillator frequency (1)		0.6		30	MHz
ESR	Crystal Equivalent Series Resistance (2)	f = 0.455MHz, C_{LEXT} = 100pF SCIF.OSCCTRL.GAIN = 0			17000	Ω
		f = 2MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 0			2000	
		f = 4MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 1			1500	
		f = 8MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 2			300	
		f = 16MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 3			350	
		f = 30MHz, C_{LEXT} = 18pF SCIF.OSCCTRL.GAIN = 4			45	

9.7.7 1MHz RC Oscillator (RC1M) Characteristics

Table 9-30. RC1M Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)		0.91	1	1.12	MHz
I_{RC1M}	Current consumption (2)			35		µA
Duty	Duty cycle(1)		48.6	49.9	54.4	%

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.7.8 4/8/12MHz RC Oscillator (RCFAST) Characteristics

Table 9-31. RCFAST Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)	Calibrated, FRANGE=0	4	4.3	4.6	MHz
		Calibrated, FRANGE=1	7.8	8.2	8.5	
		Calibrated, FRANGE=2	11.3	12	12.3	
I_{RCFAST}	Current consumption (2)	Calibrated, FRANGE=0		90	110	µA
		Calibrated, FRANGE=1		130	150	
		Calibrated, FRANGE=2		180	205	
Duty	Duty cycle(1)	Calibrated, FRANGE=0	48.8	49.6	50.1	%
		Calibrated, FRANGE=1	47.8	49.2	50.1	
		Calibrated, FRANGE=2	46.7	48.8	50.0	
$t_{STARTUP}$	Startup time(1)	Calibrated, FRANGE=2	0.1	0.31	0.71	µs

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.7.9 80MHz RC Oscillator (RC80M) Characteristics

Table 9-32. Internal 80 MHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)	After calibration Note that RC80M is not available in PS1	60	80	100	MHz
I_{RC80M}	Current consumption (2)			330		µA
$t_{STARTUP}$	Startup time(1)		0.57	1.72	3.2	µs
Duty	Duty cycle(2)		45	50	55	%

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.8 Flash Characteristics

Table 9-33 gives the device maximum operating frequency depending on the number of flash wait states and the flash read mode. The FWS bit in the FLASHCALW FCR register controls the number of wait states used when accessing the flash memory.

Table 9-33. Maximum Operating Frequency (1)

PowerScaling Mode	Flash Read Mode	Flash Wait States	Maximum Operating Frequency	Unit
0	Low power (HSDIS) + Flash internal reference: BPM.PMCON.FASTWKUP=1	1	12	MHz
	Low power(HSDIS)	0	18	
		1	36	
1	Low power (HSDIS) + Flash internal reference: BPM.PMCON.FASTWKUP=1	1	12	
	Low power (HSDIS)	0	8	
		1	12	
2	High speed (HSEN)	0	24	
		1	48	

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-34. Flash Characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FPP}	Page programming time	f_{CLK_AHB} = 48MHz		4.38		ms
t_{FPE}	Page erase time			4.38		
t_{FFP}	Fuse programming time			0.63		
t_{FEA}	Full chip erase time (EA)			5.66		
t_{FCE}	JTAG chip erase time (CHIP_ERASE)	f_{CLK_AHB} = 115kHz		304		

9.9.4 Analog- to Digital Converter Characteristics

Table 9-45. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Temperature range		-40		+85	°C
	Resolution (1)	Max		12	12 (2)	Bit
	Sampling clock (3)	Differential modes, Gain=1X	5		300	kHz
		Unipolar modes, Gain=1X	5		250	
f_{ADC}	ADC clock frequency(3)	Differential modes	0.03		1.8	MHz
		Unipolar modes	0.03		1.5	
$T_{SAMPLEHOLD}$	Sampling time(3)	Differential modes	16.5		277	µs
		Unipolar modes	16.5		333	
	Conversion rate(1)	1X gain, differential			300	kSps
	Internal channel conversion rate(3)	V_{VDD}/10, Bandgap and Temperature channels			125	kSps
	Conversion time (latency) Differential mode (no windowing)	1X gain, (resolution/2)+gain (4)			6	Cycles
		2X and 4X gain			7	
		8X and 16X gain			8	
		32X and 64X gain			9	
		64X gain and unipolar			10	

1. These values are based on characterization. These values are not covered by test limits in production
2. Single ended or using divide by two max resolution: 11 bits
3. These values are based on simulation. These values are not covered by test limits in production
4. See Figure 9-5

Figure 9-5. Maximum input common mode voltage

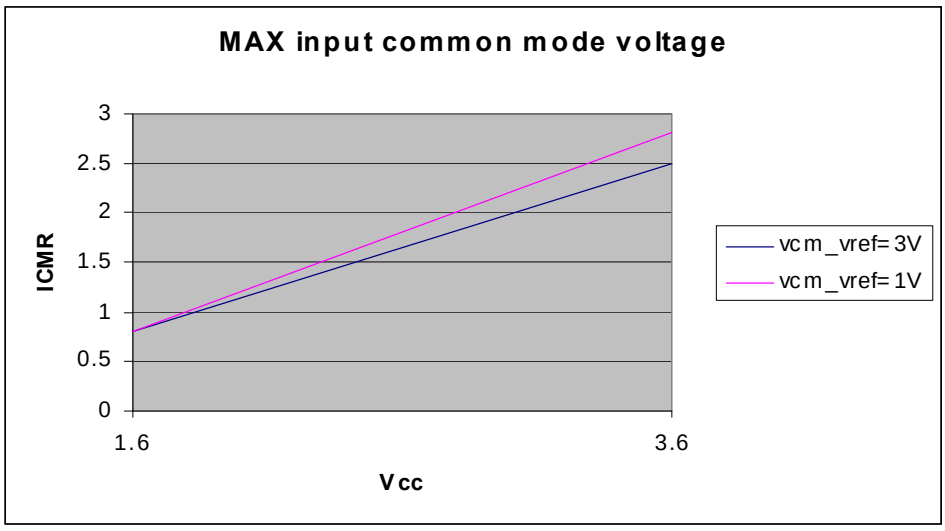


Table 9-48. Unipolar mode, gain=1

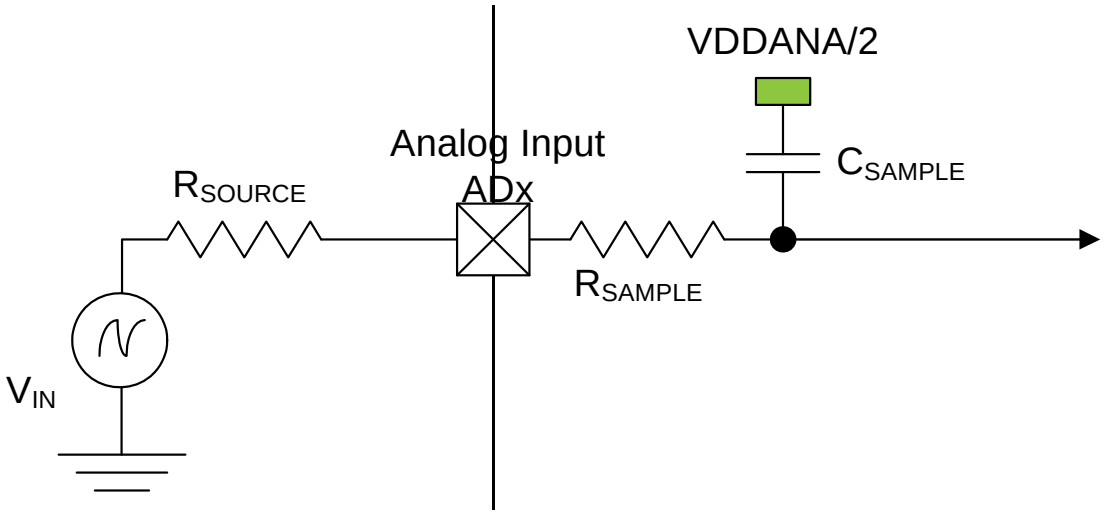
	PSRR[1]	fVdd=100kHz, VDDIO=3.6V		62		dB
		fVdd=1MHz, VDDIO=3.6V		49		
	DC supply current[1]	VDDANA=3.6V		1	2	mA
		VDDANA=1.6V, ADVREFP=1.0V		1	1.3	

1. These values are based on simulation. These values are not covered by test limits in production or characterization.
2. These values are based on characterization and not tested in production, and valid for an input voltage between 10% to 90% of reference voltage.

9.9.4.1 *Inputs and Sample and Hold Acquisition Times*

The analog voltage source must be able to charge the sample and hold (S/H) capacitor in the ADC in order to achieve maximum accuracy. Seen externally the ADC input consists of a resistor (R_{SAMPLE}) and a capacitor (C_{SAMPLE}). In addition, the source resistance (R_{SOURCE}) must be taken into account when calculating the required sample and hold time. Figure 9-6 shows the ADC input channel equivalent circuit.

Figure 9-6. ADC Input



To achieve *n* bits of accuracy, the C_{SAMPLE} capacitor must be charged at least to a voltage of

$$V_{CSAMPLE} \geq V_{IN} \times (1 - 2^{-(n+1)})$$

The minimum sampling time $t_{SAMPLEHOLD}$ for a given R_{SOURCE} can be found using this formula:

$$t_{SAMPLEHOLD} \geq (R_{SAMPLE} + R_{SOURCE}) \times (C_{SAMPLE}) \times (n+1) \times \ln(2)$$

for a 12 bits accuracy : $t_{SAMPLEHOLD} \geq (R_{SAMPLE} + R_{SOURCE}) \times (C_{SAMPLE}) \times 9,02$

where

$$t_{SAMPLEHOLD} = \frac{1}{2 \times fADC}$$

Figure 9-16. SPI Slave Mode, NPCS Timing

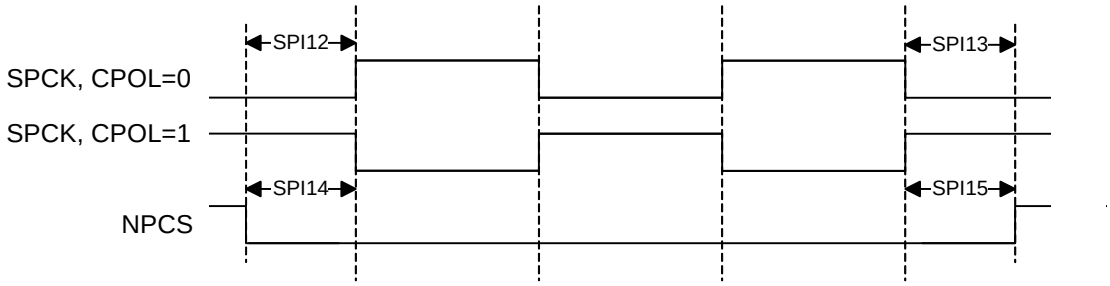


Table 9-63. SPI Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
SPI6	SPCK falling to MISO delay	V_{VDDIO} from 2.85V to 3.6V, maximum external capacitor = 40pF	19	47	ns
SPI7	MOSI setup time before SPCK rises		0		
SPI8	MOSI hold time after SPCK rises		5.4		
SPI9	SPCK rising to MISO delay		19	46	
SPI10	MOSI setup time before SPCK falls		0		
SPI11	MOSI hold time after SPCK falls		5.3		
SPI12	NPCS setup time before SPCK rises		4		
SPI13	NPCS hold time after SPCK falls		2.5		
SPI14	NPCS setup time before SPCK falls		6		
SPI15	NPCS hold time after SPCK rises		1.1		

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{CLKSPI}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, SPI7 + SPI8 or SPI10 + SPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$