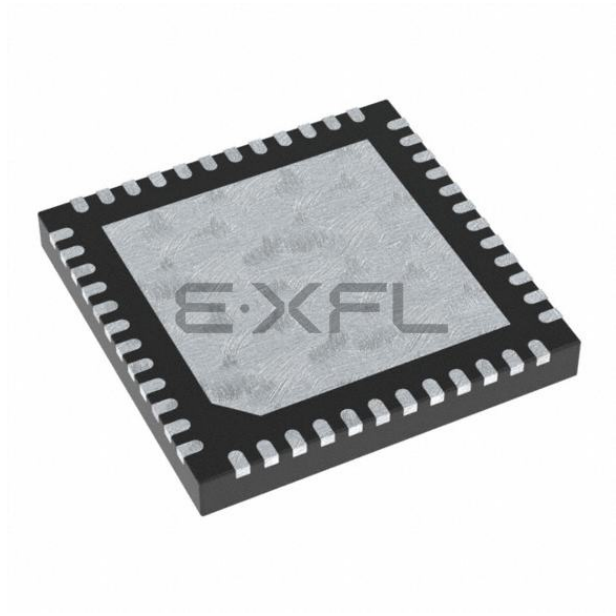

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	32
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 3x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls2aa-mu

Table 3-1. 100-pin GPIO Controller Function Multiplexing (Sheet 4 of 4)

ATSAM4LC		ATSAM4LS		Pin	GPIO	Supply	GPIO Functions						
QFN	VFBGA	QFN	VFBGA				A	B	C	D	E	F	G
59	J6	59	J6	PC16	80	LCDA	TC1 B0			GLOC IN5		LCDCA SEG1	CATB SENSE17
60	H4	60	H4	PC17	81	LCDA	TC1 A1			GLOC IN6		LCDCA SEG2	CATB SENSE18
61	K6	61	K6	PC18	82	LCDA	TC1 B1			GLOC IN7		LCDCA SEG3	CATB SENSE19
62	G4	62	G4	PC19	83	LCDA	TC1 A2			GLOC OUT1		LCDCA SEG4	CATB SENSE20
68	H7	68	H7	PC20	84	LCDA	TC1 B2					LCDCA SEG10	CATB SENSE21
69	K8	69	K8	PC21	85	LCDA	TC1 CLK0			PARC PCCK		LCDCA SEG11	CATB SENSE22
70	J8	70	J8	PC22	86	LCDA	TC1 CLK1			PARC PCEN1		LCDCA SEG12	CATB SENSE23
71	H8	71	H8	PC23	87	LCDA	TC1 CLK2			PARC PCEN2		LCDCA SEG13	CATB DIS
79	J9	79	J9	PC24	88	LCDB	USART1 RTS	EIC EXTINT1	PEVC PAD EVT0	PARC PCDATA0		LCDCA SEG24	CATB SENSE24
80	H9	80	H9	PC25	89	LCDB	USART1 CLK	EIC EXTINT2	PEVC PAD EVT1	PARC PCDATA1		LCDCA SEG25	CATB SENSE25
81	G9	81	G9	PC26	90	LCDB	USART1 RXD	EIC EXTINT3	PEVC PAD EVT2	PARC PCDATA2	SCIF GCLK0	LCDCA SEG26	CATB SENSE26
82	F6	82	F6	PC27	91	LCDB	USART1 TXD	EIC EXTINT4	PEVC PAD EVT3	PARC PCDATA3	SCIF GCLK1	LCDCA SEG27	CATB SENSE27
83	G10	83	G10	PC28	92	LCDB	USART3 RXD	SPI MISO	GLOC IN4	PARC PCDATA4	SCIF GCLK2	LCDCA SEG28	CATB SENSE28
84	F7	84	F7	PC29	93	LCDB	USART3 TXD	SPI MOSI	GLOC IN5	PARC PCDATA5	SCIF GCLK3	LCDCA SEG29	CATB SENSE29
85	F8	85	F8	PC30	94	LCDB	USART3 RTS	SPI SCK	GLOC IN6	PARC PCDATA6	SCIF GCLK IN0	LCDCA SEG30	CATB SENSE30
86	F9	86	F9	PC31	95	LCDB	USART3 CLK	SPI NPCS0	GLOC OUT1	PARC PCDATA7	SCIF GCLK IN1	LCDCA SEG31	CATB SENSE31

Table 3-2. 64-pin GPIO Controller Function Multiplexing (Sheet 1 of 3)

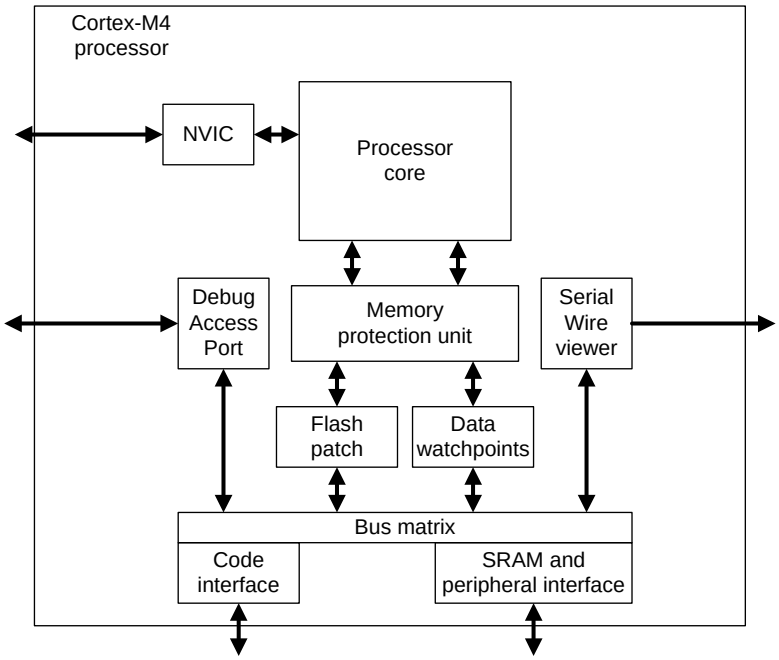
ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
QFP QFN	QFP QFN				A	B	C	D	E	F	G
1	1	PA00	0	VDDIO							
2	2	PA01	1	VDDIO							
3	3	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
10	10	PA03	3	VDDIN		SPI MISO					

4. Cortex-M4 processor and core peripherals

4.1 Cortex-M4

The Cortex-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- **outstanding processing performance combined with fast interrupt handling**
- **enhanced system debug with extensive breakpoint and trace capabilities**
- **efficient processor core, system and memories**
- **ultra-low power consumption with integrated sleep modes**
- **platform security robustness, with integrated memory protection unit (MPU).**



The Cortex-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division.

To facilitate the design of cost-sensitive devices, the Cortex-M4 processor implements tightly-coupled system components that reduce processor area while significantly improving interrupt handling and system debug capabilities. The Cortex-M4 processor implements a version of the Thumb® instruction set based on Thumb-2 technology, ensuring high code density and reduced program memory requirements. The Cortex-M4 instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers.

The Cortex-M4 processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC includes a *non-maskable interrupt* (NMI), and provides up to 80 interrupt priority levels. The tight integration of the proces-

5.2 Embedded Memories

- **Internal high-speed flash**
  - **512Kbytes (ATSAM4Lx8)**
  - **256Kbytes (ATSAM4Lx4)**
  - **128Kbytes (ATSAM4Lx2)**
    - **Pipelined flash architecture, allowing burst reads from sequential flash locations, hiding penalty of 1 wait state access**
    - **Pipelined flash architecture typically reduces the cycle penalty of 1 wait state operation compared to 0 wait state operation**
    - **100 000 write cycles, 15-year data retention capability**
    - **Sector lock capabilities, bootloader protection, security bit**
    - **32 fuses, erased during chip erase**
    - **User page for data to be preserved during chip erase**
- **Internal high-speed SRAM, single-cycle access at full speed**
  - **64Kbytes (ATSAM4Lx8)**
  - **32Kbytes (ATSAM4Lx4, ATSAM4Lx2)**

5.3 Physical Memory Map

The system bus is implemented as a bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even during boot. The 32-bit physical address space is mapped as follows:

Table 5-1. ATSAM4L8/L4/L2 Physical Memory Map

Memory	Start Address	Size	Size
		ATSAM4Lx4	ATSAM4Lx2
Embedded Flash	0x00000000	256Kbytes	128Kbytes
Embedded SRAM	0x20000000	32Kbytes	32Kbytes
Cache SRAM	0x21000000	4Kbytes	4Kbytes
Peripheral Bridge A	0x40000000	64Kbytes	64Kbytes
Peripheral Bridge B	0x400A0000	64Kbytes	64Kbytes
AESA	0x400B0000	256 bytes	256 bytes
Peripheral Bridge C	0x400E0000	64Kbytes	64Kbytes
Peripheral Bridge D	0x400F0000	64Kbytes	64Kbytes

Memory	Start Address	Size
		ATSAM4Lx8
Embedded Flash	0x00000000	512Kbytes
Embedded SRAM	0x20000000	64Kbytes
Cache SRAM	0x21000000	4Kbytes
Peripheral Bridge A	0x40000000	64Kbytes
Peripheral Bridge B	0x400A0000	64Kbytes

At power-up or after a reset, the ATSAM4L8/L4/L2 is in the RUN0 mode. Only the necessary clocks are enabled allowing software execution. The Power Manager (PM) can be used to adjust the clock frequencies and to enable and disable the peripheral clocks.

When the CPU is entering a Power Save Mode, the CPU stops executing code. The user can choose between four Power Save Modes to optimize power consumption:

- SLEEP mode: the Cortex-M4 core is stopped, optionally some clocks are stopped, peripherals are kept running if enabled by the user.
- WAIT mode: all clock sources are stopped, the core and all the peripherals are stopped except the modules running with the 32kHz clock if enabled. This is the lowest power configuration where SleepWalking is supported.
- RETENTION mode: similar to the WAIT mode in terms of clock activity. This is the lowest power configuration where the logic is retained.
- BACKUP mode: the Core domain is powered off, the Backup domain is kept powered.

A wake up source exits the system to the RUN mode from which the Power Save Mode was entered.

A reset source always exits the system from the Power Save Mode to the RUN0 mode.

The configuration of the I/O lines are maintained in all Power Save Modes. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677.

7.1.1 SLEEP mode

The SLEEP mode allows power optimization with the fastest wake up time.

The CPU is stopped. To further reduce power consumption, the user can switch off modules-clocks and synchronous clock sources through the BPM.PMCON.SLEEP field (See Table 7-1). The required modules will be halted regardless of the bit settings of the mask registers in the Power Manager (PM.AHBMASK, PM.APBxMASK).

Table 7-1. SLEEP mode Configuration

BPM.PSAVE.SLEEP	CPU clock	AHB clocks	APB clocks GCLK	Clock sources: OSC, RCFAST, RC80M, PLL, DFLL	RCSYS	OSC32K RC32K(2)	Wake up Sources
0	Stop	Run	Run	Run	Run	Run	Any interrupt
1	Stop	Stop	Run	Run	Run	Run	Any interrupt(1)
2	Stop	Stop	Stop	Run	Run	Run	Any interrupt(1)
3	Stop	Stop	Stop	Stop	Run	Run	Any interrupt(1)

Notes: 1. from modules with clock running.
2. OSC32K and RC32K will only remain operational if pre-enabled.

7.1.1.1 Entering SLEEP mode

The SLEEP mode is entered by executing the WFI instruction.

Additionally, if the SLEEPONEXIT bit in the Cortex-M4 System Control Register (SCR) is set, the SLEEP mode will also be entered when the Cortex-M4 exits the lowest priority ISR. This

  - Fix the ATB ID to 1
- Write 0x1 into the Trace Enable Register:
  - Enable the Stimulus port 0
- Write 0x1 into the Trace Privilege Register:
  - Stimulus port 0 only accessed in privileged mode (Clearing a bit in this register will result in the corresponding stimulus port being accessible in user mode.)
- Write into the Stimulus port 0 register: TPIU (Trace Port Interface Unit)

  The TPIU acts as a bridge between the on-chip trace data and the Instruction Trace Macrocell (ITM).

  The TPIU formats and transmits trace data off-chip at frequencies asynchronous to the core.

Asynchronous Mode:

The TPIU is configured in asynchronous mode, trace data are output using the single TRACESWO pin. The TRACESWO signal is multiplexed with the TDO signal of the JTAG Debug Port. As a consequence, asynchronous trace mode is only available when the Serial Wire Debug mode is selected since TDO signal is used in JTAG debug mode.

Two encoding formats are available for the single pin output:

- Manchester encoded stream. This is the reset value.
- NRZ_based UART byte structure

5.4.3. How to Configure the TPIU

This example only concerns the asynchronous trace mode.

- Set the TRCENA bit to 1 into the Debug Exception and Monitor Register (0xE000EDFC) to enable the use of trace and debug blocks.
- Write 0x2 into the Selected Pin Protocol Register
  - Select the Serial Wire Output – NRZ
- Write 0x100 into the Formatter and Flush Control Register
- Set the suitable clock prescaler value into the Async Clock Prescaler Register to scale the baud rate of the asynchronous output (this can be done automatically by the debugging tool).

8.7.5 Product Dependencies

8.7.5.1 I/O Lines

The TCK pin is dedicated to the EDP. The other debug port pins default after reset to their GPIO functionality and are automatically reassigned to the JTAG functionalities on detection of a debugger. In serial wire mode, TDI and TDO can be used as GPIO functions. Note that in serial wire mode TDO can be used as a single pin trace output.

8.7.5.2 Power Management

When a debugger is present, the connection is kept alive allowing debug operations. As a side effect, the power is never turned off. The hot plugging functionality is always available except when the system is in BACKUP Power Save Mode.

8.7.5.3 Clocks

The SWJ-DP uses the external TCK pin as its clock source. This clock must be provided by the external JTAG master device.

Some of the JTAG Instructions are used to access an Access Port (SMAP or AHB-AP). These instructions require the CPU clock to be running.

If the CPU clock is not present because the CPU is in a Power Save Mode where this clock is not provided, the Power Manager(PM) will automatically restore the CPU clock on detection of a debug access.

The RCSYS clock is used as CPU clock when the external reset is applied to ensure correct Access Port operations.

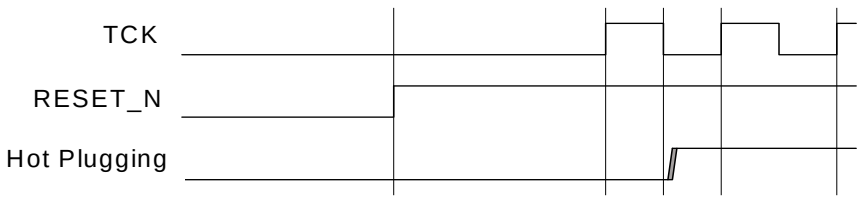
8.7.6 Module Initialization

This module is enabled as soon as a TCK falling edge is detected when RESET_N is not asserted (refer to Section 8.7.7 below). Moreover, the module is synchronously reseted as long as the TAP machine is in the TEST_LOGIC_RESET (TLR) state. It is advised asserting TMS at least 5 TCK clock periods after the debugger has been detected to ensure the module is in the TLR state prior to any operation. This module also has the ability to maintain the Cortex-M4 under reset (refer to the Section 8.7.8 ”SMAP Core Reset Request Source” on page 70).

8.7.7 Debugger Hot Plugging

The TCK pin is dedicated to the EDP. After reset has been released, the EDP detects that a debugger has been attached when a TCK falling edge arises.

Figure 8-4. Debugger Hot Plugging Detection Timings Diagram



– All other peripheral clocks stopped
- I/Os are inactive with internal pull-up
- CPU is running on flash with 1 wait state
- Low power cache enabled
- BOD18 and BOD33 disabled

Table 9-8. ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 1

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	205	224	µA/MHz
		85°C		212	231	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	213	244	
		85°C		230	270	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	95	112	
		85°C		100	119	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	100	128	
		85°C		107	138	
SLEEP0	Switching mode	25°C	9 * Main clock cycles	527	627	µA
		85°C		579	739	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	369	445	
		85°C		404	564	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	305	381	
		85°C		334	442	
SLEEP3	Linear mode	25°C		46	55	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	4.7	7.5	
	OSC32K and AST stopped Fast wake-up enable			3.5	6.3	
RETENTION	OSC32K running AST running at 1kHz		1.5µs	2.6	4.8	
	AST and OSC32K stopped			1.5	4	
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-9. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 1

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	222	240	µA/MHz
		85°C		233	276	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	233	276	
		85°C		230	270	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	100	112	
		85°C		100	119	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	104	128	
		85°C		107	138	
SLEEP0	Switching mode	25°C	9 * Main clock cycles	527	627	µA
		85°C		579	739	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	369	445	
		85°C		404	564	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	305	381	
		85°C		334	442	
SLEEP3	Linear mode	25°C		46	55	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	5.5		
	OSC32K and AST stopped Fast wake-up enable			4.3		
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.4		
	AST and OSC32K stopped			2.3		
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-10. Typical Power Consumption running CoreMark on CPU clock sources (1)

Clock Source	Conditions	Regulator	Frequency (MHz)	Typ	Unit

Table 9-16. TWI Pin Characteristics in TWI configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CS}	Current Source(3)	DRIVEH=0			0.5		mA
		DRIVEH=1			1		
		DRIVEH=2			1.5		
		DRIVEH=3			3		
f_{MAX}	Max frequency(2)	HsMode with Current source; DRIVEx=3, SLEW=0 Cbus = 400pF, V_{VDD} = 1.68V		3.5	6.4		MHz
t_{RISE}	Rise time(2)	HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			28	38	ns
t_{FALL}	Fall time(2)	Standard Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	ns
		HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Table 9-17. TWI Pin Characteristics in GPIO configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-up resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.8	mA
			2.7V<V_{VDD}<3.6V			3.5	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.6	
			2.7V<V_{VDD}<3.6V			6.8	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.8	mA
			2.7V<V_{VDD}<3.6V			3.5	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.6	
			2.7V<V_{VDD}<3.6V			6.8	

Table 9-20. High Drive TWI Pin Characteristics in GPIO configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-up resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			3.4	mA
			2.7V<V_{VDD}<3.6V			6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			5.2	mA
			2.7V<V_{VDD}<3.6V			8	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			3.4	mA
			2.7V<V_{VDD}<3.6V			6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			5.2	mA
			2.7V<V_{VDD}<3.6V			8	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		18		ns
		OSRR0=1			110		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		10		ns
		OSRR0=1			50		
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		19		ns
		OSRR0=1			140		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		12		ns
		OSRR0=1			63		

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Table 9-21. Common High Drive TWI Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LEAK}	Input leakage current (1)	Pull-up resistors disabled		0.01	2	µA
C_{IN}	Input capacitance(1)			10		pF

1. These values are based on simulation. These values are not covered by test limits in production or characterization

9.7.9 80MHz RC Oscillator (RC80M) Characteristics

Table 9-32. Internal 80 MHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)	After calibration Note that RC80M is not available in PS1	60	80	100	MHz
I_{RC80M}	Current consumption (2)			330		µA
$t_{STARTUP}$	Startup time(1)		0.57	1.72	3.2	µs
Duty	Duty cycle(2)		45	50	55	%

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.8 Flash Characteristics

Table 9-33 gives the device maximum operating frequency depending on the number of flash wait states and the flash read mode. The FWS bit in the FLASHCALW FCR register controls the number of wait states used when accessing the flash memory.

Table 9-33. Maximum Operating Frequency (1)

PowerScaling Mode	Flash Read Mode	Flash Wait States	Maximum Operating Frequency	Unit
0	Low power (HSDIS) + Flash internal reference: BPM.PMCON.FASTWKUP=1	1	12	MHz
	Low power(HSDIS)	0	18	
		1	36	
1	Low power (HSDIS) + Flash internal reference: BPM.PMCON.FASTWKUP=1	1	12	
	Low power (HSDIS)	0	8	
		1	12	
2	High speed (HSEN)	0	24	
		1	48	

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-34. Flash Characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FPP}	Page programming time	f_{CLK_AHB} = 48MHz		4.38		ms
t_{FPE}	Page erase time			4.38		
t_{FFP}	Fuse programming time			0.63		
t_{FEA}	Full chip erase time (EA)			5.66		
t_{FCE}	JTAG chip erase time (CHIP_ERASE)	f_{CLK_AHB} = 115kHz		304		

Maximum SPI Frequency, Master Output

The maximum SPI master output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn}, \frac{f_{CLKSPI} \times 2}{9})$$

Where $SPIn$ is the MOSI delay, USPI2 or USPI5 depending on CPOL and NCPHA. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Master Input

The maximum SPI master input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{1}{SPIn + t_{VALID}}, \frac{f_{CLKSPI} \times 2}{9})$$

Where $SPIn$ is the MISO setup and hold time, USPI0 + USPI1 or USPI3 + USPI4 depending on CPOL and NCPHA. T_{VALID} is the SPI slave response time. refer to the SPI slave datasheet for $T_{VALID} \cdot f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

9.10.2.2 Slave mode

Figure 9-9. USART in SPI Slave Mode with (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

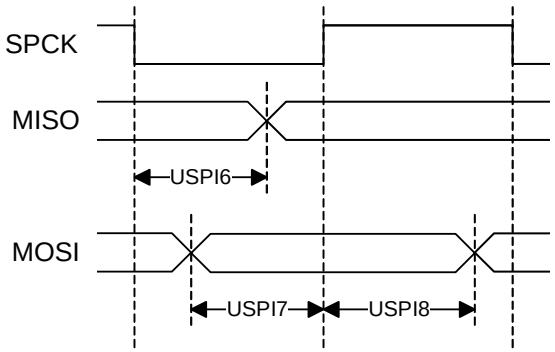


Table 9-65. JTAG Timings[1]

Symbol	Parameter	Conditions	Min	Max	Units
JTAG0	TCK Low Half-period	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF	21.8		ns
JTAG1	TCK High Half-period		8.6		
JTAG2	TCK Period		30.3		
JTAG3	TDI, TMS Setup before TCK High		2.0		
JTAG4	TDI, TMS Hold after TCK High		2.3		
JTAG5	TDO Hold Time		9.5		
JTAG6	TCK Low to TDO Valid			21.8	
JTAG7	Boundary Scan Inputs Setup Time		0.6		
JTAG8	Boundary Scan Inputs Hold Time		6.9		
JTAG9	Boundary Scan Outputs Hold Time		9.3		
JTAG10	TCK to Boundary Scan Outputs Valid			32.2	

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

9.10.6 SWD Timing

Figure 9-18. SWD Interface Signals

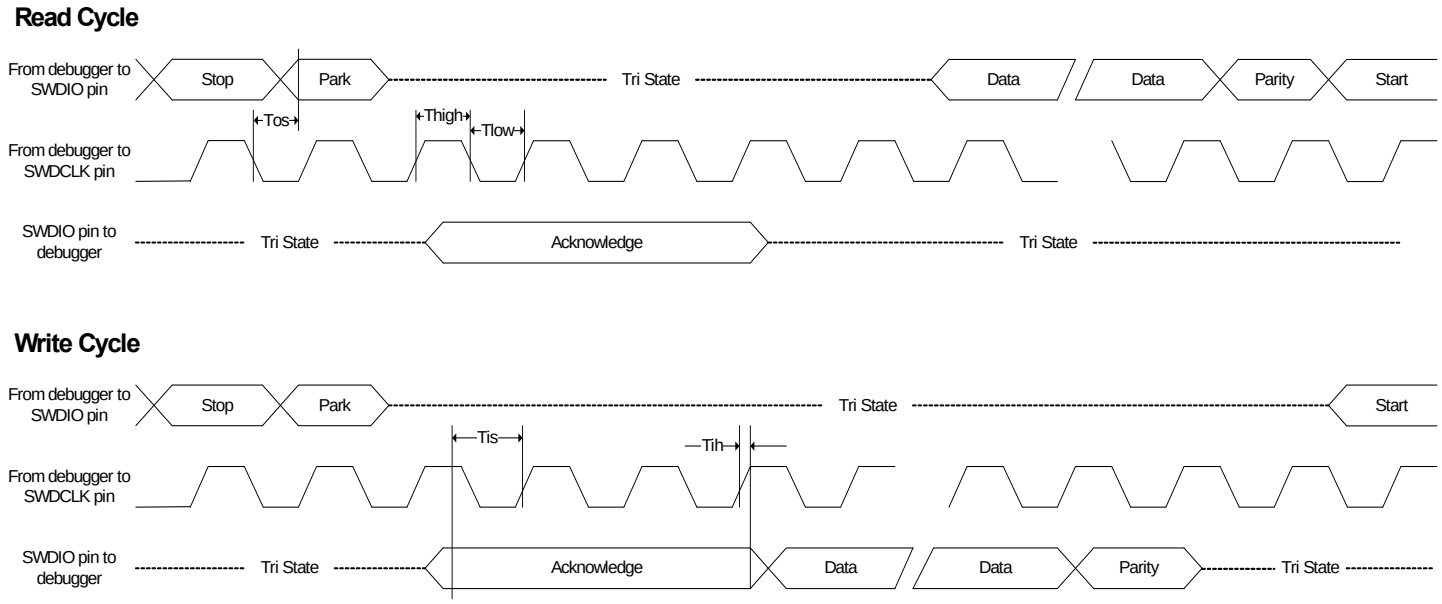


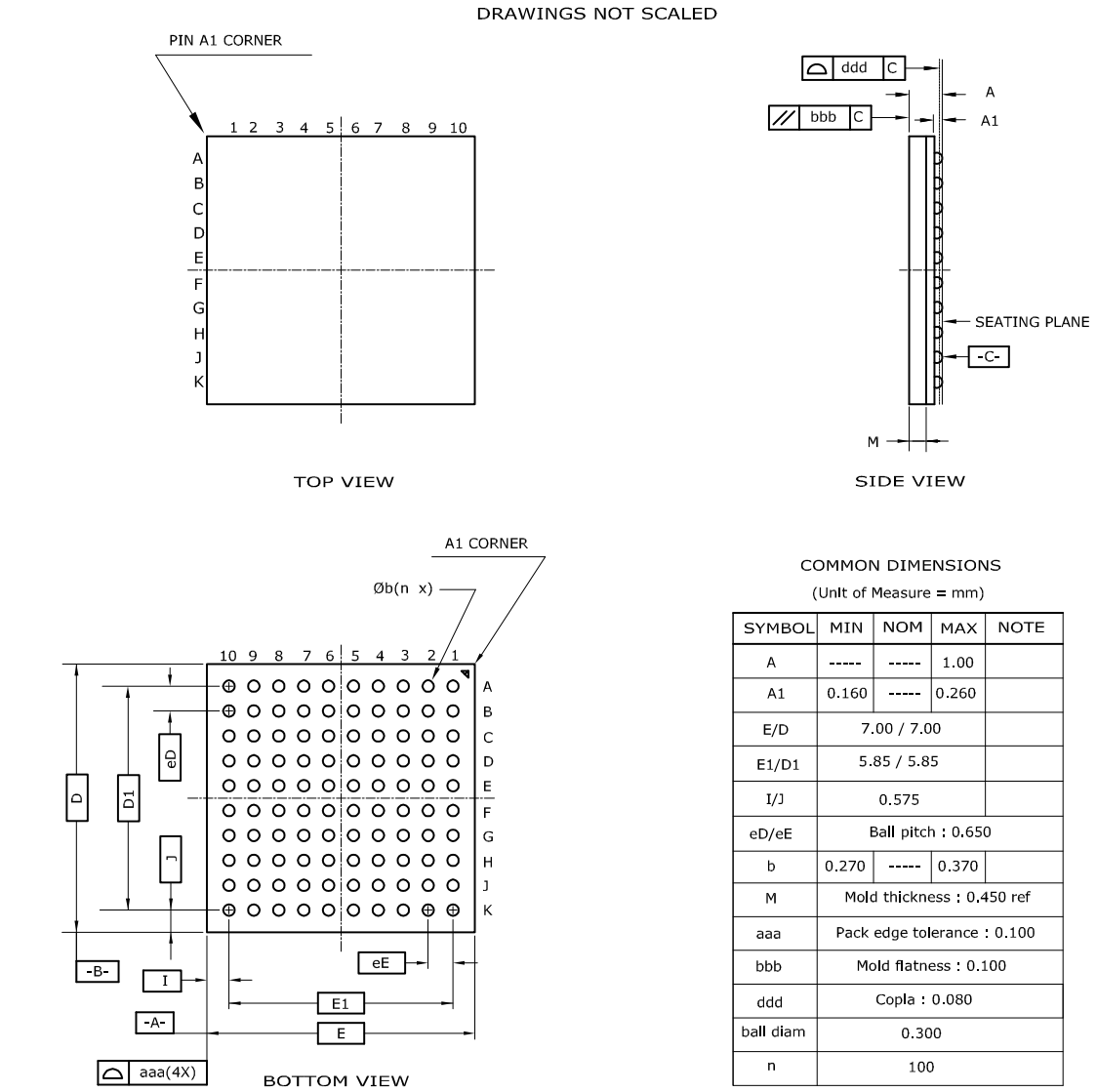
Table 9-66. SWD Timings[1]

Symbol	Parameter	Conditions	Min	Max	Units
Thigh	SWDCLK High period	V_{VDDIO} from 3.0 V to 3.6 V, maximum external capacitor = 40 pF	10	500 000	ns
Tlow	SWDCLK Low period		10	500 000	
Tos	SWDIO output skew to falling edge SWDCLK		-5	5	
Tis	Input Setup time required between SWDIO		4	-	
Tih	Input Hold time required between SWDIO and rising edge SWDCLK		1	-	

Note: 1. These values are based on simulation. These values are not covered by test limits in production or characterization.

10.2 Package Drawings

Figure 10-1. VFBGA-100 package drawing



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-----	-----	1.00	
A1	0.160	-----	0.260	
E/D	7.00 / 7.00			
E1/D1	5.85 / 5.85			
I/J	0.575			
eD/eE	Ball pitch : 0.650			
b	0.270	-----	0.370	
M	Mold thickness : 0.450 ref			
aaa	Pack edge tolerance : 0.100			
bbb	Mold flatness : 0.100			
ddd	Copla : 0.080			
ball diam	0.300			
n	100			

Notes : 1. No JEDEC Drawing Reference.
2. Array as seen from the bottom of the package.
3. Dimension A includes stand-off height A1, package body thickness, and lid height, but does not include attached features.
4. Dimension b is measured at the maximum ball diameter, parallel to primary datum C.

Table 10-2. Device and Package Maximum Weight

120	mg

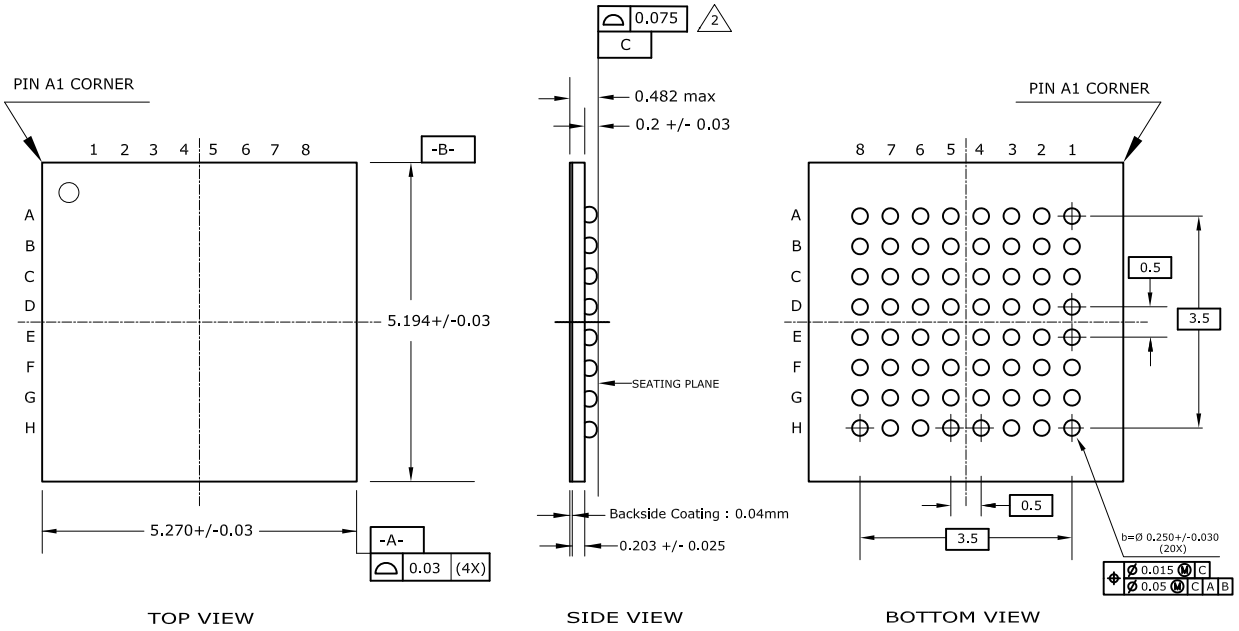
Table 10-3. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-4. Package Reference

JEDEC Drawing Reference	N/A
JESD97 Classification	E1

Figure 10-5. WLCSP64 SAM4LC8 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.75	1.75
A2	GNDANA	1.75	1.25
A3	ADVREFP	1.75	0.75
A4	VDDANA	1.75	0.25
A5	PA09	1.75	-0.25
A6	CAPL	1.75	-0.75
A7	CAPH	1.75	-1.25
A8	PA12	1.75	-1.75
B1	PB03	1.25	1.75
B2	XIN32	1.25	1.25
B3	XOUT32	1.25	0.75
B4	PA08	1.25	0.25
B5	PB06	1.25	-0.25
B6	PA10	1.25	-0.75
B7	PA11	1.25	-1.25
B8	VLCD	1.25	-1.75
C1	VDDIN	0.75	1.75
C2	PB01	0.75	1.25
C3	PA05	0.75	0.75
C4	PA06	0.75	0.25
C5	PA07	0.75	-0.25
C6	PB07	0.75	-0.75

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	0.75	-1.25
C8	BIAS1	0.75	-1.75
D1	VDDOUT	0.25	1.75
D2	PB00	0.25	1.25
D3	PA04	0.25	0.75
D4	PB05	0.25	0.25
D5	PB12	0.25	-0.25
D6	PB08	0.25	-0.75
D7	PA14	0.25	-1.25
D8	BIAS2	0.25	-1.75
E1	GNDIN	-0.25	1.75
E2	PA03	-0.25	1.25
E3	PB02	-0.25	0.75
E4	RESET_N	-0.25	0.25
E5	PB13	-0.25	-0.25
E6	PB09	-0.25	-0.75
E7	PA15	-0.25	-1.25
E8	GNDIO0	-0.25	-1.75
F1	VDDCORE	-0.75	1.75
F2	TCK	-0.75	1.25
F3	PA02	-0.75	0.75
F4	PB14	-0.75	0.25

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.75	-0.25
F6	PB10	-0.75	-0.75
F7	PA16	-0.75	-1.25
F8	VLCDIN	-0.75	-1.75
G1	GNDIO1	-1.25	1.75
G2	PA26	-1.25	1.25
G3	PA24	-1.25	0.75
G4	PA00	-1.25	0.25
G5	PA01	-1.25	-0.25
G6	PA19	-1.25	-0.75
G7	PA18	-1.25	-1.25
G8	PA17	-1.25	-1.75
H1	VDDIO1	-1.75	1.75
H2	PA25	-1.75	1.25
H3	PA23	-1.75	0.75
H4	PB15	-1.75	0.25
H5	PA21	-1.75	-0.25
H6	VDDIO0	-1.75	-0.75
H7	PA20	-1.75	-1.25
H8	PB11	-1.75	-1.75

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-14. Device and Package Maximum Weight

14.8	mg

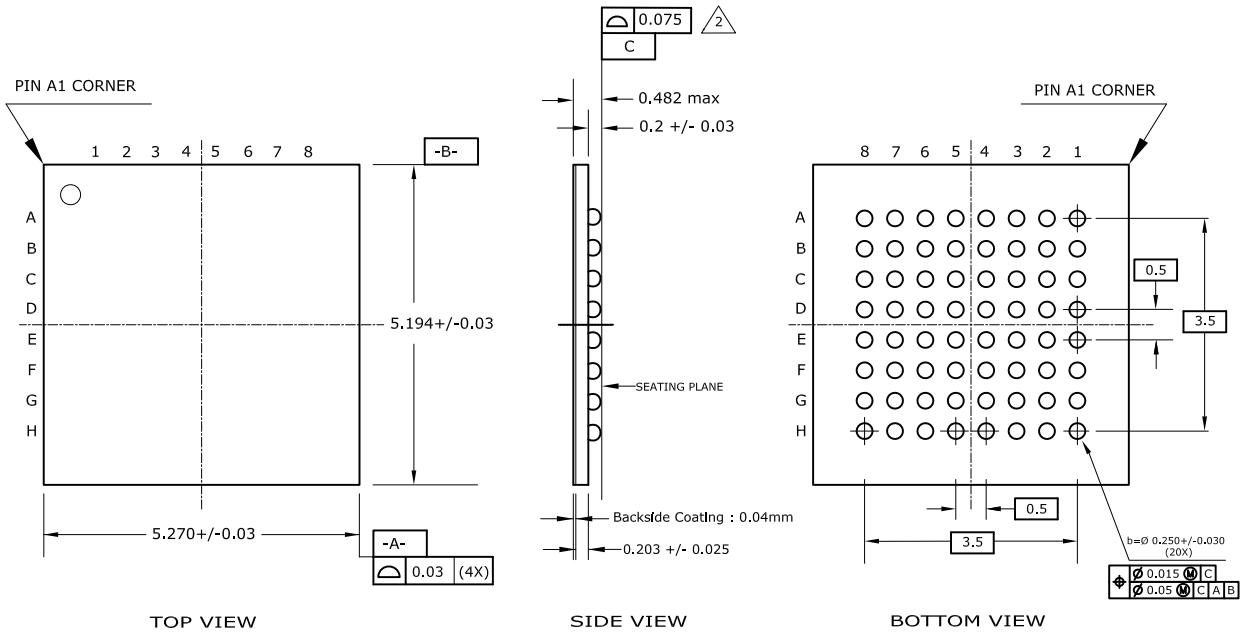
Table 10-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-16. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

Figure 10-6. WLCSP64 SAM4LS8 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.75	1.75
A2	GNDANA	1.75	1.25
A3	ADVREFP	1.75	0.75
A4	VDDANA	1.75	0.25
A5	PA09	1.75	-0.25
A6	PA28	1.75	-0.75
A7	PA27	1.75	-1.25
A8	PA12	1.75	-1.75
B1	PB03	1.25	1.75
B2	XIN32	1.25	1.25
B3	XOUT32	1.25	0.75
B4	PA08	1.25	0.25
B5	PB06	1.25	-0.25
B6	PA10	1.25	-0.75
B7	PA11	1.25	-1.25
B8	PA29	1.25	-1.75
C1	VDDIN	0.75	1.75
C2	PB01	0.75	1.25
C3	PA05	0.75	0.75
C4	PA06	0.75	0.25
C5	PA07	0.75	-0.25
C6	PB07	0.75	-0.75

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	0.75	-1.25
C8	GNDIO0	0.75	-1.75
D1	VDDOUT	0.25	1.75
D2	PB00	0.25	1.25
D3	PA04	0.25	0.75
D4	PB05	0.25	0.25
D5	PB12	0.25	-0.25
D6	PB08	0.25	-0.75
D7	PA14	0.25	-1.25
D8	VLCDIN	0.25	-1.75
E1	GNDIN	-0.25	1.75
E2	PA03	-0.25	1.25
E3	PB02	-0.25	0.75
E4	RESET_N	-0.25	0.25
E5	PB13	-0.25	-0.25
E6	PB09	-0.25	-0.75
E7	PA15	-0.25	-1.25
E8	PA30	-0.25	-1.75
F1	VDDCORE	-0.75	1.75
F2	TCK	-0.75	1.25
F3	PA02	-0.75	0.75
F4	PB14	-0.75	0.25

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.75	-0.25
F6	PB10	-0.75	-0.75
F7	PA16	-0.75	-1.25
F8	PA31	-0.75	-1.75
G1	GNDIO1	-1.25	1.75
G2	PA26	-1.25	1.25
G3	PA24	-1.25	0.75
G4	PA00	-1.25	0.25
G5	PA01	-1.25	-0.25
G6	PA19	-1.25	-0.75
G7	PA18	-1.25	-1.25
G8	PA17	-1.25	-1.75
H1	VDDIO1	-1.75	1.75
H2	PA25	-1.75	1.25
H3	PA23	-1.75	0.75
H4	PB15	-1.75	0.25
H5	PA21	-1.75	-0.25
H6	VDDIO0	-1.75	-0.75
H7	PA20	-1.75	-1.25
H8	PB11	-1.75	-1.75

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-17. Device and Package Maximum Weight

14.8	mg

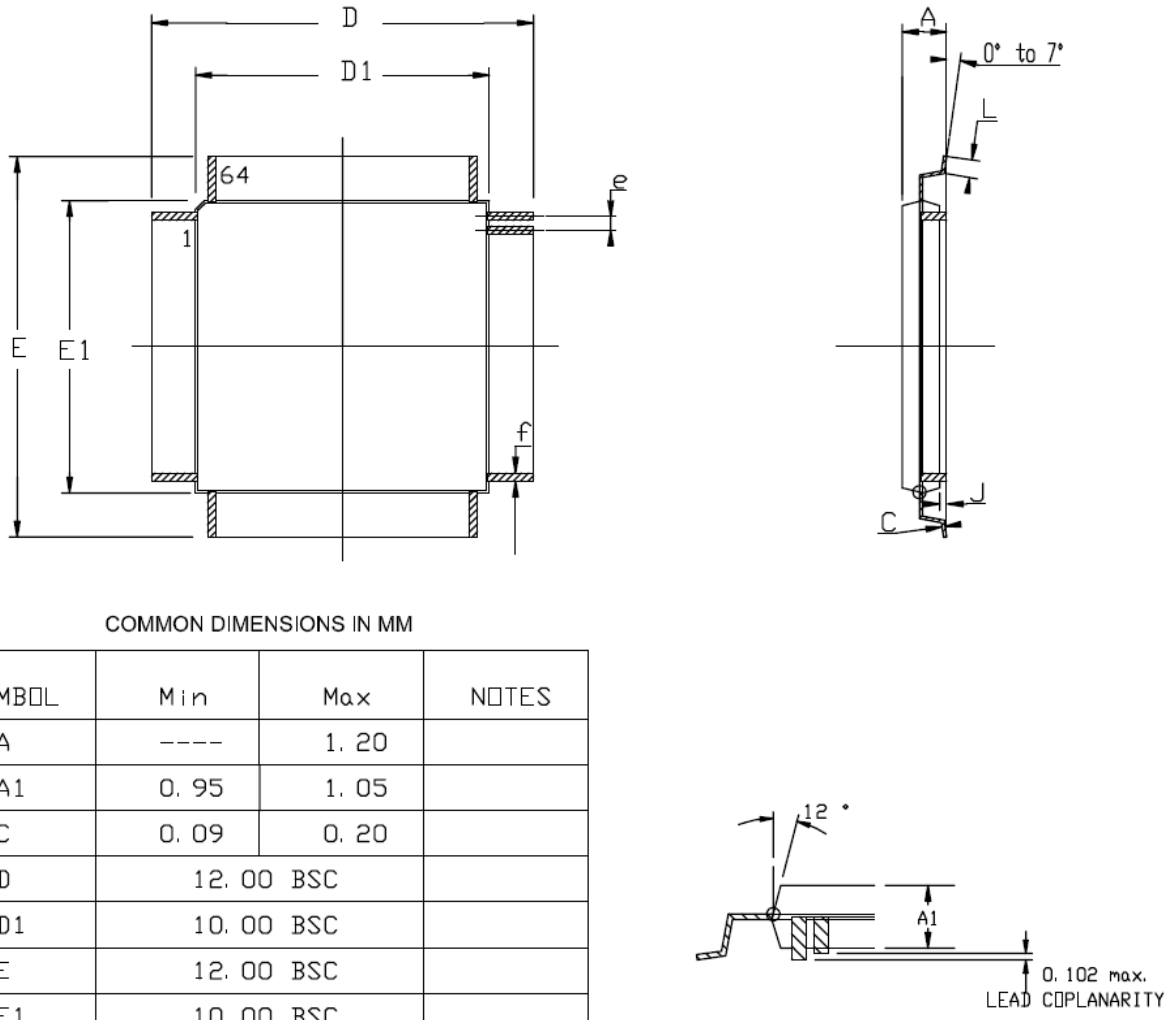
Table 10-18. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-19. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

Figure 10-7. TQFP-64 Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

Table 10-20. Device and Package Maximum Weight

300	mg

Table 10-21. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-22. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

10.3 Soldering Profile

Table 10-35 gives the recommended soldering profile from J-STD-20.

Table 10-35. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150 s
Time within 5·C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25·C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

12.1.7 FLASHCALW

Corrupted data in flash may happen after flash page write operations.
After a flash page write operation, reading (data read or code fetch) in flash may fail. This may lead to an expecption or to others errors derived from this corrupted read access.
Fix/Workaround
Before any flash page write operation, each 64-bit doublewords write in the page buffer must preceded by a 64-bit doublewords write in the page buffer with 0xFFFFFFFF_FFFFFFFF content at any address in the page. Note that special care is required when loading page buffer, refer to Section 2.5.9 ”Page Buffer Operations” on page 11.