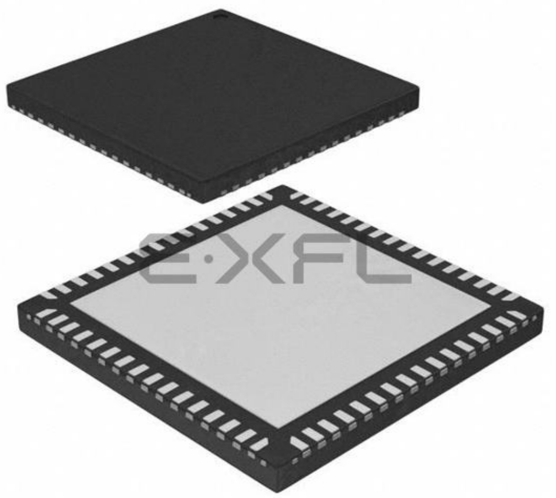


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 7x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls2ba-mu

Table 3-2. 64-pin GPIO Controller Function Multiplexing (Sheet 3 of 3)

ATSAM4LC QFP QFN	ATSAM4LS QFP QFN	Pin	GPIO	Supply	GPIO Functions A	B	C	D	E	F	G
	33	PA27	27	LCDA	SPI MISO	IISC ISCK	ABDACB DAC0	GLOC IN4	USART3 RTS		CATB SENSE0
	34	PA28	28	LCDA	SPI MOSI	IISC ISDI	ABDACB DACN0	GLOC IN5	USART3 CTS		CATB SENSE1
	35	PA29	29	LCDA	SPI SCK	IISC IWS	ABDACB DAC1	GLOC IN6	USART3 CLK		CATB SENSE2
	38	PA30	30	LCDA	SPI NPCS0	IISC ISDO	ABDACB DACN1	GLOC IN7	USART3 RXD		CATB SENSE3
	39	PA31	31	LCDA	SPI NPCS1	IISC IMCK	ABDACB CLK	GLOC OUT1	USART3 TXD		CATB DIS
11	11	PB00	32	VDDIN	TWIMS1 TWD	USART0 RXD					CATB SENSE21
12	12	PB01	33	VDDIN	TWIMS1 TWCK	USART0 TXD	EIC EXTINT0				CATB SENSE22
13	13	PB02	34	VDDANA	ADCIFE AD3	USART1 RTS	ABDACB DAC0	IISC ISCK	ACIFC ACBN0		CATB SENSE23
14	14	PB03	35	VDDANA	ADCIFE AD4	USART1 CLK	ABDACB DACN0	IISC ISDI	ACIFC ACBP0		CATB DIS
19	19	PB04	36	VDDANA	ADCIFE AD5	USART1 RXD	ABDACB DAC1	IISC ISDO	DACC EXT TRIG0		CATB SENSE24
20	20	PB05	37	VDDANA	ADCIFE AD6	USART1 TXD	ABDACB DACN1	IISC IMCK			CATB SENSE25
27	27	PB06	38	LCDA	USART3 RTS		GLOC IN4	IISC IWS		LCDCA SEG22	CATB SENSE26
28	28	PB07	39	LCDA	USART3 CTS		GLOC IN5	TC0 A0		LCDCA SEG21	CATB SENSE27
45	45	PB08	40	LCDA	USART3 CLK		GLOC IN6	TC0 B0		LCDCA SEG14	CATB SENSE28
46	46	PB09	41	LCDA	USART3 RXD	PEVC PAD EVT2	GLOC IN7	TC0 A1		LCDCA SEG15	CATB SENSE29
47	47	PB10	42	LCDA	USART3 TXD	PEVC PAD EVT3	GLOC OUT1	TC0 B1	SCIF GCLK0	LCDCA SEG16	CATB SENSE30
48	48	PB11	43	LCDA	USART0 CTS	SPI NPCS2		TC0 A2	SCIF GCLK1	LCDCA SEG17	CATB SENSE31
53	53	PB12	44	LCDC	USART0 RTS	SPI NPCS3	PEVC PAD EVT0	TC0 B2	SCIF GCLK2	LCDCA SEG32	CATB DIS
54	54	PB13	45	LCDC	USART0 CLK	SPI NPCS1	PEVC PAD EVT1	TC0 CLK0	SCIF GCLK3	LCDCA SEG33	CATB SENSE0
57	57	PB14	46	LCDC	USART0 RXD	SPI MISO	TWIM3 TWD	TC0 CLK1	SCIF GCLK IN0	LCDCA SEG36	CATB SENSE1
58	58	PB15	47	LCDC	USART0 TXD	SPI MOSI	TWIM3 TWCK	TC0 CLK2	SCIF GCLK IN1	LCDCA SEG37	CATB SENSE2

Table 3-3. 64-pin GPIO Controller Function Multiplexing for WLCSP package (Sheet 1 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
WLCSP	WLCSP				A	B	C	D	E	F	G
G4	G4	PA00	0	VDDIO							
G5	G5	PA01	1	VDDIO							
F3	F3	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
E2	E2	PA03	3	VDDIN		SPI MISO					
D3	D3	PA04	4	VDDANA	ADCIFE AD0	USART0 CLK	EIC EXTINT2	GLOC IN1			CATB SENSE0
C3	C3	PA05	5	VDDANA	ADCIFE AD1	USART0 RXD	EIC EXTINT3	GLOC IN2	ADCIFE TRIGGER		CATB SENSE1
C4	C4	PA06	6	VDDANA	DACC VOUT	USART0 RTS	EIC EXTINT1	GLOC IN0	ACIFC ACAN0		CATB SENSE2
C5	C5	PA07	7	VDDANA	ADCIFE AD2	USART0 TXD	EIC EXTINT4	GLOC IN3	ACIFC ACAP0		CATB SENSE3
B4	B4	PA08	8	LCDA	USART0 RTS	TC0 A0	PEVC PAD EVT0	GLOC OUT0		LCDCA SEG23	CATB SENSE4
A5	A5	PA09	9	LCDA	USART0 CTS	TC0 B0	PEVC PAD EVT1	PARC PCDATA0		LCDCA COM3	CATB SENSE5
B6	B6	PA10	10	LCDA	USART0 CLK	TC0 A1	PEVC PAD EVT2	PARC PCDATA1		LCDCA COM2	CATB SENSE6
B7	B7	PA11	11	LCDA	USART0 RXD	TC0 B1	PEVC PAD EVT3	PARC PCDATA2		LCDCA COM1	CATB SENSE7
A8	A8	PA12	12	LCDA	USART0 TXD	TC0 A2		PARC PCDATA3		LCDCA COM0	CATB DIS
C7	C7	PA13	13	LCDA	USART1 RTS	TC0 B2	SPI NPCS1	PARC PCDATA4		LCDCA SEG5	CATB SENSE8
D7	D7	PA14	14	LCDA	USART1 CLK	TC0 CLK0	SPI NPCS2	PARC PCDATA5		LCDCA SEG6	CATB SENSE9
E7	E7	PA15	15	LCDA	USART1 RXD	TC0 CLK1	SPI NPCS3	PARC PCDATA6		LCDCA SEG7	CATB SENSE10
F7	F7	PA16	16	LCDA	USART1 TXD	TC0 CLK2	EIC EXTINT1	PARC PCDATA7		LCDCA SEG8	CATB SENSE11
G8	G8	PA17	17	LCDA	USART2 RTS	ABDACB DAC0	EIC EXTINT2	PARC PCCK		LCDCA SEG9	CATB SENSE12
G7	G7	PA18	18	LCDA	USART2 CLK	ABDACB DACN0	EIC EXTINT3	PARC PCEN1		LCDCA SEG18	CATB SENSE13
G6	G6	PA19	19	LCDA	USART2 RXD	ABDACB DAC1	EIC EXTINT4	PARC PCEN2	SCIF GCLK0	LCDCA SEG19	CATB SENSE14
H7	H7	PA20	20	LCDA	USART2 TXD	ABDACB DACN1	EIC EXTINT5	GLOC IN0	SCIF GCLK1	LCDCA SEG20	CATB SENSE15
H5	H5	PA21	21	LCDC	SPI MISO	USART1 CTS	EIC EXTINT6	GLOC IN1	TWIM2 TWD	LCDCA SEG34	CATB SENSE16
F5	F5	PA22	22	LCDC	SPI MOSI	USART2 CTS	EIC EXTINT7	GLOC IN2	TWIM2 TWCK	LCDCA SEG35	CATB SENSE17

3.2.4 ITM Trace Connections

If the ITM trace is enabled, the ITM will take control over the pin PA23, irrespectively of the I/O Controller configuration. The Serial Wire Trace signal is available on pin PA23

3.2.5 Oscillator Pinout

The oscillators are not mapped to the normal GPIO functions and their muxings are controlled by registers in the System Control Interface (SCIF) or Backup System Control Interface (BSCIF). Refer to the Section 15. "System Control Interface (SCIF)" on page 308 and Section 15. "Backup System Control Interface (BSCIF)" on page 308 for more information about this.

Table 3-7. Oscillator Pinout

48-pin Packages	64-pin QFN/QFP	64-pin WLCSP	100-pin Packages	100-ball VFBGA	Pin Name	Oscillator Pin
1	1	G4	5	B9	PA00	XIN0
13	17	B2	26	B2	XIN32	XIN32
2	2	G5	6	B8	PA01	XOUT0
14	18	B3	27	C2	XOUT32	XOUT32

Table 3-8. Signal Descriptions List (Sheet 4 of 4)

Signal Name	Function	Type	Active Level	Comments
PA31 - PA00	Parallel I/O Controller I/O Port A	I/O		
PB15 - PB00	Parallel I/O Controller I/O Port B	I/O		
PC31 - PC00	Parallel I/O Controller I/O Port C	I/O		

Note: 1. See “Power and Startup Considerations” section.

3.4 I/O Line Considerations

3.4.1 SW/JTAG Pins

The JTAG pins switch to the JTAG functions if a rising edge is detected on TCK low after the RESET_N pin has been released. The TMS, and TDI pins have pull-up resistors when used as JTAG pins. The TCK pin always has pull-up enabled during reset. The JTAG pins can be used as GPIO pins and multiplexed with peripherals when the JTAG is disabled. Refer to Section 3.2.3 ”JTAG Port Connections” on page 29 for the JTAG port connections.

For more details, refer to Section 1.1 ”Enhanced Debug Port (EDP)” on page 3.

3.4.2 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIN. As the product integrates a power-on reset detector, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

3.4.3 TWI Pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and-inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as GPIO pins.

3.4.4 GPIO Pins

All the I/O lines integrate a pull-up/pull-down resistor and slew rate controller. Programming these features is performed independently for each I/O line through the GPIO Controllers. After reset, I/O lines default as inputs with pull-up and pull-down resistors disabled and slew rate enabled.

3.4.5 High-drive Pins

The six pins PA02, PB00, PB01, PC04, PC05 and PC06 have high-drive output capabilities. Refer to Section 9.6.2 ”High-drive I/O Pin : PA02, PC04, PC05, PC06” on page 115 for electrical characteristics.

3.4.6 USB Pins

When these pins are used for USB, the pins are behaving according to the USB specification. When used as GPIO pins or used for other peripherals, the pins have the same behavior as other normal I/O pins, but the characteristics are different. Refer to Section 9.6.3 ”USB I/O Pin : PA25, PA26” on page 116 for electrical characteristics.

These pins are compliant to USB standard only when VDDIO power supply is 3.3V nominal.

Table 4-2. Interrupt Request Signal Map (Sheet 2 of 3)

Line	Module	Signal
12	Peripheral DMA Controller	PDCA 11
13	Peripheral DMA Controller	PDCA 12
14	Peripheral DMA Controller	PDCA 13
15	Peripheral DMA Controller	PDCA 14
16	Peripheral DMA Controller	PDCA 15
17	CRC Calculation Unit	CRCCU
18	USB 2.0 Interface	USBC
19	Peripheral Event Controller	PEVC TR
20	Peripheral Event Controller	PEVC OV
21	Advanced Encryption Standard	AESA
22	Power Manager	PM
23	System Control Interface	SCIF
24	Frequency Meter	FREQM
25	General-Purpose Input/Output Controller	GPIO 0
26	General-Purpose Input/Output Controller	GPIO 1
27	General-Purpose Input/Output Controller	GPIO 2
28	General-Purpose Input/Output Controller	GPIO 3
29	General-Purpose Input/Output Controller	GPIO 4
30	General-Purpose Input/Output Controller	GPIO 5
31	General-Purpose Input/Output Controller	GPIO 6
32	General-Purpose Input/Output Controller	GPIO 7
33	General-Purpose Input/Output Controller	GPIO 8
34	General-Purpose Input/Output Controller	GPIO 9
35	General-Purpose Input/Output Controller	GPIO 10
36	General-Purpose Input/Output Controller	GPIO 11
37	Backup Power Manager	BPM
38	Backup System Control Interface	BSCIF
39	Asynchronous Timer	AST ALARM
40	Asynchronous Timer	AST PER
41	Asynchronous Timer	AST OVF
42	Asynchronous Timer	AST READY
43	Asynchronous Timer	AST CLKREADY
44	Watchdog Timer	WDT
45	External Interrupt Controller	EIC 1
46	External Interrupt Controller	EIC 2
47	External Interrupt Controller	EIC 3

mechanism can be useful for applications that only require the processor to run when an interrupt occurs.

Before entering the SLEEP mode, the user must configure:

- the SLEEP mode configuration field (BPM.PMCON.SLEEP), Refer to Table 7-1.
- the SCR.SLEEPDEEP bit to 0. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- the BPM.PMCON.RET bit to 0.
- the BPM.PMCON.BKUP bit to 0.

7.1.1.2 Exiting SLEEP mode

The NVIC wakes the system up when it detects any non-masked interrupt with sufficient priority to cause exception entry. The system goes back to the RUN mode from which the SLEEP mode was entered. The CPU and affected modules are restarted. Note that even if an interrupt is enabled in SLEEP mode, it will not trigger if the source module is not clocked.

7.1.2 WAIT Mode and RETENTION Mode

The WAIT and RETENTION modes allow achieving very low power consumption while maintaining the Core domain powered-on. Internal SRAM and registers contents of the Core domain are preserved.

In these modes, all clocks are stopped except the 32kHz clocks (OSC32K, RC32K) which are kept running if enabled.

In RETENTION mode, the SleepWalking feature is not supported and must not be used.

7.1.2.1 Entering WAIT or RETENTION Mode

The WAIT or RETENTION modes are entered by executing the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 0.
- set the BPM.PMCON.RET bit to RETENTION or WAIT mode.

SLEEPONEXIT feature is also available. See ”Entering SLEEP mode” on page 56.

7.1.2.2 Exiting WAIT or RETENTION Mode

In WAIT or RETENTION modes, synchronous clocks are stopped preventing interrupt sources from triggering. To wakeup the system, asynchronous wake up sources (AST, EIC, USBC ...) should be enabled in the peripheral (refer to the documentation of the peripheral). The PM.AWEN (Asynchronous Wake Up Enable) register should also be enabled for all peripheral except for EIC and AST.

When the enabled asynchronous wake up event occurs and the system is waken-up, it will generate either:

- an interrupt on the PM WAKE interrupt line if enabled (Refer to Section 9. ”Power Manager (PM)” on page 677). In that case, the PM.WCAUSE register indicates the wakeup source.
- or an interrupt directly from the peripheral if enabled (Refer to the section of the peripheral).

When waking up, the system goes back to the RUN mode mode from which the WAIT or RETENTION mode was entered.

7.1.3 BACKUP Mode

The BACKUP mode allows achieving the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time.

The Core domain is powered-off. The internal SRAM and register contents of the Core domain are lost. The Backup domain is kept powered-on. The 32kHz clock (RC32K or OSC32K) is kept running if enabled to feed modules that require clocking.

In BACKUP mode, the configuration of the I/O lines is preserved. Refer to Section 9. "Backup Power Manager (BPM)" on page 677 to have more details.

7.1.3.1 Entering BACKUP Mode

The Backup mode is entered by using the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 1.

7.1.3.2 Exiting BACKUP Mode

Exit from BACKUP mode happens if a reset occurs or if an enabled wake up event occurs.

The reset sources are:

- BOD33 reset
- BOD18 reset
- WDT reset
- External reset in RESET_N pin

The wake up sources are:

- EIC lines (level transition only)
- BOD33 interrupt
- BOD18 interrupt
- AST alarm, periodic, overflow
- WDT interrupt

The RC32K or OSC32K should be used as clock source for modules if required. The PMCON.CK32S is used to select one of these two 32kHz clock sources.

Exiting the BACKUP mode is triggered by:

- a reset source: an internal reset sequence is performed according to the reset source. Once VDDCORE is stable and has the correct value according to RUN0 mode, the internal reset is released and program execution starts. The corresponding reset source is flagged in the Reset Cause register (RCAUSE) of the PM.
- a wake up source: the Backup domain is not reset. An internal reset is generated to the Core domain, and the system switches back to the previous RUN mode. Once VDDCORE is stable and has the correct value, the internal reset in the Core domain is released and program execution starts. The BKUP bit is set in the Reset Cause register (RCAUSE) of the PM. It allows the user to discriminate between the reset cause and a wake up cause from the BACKUP mode. The wake up cause can be found in the Backup Wake up Cause register (BPM.BKUPWCAUSE).

0: No bus error has been detected sincle last clear of this bit

- **HCR: Hold Core reset**

  1: The Cortex-M4 core is held under reset

  0: The Cortex-M4 core is not held under reset

- **DONE: Operation done**

  1: At least one operation has terminated since last clear of this field

  0: No operation has terminated since last clear of this field

8.9.11.6 Data Register

Name: DATA

Access Type: Read/Write

Offset: 0x14

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DATA							

23	22	21	20	19	18	17	16
DATA							

15	14	13	12	11	10	9	8
DATA							

7	6	5	4	3	2	1	0
DATA							

- **DATA: Generic data register**

8.9.11.8 Chip Identification Register

Name: CIDR

Access Type: Read-Only

Offset: 0xF0

Reset Value: -

31	30	29	28	27	26	25	24
EXT	NVPTYP			ARCH			

23	22	21	20	19	18	17	16
ARCH			SRAMSIZ				

15	14	13	12	11	10	9	8
NVPSIZ2				NVPSIZ			

7	6	5	4	3	2	1	0
EPROC			VERSION				

Note: Refer to section CHIPID for more information on this register.

3. These values are based on characterization. These values are not covered by test limits in production

9.6.2 High-drive I/O Pin : PA02, PC04, PC05, PC06

Table 9-14. High-drive I/O Pin Characteristics [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance [2]				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance [2]				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current [3]	ODCR0=0	1.68V<V_{VDD}<2.7V			1.8	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
I_{OH}	Output high-level current [3]	ODCR0=0	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
t_{RISE}	Rise time [2]	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
t_{FALL}	Fall time [2]	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
F_{PINMAX}	Output frequency [2]	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			22	MHz
		OSRR0=1				17	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			35	MHz
		OSRR0=1				26	MHz
I_{LEAK}	Input leakage current [3]	Pull-up resistors disabled			0.01	2	µA
C_{IN}	Input capacitance [2]				10		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.6.3 USB I/O Pin : PA25, PA26

Table 9-15. USB I/O Pin Characteristics in GPIO configuration [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance [2]				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance[2]				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current [3]	ODCR0=0	1.68V<V_{VDD}<2.7V		20		mA
			2.7V<V_{VDD}<3.6V		30		
I_{OH}	Output high-level current[3]	ODCR0=0	1.68V<V_{VDD}<2.7V		20		mA
			2.7V<V_{VDD}<3.6V		30		
F_{PINMAX}	Maximum frequency[2]	ODCR0=0 OSRR0=0	load = 25pF			20	MHz
I_{LEAK}	Input leakage current[3]	Pull-up resistors disabled			0.01	1	µA
C_{IN}	Input capacitance[2]				5		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.6.4 TWI Pin : PA21, PA22, PA23, PA24, PB14, PB15

Table 9-16. TWI Pin Characteristics in TWI configuration [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance [2]				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance[2]				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.3 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.7 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
I_{OL}	Output low-level current [3]	DRIVEL=0				0.5	mA
		DRIVEL=1				1.0	
		DRIVEL=2				1.6	
		DRIVEL=3				3.1	
		DRIVEL=4				6.2	
		DRIVEL=5				9.3	
		DRIVEL=6				15.5	
		DRIVEL=7				21.8	

Table 9-17. TWI Pin Characteristics in GPIO configuration [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{RISE}	Rise time[2]	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		18		ns
		OSRR0=1			110		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		10		ns
		OSRR0=1			50		
t_{FALL}	Fall time[2]	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		19		ns
		OSRR0=1			140		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		12		ns
		OSRR0=1			63		

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Table 9-18. Common TWI Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LEAK}	Input leakage current [1]	Pull-up resistors disabled		0.01	1	µA
C_{IN}	Input capacitance[2]			5		pF

1. These values are based on simulation. These values are not covered by test limits in production or characterization

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-35. Flash Endurance and Data Retention [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{FARRAY}	Array endurance (write/page)	f_{CLK_AHB} > 10MHz	100k			cycles
N_{FFUSE}	General Purpose fuses endurance (write/bit)	f_{CLK_AHB} > 10MHz	10k			
t_{RET}	Data retention		15			years

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-50. Analog Comparator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Hysteresis[1]	V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 1[2] Fast mode	10		55	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 1[2] Low power mode	10		68	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 2[2] Fast mode	26		83	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 2[2] Low power mode	19		91	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 3[2] Fast mode	43		106	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 3[2] Low power mode	32		136	mV
	Propagation delay[1]	Changes for V_{ACM}=VDDIO/2 100mV Overdrive Fast mode			67	ns
		Changes for V_{ACM}=VDDIO/2 100mV Overdrive Low power mode			315	ns
$t_{STARTUP}$	Startup time[1]	Enable to ready delay Fast mode			1.19	µs
		Enable to ready delay Low power mode			3.61	µs
I_{AC}	Channel current consumption [3]	Low power mode, no hysteresis		4.9	8.7	µA
		Fast mode, no hysteresis		63	127	

1. These values are based on characterization. These values are not covered by test limits in production
2. HYSTAC.CONFn.HYS field, refer to the Analog Comparator Interface chapter
3. These values are based on simulation. These values are not covered by test limits in production or characterization

Figure 9-10. USART in SPI Slave Mode with (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

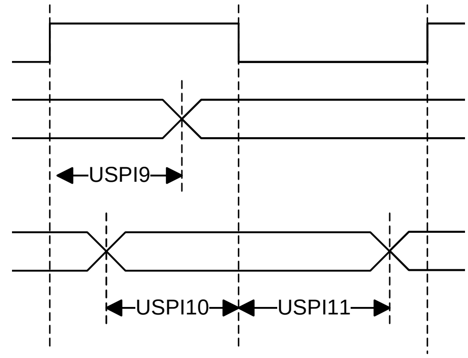


Figure 9-11. USART in SPI Slave Mode, NPCS Timing

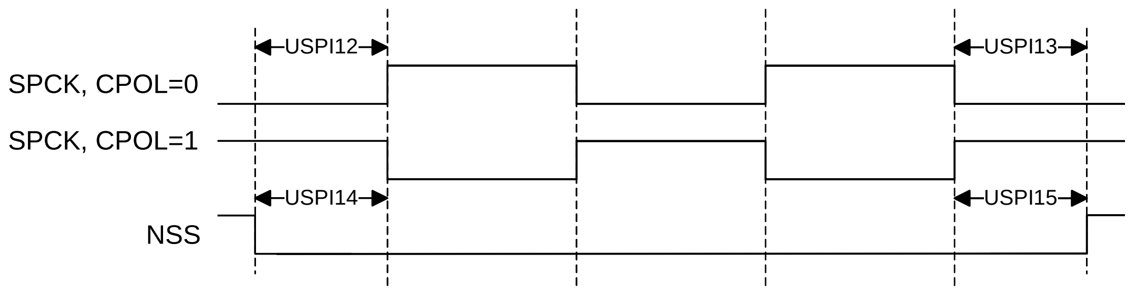
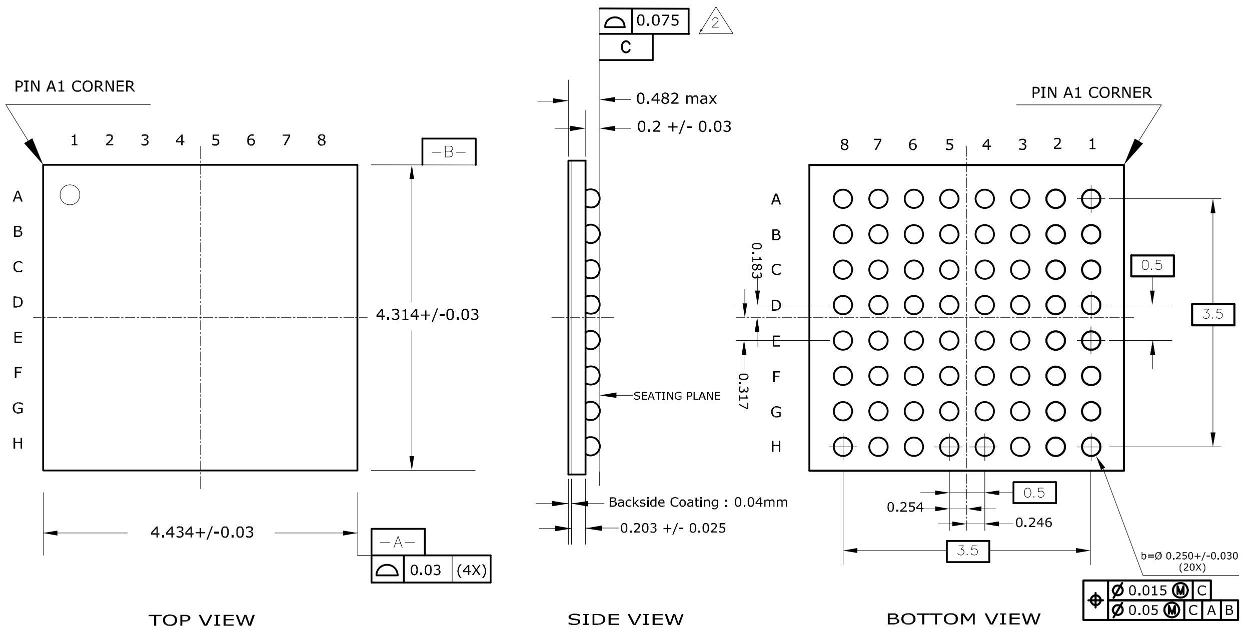


Table 9-58. USART0 in SPI mode Timing, Slave Mode(1)

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		740.67	ns
USPI7	MOSI setup time before SPCK rises		56.73 + t_{SAMPLE}(2) + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		45.18 -(t_{SAMPLE}(2) + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			670.18	
USPI10	MOSI setup time before SPCK falls		56.73 +(t_{SAMPLE}(2) + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		45.18 -(t_{SAMPLE}(2) + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		688.71		
USPI13	NSS hold time after SPCK falls		-2.25		
USPI14	NSS setup time before SPCK falls		688.71		
USPI15	NSS hold time after SPCK rises		-2.25		

Figure 10-3. WLCSP64 SAM4LC4/2 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.746	1.683
A2	GNDANA	1.246	1.683
A3	ADVREFP	0.746	1.683
A4	VDDANA	0.246	1.683
A5	PA09	-0.254	1.683
A6	CAPL	-0.754	1.683
A7	CAPH	-1.254	1.683
A8	PA12	-1.754	1.683
B1	PB03	1.746	1.183
B2	XIN32	1.246	1.183
B3	XOUT32	0.746	1.183
B4	PA08	0.246	1.183
B5	PB06	-0.254	1.183
B6	PA10	-0.754	1.183
B7	PA11	-1.254	1.183
B8	VLCD	-1.754	1.183
C1	VDDIN	1.746	0.683
C2	PB01	1.246	0.683
C3	PA05	0.746	0.683
C4	PA06	0.246	0.683
C5	PA07	-0.254	0.683
C6	PB07	-0.754	0.683

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	-1.254	0.683
C8	BIAS1	-1.754	0.683
D1	VDDOUT	1.746	0.183
D2	PB00	1.246	0.183
D3	PA04	0.746	0.183
D4	PB05	0.246	0.183
D5	PB12	-0.254	0.183
D6	PB08	-0.754	0.183
D7	PA14	-1.254	0.183
D8	BIAS2	-1.754	0.183
E1	GNDIN	1.746	-0.317
E2	PA03	1.246	-0.317
E3	PB02	0.746	-0.317
E4	RESET_N	0.246	-0.317
E5	PB13	-0.254	-0.317
E6	PB09	-0.754	-0.317
E7	PA15	-1.254	-0.317
E8	GNDIO0	-1.754	-0.317
F1	VDDCORE	1.746	-0.817
F2	TCK	1.246	-0.817
F3	PA02	0.746	-0.817
F4	PB14	0.246	-0.817

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.254	-0.817
F6	PB10	-0.754	-0.817
F7	PA16	-1.254	-0.817
F8	VLCDIN	-1.754	-0.817
G1	GNDIO1	1.746	-1.317
G2	PA26	1.246	-1.317
G3	PA24	0.746	-1.317
G4	PA00	0.246	-1.317
G5	PA01	-0.254	-1.317
G6	PA19	-0.754	-1.317
G7	PA18	-1.254	-1.317
G8	PA17	-1.754	-1.317
H1	VDDIO1	1.746	-1.817
H2	PA25	1.246	-1.817
H3	PA23	0.746	-1.817
H4	PB15	0.246	-1.817
H5	PA21	-0.254	-1.817
H6	VDDIO0	-0.754	-1.817
H7	PA20	-1.254	-1.817
H8	PB11	-1.754	-1.817

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-8. Device and Package Maximum Weight

14.8	mg

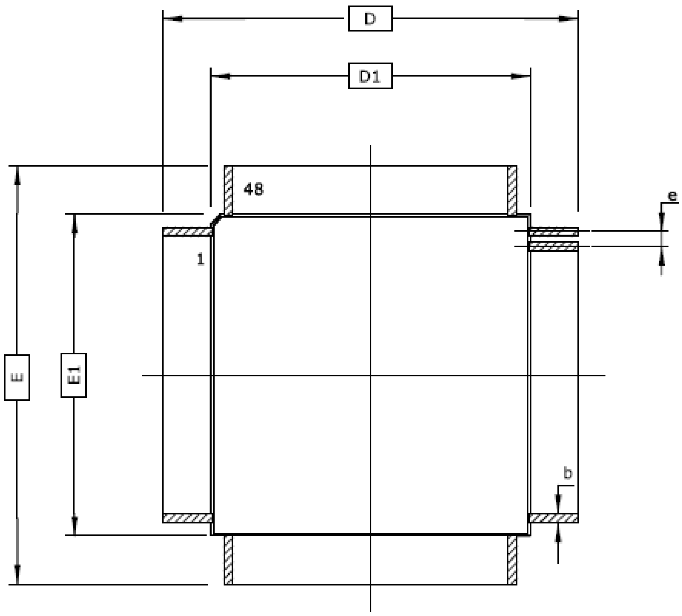
Table 10-9. Package Characteristics

Moisture Sensitivity Level	MSL3

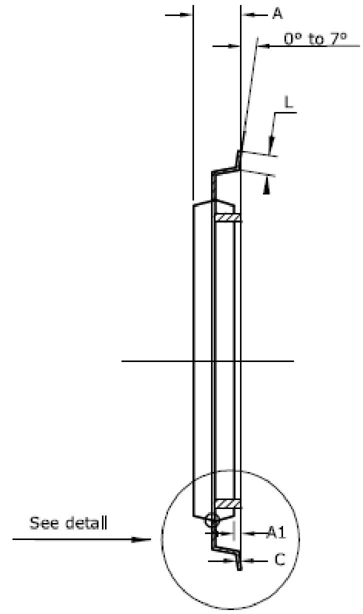
Table 10-10. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

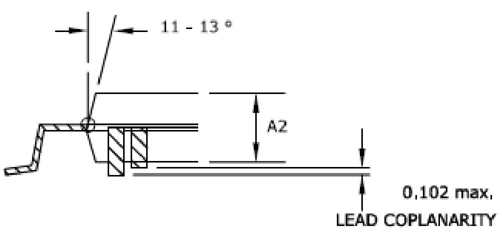
Figure 10-9. TQFP-48 (ATSAM4LC4/2 and ATSAM4LS4/2 Only) Package Drawing



TOP VIEW



SIDE VIEW



DETAIL VIEW

COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	
A1	0.05	---	0.15	
A2	0.95	---	1.05	
C	0.09	---	0.20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0.45	---	0.75	
b	0.17	---	0.27	
e	0.50 BSC			

Table 10-26. Device and Package Maximum Weight

140	mg

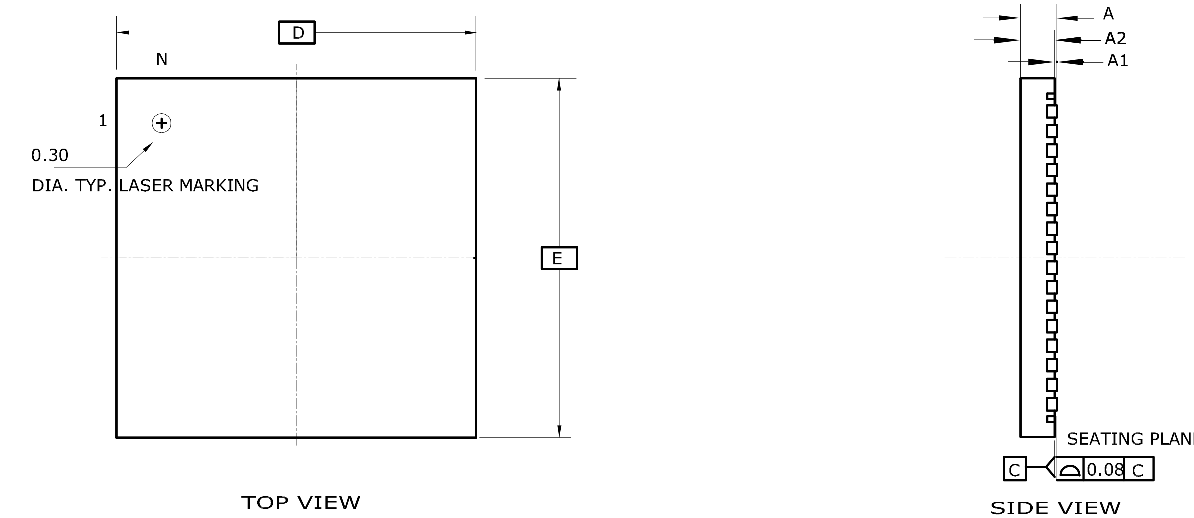
Table 10-27. Package Characteristics

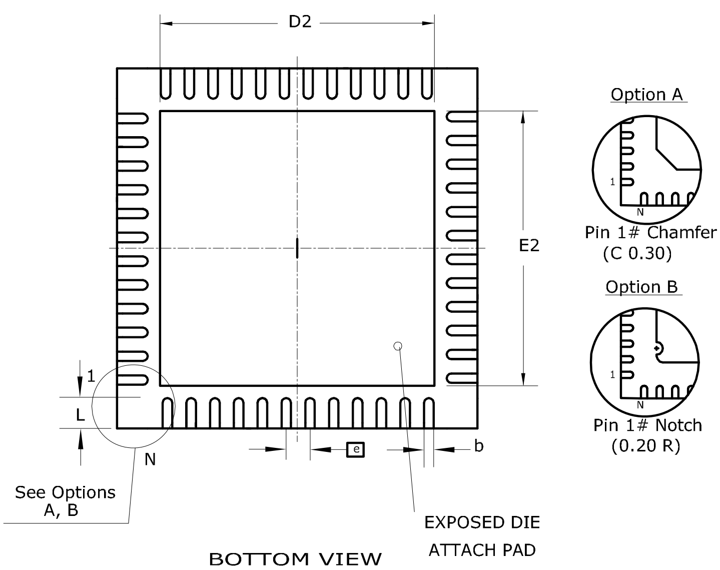
Moisture Sensitivity Level	MSL3

Table 10-28. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 10-11. QFN-48 Package Drawing for ATSAM4LC8 and ATSAM4LS8





COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A2	0.75	-----	1.00	
D/E		7 BSC		
D2/E2	5.50	5.60	5.70	
L	0.30	0.40	0.50	
b	0.17	-----	0.30	2
e		0.50 BSC		
n		48		

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 10-32. Device and Package Maximum Weight

140	mg

Table 10-33. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-34. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

Table 11-5. ATSAM4LS4 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LS4CA-AU-ES	256	32	TQFP100	ES	Green	N/A
ATSAM4LS4CA-AU	256	32	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS4CA-AUR	256	32	TQFP100	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS4CA-CFU	256	32	VFBGA100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS4CA-CFUR	256	32	VFBGA100	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS4BA-AU-ES	256	32	TQFP64	ES	Green	N/A
ATSAM4LS4BA-AU	256	32	TQFP64	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS4BA-AUR	256	32	TQFP64	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS4BA-MU-ES	256	32	QFN64	ES	Green	N/A
ATSAM4LS4BA-MU	256	32	QFN64	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS4BA-MUR	256	32	QFN64	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS4BA-UUR	256	32	WLCSP64	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS4AA-AU-ES	256	32	TQFP48	ES	Green	N/A
ATSAM4LS4AA-AU	256	32	TQFP48	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS4AA-AUR	256	32	TQFP48	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS4AA-MU-ES	256	32	QFN48	ES	Green	N/A
ATSAM4LS4AA-MU	256	32	QFN48	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS4AA-MUR	256	32	QFN48	Reel	Green	Industrial -40°C to 85°C

Table 11-6. ATSAM4LS2 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LS2CA-AU	128	32	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS2CA-AUR	128	32	TQFP100	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS2CA-CFU	128	32	VFBGA100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS2CA-CFUR	128	32	VFBGA100	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS2BA-AU	128	32	TQFP64	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS2BA-AUR	128	32	TQFP64	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS2BA-MU	128	32	QFN64	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS2BA-MUR	128	32	QFN64	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS2BA-UUR	128	32	WLCSP64	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS2AA-AU	128	32	TQFP48	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS2AA-AUR	128	32	TQFP48	Reel	Green	Industrial -40°C to 85°C
ATSAM4LS2AA-MU	128	32	QFN48	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS2AA-MUR	128	32	QFN48	Reel	Green	Industrial -40°C to 85°C