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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls2ca-aur

  - PLL up to 240MHz for device clock and for USB
  - Digital Frequency Locked Loop (DFLL) with wide input range
  - Up to 16 peripheral DMA (PDCA) channels
- Peripherals
  - USB 2.0 Device and Embedded Host: 12 Mbps, up to 8 bidirectional Endpoints and Multi-packet Ping-pong Mode. On-Chip Transceiver
  - Liquid Crystal Display (LCD) Module with Capacity up to 40 Segments and up to 4 Common Terminals
  - One USART with ISO7816, IrDA®, RS-485, SPI, Manchester and LIN Mode
  - Three USART with SPI Mode
  - One PicoUART for extended UART wake-up capabilities in all sleep modes
  - Windowed Watchdog Timer (WDT)
  - Asynchronous Timer (AST) with Real-time Clock Capability, Counter or Calendar Mode Supported
  - Frequency Meter (FREQM) for Accurate Measuring of Clock Frequency
  - Six 16-bit Timer/Counter (TC) Channels with capture, waveform, compare and PWM mode
  - One Master/Slave Serial Peripheral Interface (SPI) with Chip Select Signals
  - Four Master and Two Slave Two-wire Interfaces (TWI), up to 3.4Mbit/s I^2C-compatible
  - One Advanced Encryption System (AES) with 128-bit key length
  - One 16-channel ADC 300Ksps (ADC) with up to 12 Bits Resolution
  - One DAC 500Ksps (DACC) with up to 10 Bits Resolution
  - Four Analog Comparators (ACIFC) with Optional Window Detection
  - Capacitive Touch Module (CATB) supporting up to 32 buttons
  - Audio Bitstream DAC (ABDACB) Suitable for Stereo Audio
  - Inter-IC Sound (IISC) Controller, Compliant with Inter-IC Sound (I^2S) Specification
  - Peripheral Event System for Direct Peripheral to Peripheral Communication
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)
  - Random generator (TRNG)
  - Parallel Capture Module (PARC)
  - Glue Logic Controller (GLOC)
- I/O
  - Up to 75 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and slew-rate control
  - Up to Six High-drive I/O Pins
- Single 1.68-3.6V Power Supply
- Packages
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball VFBGA, 7x7 mm, pitch 0.65 mm
  - 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm
  - 64-ball WLCSP, 4,314x4,434 mm, pitch 0.5 mm for SAM4LC4/2 and SAM4LS4/2 series
  - 64-ball WLCSP, 5,270x5,194 mm, pitch 0.5 mm for SAM4LC8 and SAM4LS8 series
  - 48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm

Table 2-2. ATSAM4LC Configuration Summary

Feature	ATSAM4LC8/4/2C	ATSAM4LC8/4/2B	ATSAM4LC8/4/2A
Oscillators	Digital Frequency Locked Loop 20-150MHz (DFLL) Phase Locked Loop 48-240MHz (PLL) Crystal Oscillator 0.6-30MHz (OSC0) Crystal Oscillator 32kHz (OSC32K) RC Oscillator 80MHz (RC80M) RC Oscillator 4,8,12MHz (RCFAST) RC Oscillator 115kHz (RCSYS) RC Oscillator 32kHz (RC32K)		
ADC	15-channel	7-channel	3-channel
DAC	1-channel		
Analog Comparators	4	2	1
CATB Sensors	32	32	26
USB	1		
Audio Bitstream DAC	1		
IIS Controller	1		
Packages	TQFP/VFBGA	TQFP/QFN/ WLCSP	TQFP/QFN

.

Table 2-3. ATSAM4LS Configuration Summary

Feature	ATSAM4LS8/4/2C	ATSAM4LS8/4/2B	ATSAM4LS8/4/2A
Number of Pins	100	64	48
Max Frequency	48MHz		
Flash	512/256/128KB		
SRAM	64/32/32KB		
SEGMENT LCD	NA		
GPIO	80	48	32
High-drive pins	6	3	1
External Interrupts	8 + 1 NMI		
TWI	2 Masters + 2 Masters/Slaves		1 Master + 1 Master/Slave
USART	4		3 in LC sub series 4 in LS sub series
PICOUART	1		0
Peripheral DMA Channels	16		
AESA	NA		
Peripheral Event System	1		
SPI	1		
Asynchronous Timers	1		

Table 3-2. 64-pin GPIO Controller Function Multiplexing (Sheet 3 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
QFP QFN	QFP QFN				A	B	C	D	E	F	G
	33	PA27	27	LCDA	SPI MISO	IISC ISCK	ABDACB DAC0	GLOC IN4	USART3 RTS		CATB SENSE0
	34	PA28	28	LCDA	SPI MOSI	IISC ISDI	ABDACB DACN0	GLOC IN5	USART3 CTS		CATB SENSE1
	35	PA29	29	LCDA	SPI SCK	IISC IWS	ABDACB DAC1	GLOC IN6	USART3 CLK		CATB SENSE2
	38	PA30	30	LCDA	SPI NPCS0	IISC ISDO	ABDACB DACN1	GLOC IN7	USART3 RXD		CATB SENSE3
	39	PA31	31	LCDA	SPI NPCS1	IISC IMCK	ABDACB CLK	GLOC OUT1	USART3 TXD		CATB DIS
11	11	PB00	32	VDDIN	TWIMS1 TWD	USART0 RXD					CATB SENSE21
12	12	PB01	33	VDDIN	TWIMS1 TWCK	USART0 TXD	EIC EXTINT0				CATB SENSE22
13	13	PB02	34	VDDANA	ADCIFE AD3	USART1 RTS	ABDACB DAC0	IISC ISCK	ACIFC ACBN0		CATB SENSE23
14	14	PB03	35	VDDANA	ADCIFE AD4	USART1 CLK	ABDACB DACN0	IISC ISDI	ACIFC ACBP0		CATB DIS
19	19	PB04	36	VDDANA	ADCIFE AD5	USART1 RXD	ABDACB DAC1	IISC ISDO	DACC EXT TRIG0		CATB SENSE24
20	20	PB05	37	VDDANA	ADCIFE AD6	USART1 TXD	ABDACB DACN1	IISC IMCK			CATB SENSE25
27	27	PB06	38	LCDA	USART3 RTS		GLOC IN4	IISC IWS		LCDCA SEG22	CATB SENSE26
28	28	PB07	39	LCDA	USART3 CTS		GLOC IN5	TC0 A0		LCDCA SEG21	CATB SENSE27
45	45	PB08	40	LCDA	USART3 CLK		GLOC IN6	TC0 B0		LCDCA SEG14	CATB SENSE28
46	46	PB09	41	LCDA	USART3 RXD	PEVC PAD EVT2	GLOC IN7	TC0 A1		LCDCA SEG15	CATB SENSE29
47	47	PB10	42	LCDA	USART3 TXD	PEVC PAD EVT3	GLOC OUT1	TC0 B1	SCIF GCLK0	LCDCA SEG16	CATB SENSE30
48	48	PB11	43	LCDA	USART0 CTS	SPI NPCS2		TC0 A2	SCIF GCLK1	LCDCA SEG17	CATB SENSE31
53	53	PB12	44	LCDC	USART0 RTS	SPI NPCS3	PEVC PAD EVT0	TC0 B2	SCIF GCLK2	LCDCA SEG32	CATB DIS
54	54	PB13	45	LCDC	USART0 CLK	SPI NPCS1	PEVC PAD EVT1	TC0 CLK0	SCIF GCLK3	LCDCA SEG33	CATB SENSE0
57	57	PB14	46	LCDC	USART0 RXD	SPI MISO	TWIM3 TWD	TC0 CLK1	SCIF GCLK IN0	LCDCA SEG36	CATB SENSE1
58	58	PB15	47	LCDC	USART0 TXD	SPI MOSI	TWIM3 TWCK	TC0 CLK2	SCIF GCLK IN1	LCDCA SEG37	CATB SENSE2

4.6 Cortex-M4 implementations options

This table provides the specific configuration options implemented in the SAM4L series

Option	Implementation
Inclusion of MPU	yes
Inclusion of FPU	No
Number of interrupts	80
Number of priority bits	4
Inclusion of the WIC	No
Embedded Trace Macrocell	No
Sleep mode instruction	Only WFI supported
Endianness	Little Endian
Bit-banding	No
SysTick timer	Yes
Register reset values	No

Table 4-1. Cortex-M4 implementation options

4.7 Cortex-M4 Interrupts map

The table below shows how the interrupt request signals are connected to the NVIC.

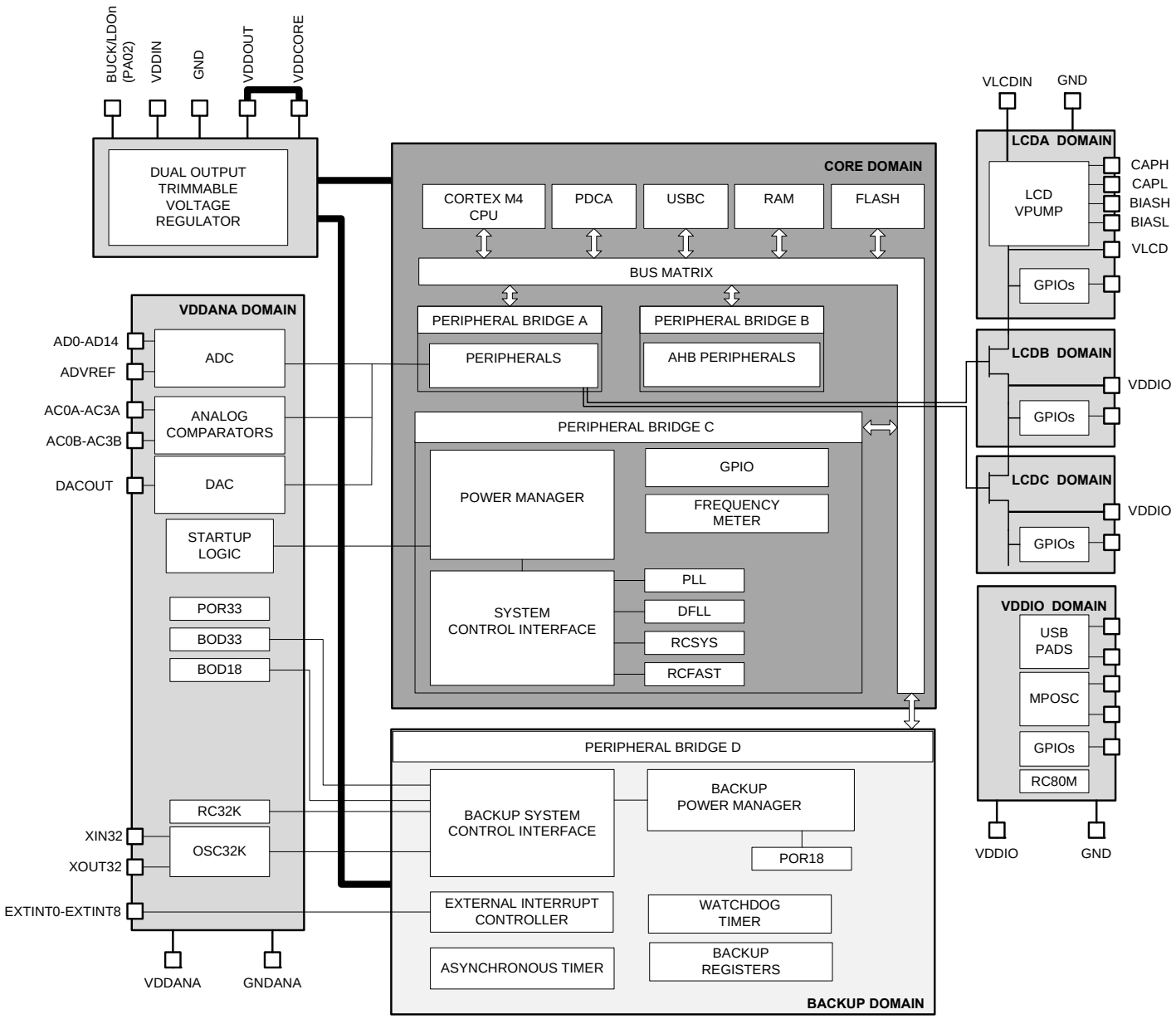
Table 4-2. Interrupt Request Signal Map (Sheet 1 of 3)

Line	Module	Signal
0	Flash Controller	HFLASHC
1	Peripheral DMA Controller	PDCA 0
2	Peripheral DMA Controller	PDCA 1
3	Peripheral DMA Controller	PDCA 2
4	Peripheral DMA Controller	PDCA 3
5	Peripheral DMA Controller	PDCA 4
6	Peripheral DMA Controller	PDCA 5
7	Peripheral DMA Controller	PDCA 6
8	Peripheral DMA Controller	PDCA 7
9	Peripheral DMA Controller	PDCA 8
10	Peripheral DMA Controller	PDCA 9
11	Peripheral DMA Controller	PDCA 10

Table 4-2. Interrupt Request Signal Map (Sheet 2 of 3)

Line	Module	Signal
12	Peripheral DMA Controller	PDCA 11
13	Peripheral DMA Controller	PDCA 12
14	Peripheral DMA Controller	PDCA 13
15	Peripheral DMA Controller	PDCA 14
16	Peripheral DMA Controller	PDCA 15
17	CRC Calculation Unit	CRCCU
18	USB 2.0 Interface	USBC
19	Peripheral Event Controller	PEVC TR
20	Peripheral Event Controller	PEVC OV
21	Advanced Encryption Standard	AESA
22	Power Manager	PM
23	System Control Interface	SCIF
24	Frequency Meter	FREQM
25	General-Purpose Input/Output Controller	GPIO 0
26	General-Purpose Input/Output Controller	GPIO 1
27	General-Purpose Input/Output Controller	GPIO 2
28	General-Purpose Input/Output Controller	GPIO 3
29	General-Purpose Input/Output Controller	GPIO 4
30	General-Purpose Input/Output Controller	GPIO 5
31	General-Purpose Input/Output Controller	GPIO 6
32	General-Purpose Input/Output Controller	GPIO 7
33	General-Purpose Input/Output Controller	GPIO 8
34	General-Purpose Input/Output Controller	GPIO 9
35	General-Purpose Input/Output Controller	GPIO 10
36	General-Purpose Input/Output Controller	GPIO 11
37	Backup Power Manager	BPM
38	Backup System Control Interface	BSCIF
39	Asynchronous Timer	AST ALARM
40	Asynchronous Timer	AST PER
41	Asynchronous Timer	AST OVF
42	Asynchronous Timer	AST READY
43	Asynchronous Timer	AST CLKREADY
44	Watchdog Timer	WDT
45	External Interrupt Controller	EIC 1
46	External Interrupt Controller	EIC 2
47	External Interrupt Controller	EIC 3

Figure 6-2. ATSAM4LC Power Domain Diagram



7.1.4 Wakeup Time

7.1.4.1 Wakeup Time From SLEEP Mode

The latency depends on the clock sources wake up time. If the clock sources are not stopped, there is no latency to wake the clocks up.

7.1.4.2 Wakeup Time From WAIT or RETENTION Mode

The wake up latency consists of:

- the switching time from the low power configuration to the RUN mode power configuration. By default, the switching time is completed when all the voltage regulation system is ready. To speed-up the startup time, the user can set the Fast Wakeup bit in BPM.PMCON register.
- the wake up time of the RC oscillator used to start the system up. By default, the RCSYS oscillator is used to startup the system. The user can use another clock source (RCFAST for example) to speed up the startup time by configuring the PM.FASTWKUP register. Refer to Section 9. ”Power Manager (PM)” on page 677.
- the Flash memory wake up time.

To have the shortest wakeup time, the user should:

- set the BPM.PMCON.FASTWKUP bit.

- configure the PM.FASTSLEEP.FASTRCOSC field to use the RCFAST main clock.

- enter the WAIT or RETENTION mode

Upon a wakeup, this is required to keep the main clock connected to RCFAST until the voltage regulation system is fully ready (when BPM.ISR.PSOK bit is one). During this wakeup period, the FLASHCALW module is automatically configured to operate in “1 wait state mode”.

7.1.4.3 Wake time from BACKUP mode

It is equal to the Core domain logic reset latency (similar to the reset latency caused by an external reset in RESET_N pin) added to the time required for the voltage regulation system to be stabilized.

8. Debug and Test

8.1 Features

- **IEEE1149.1 compliant JTAG Debug Port**
- **Serial Wire Debug Port**
- **Boundary-Scan chain on all digital pins for board-level testing**
- **Direct memory access and programming capabilities through debug ports**
- **Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches**
- **Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling**
- **Instrumentation Trace Macrocell (ITM) for support of printf style debugging**
- **Chip Erase command and status**
- **Unlimited Flash User page read access**
- **Cortex-M4 core reset source**
- **CRC32 of any memory accessible through the bus matrix**
- **Debugger Hot Plugging**

8.2 Overview

Debug and test features are made available to external tools by:

- The Enhanced Debug Port (EDP) embedding:
  - a Serial Wire Debug Port (SW-DP) part of the ARM coresight architecture
  - an IEEE 1149.1 JTAG Debug Debug Port (JTAG-DP) part of the ARM coresight architecture
  - a supplementary IEEE 1149.1 JTAG TAP machine that implements the boundary scan feature
- The System Manager Acces Port (SMAP) providing unlimited flash User page read access, CRC32 of any memory accessible through the bus matrix and Cortex-M4 core reset services
- The AHB Access Port (AHB-AP) providing Direct memory access, programming capabilities and standard debugging functions
- The Instrumentation Trace macrocell part of the ARM coresight architecture

For more information on ARM debug components, please refer to:

- ARMv7-M Architecture Reference Manual
- ARM Debug Interface v5.1 Architecture Specification document
- ARM CoreSight Architecture Specification
- ARM ETM Architecture Specification v3.5
- ARM Cortex-M4 Technical Reference Manual

8.7.5 Product Dependencies

8.7.5.1 I/O Lines

The TCK pin is dedicated to the EDP. The other debug port pins default after reset to their GPIO functionality and are automatically reassigned to the JTAG functionalities on detection of a debugger. In serial wire mode, TDI and TDO can be used as GPIO functions. Note that in serial wire mode TDO can be used as a single pin trace output.

8.7.5.2 Power Management

When a debugger is present, the connection is kept alive allowing debug operations. As a side effect, the power is never turned off. The hot plugging functionality is always available except when the system is in BACKUP Power Save Mode.

8.7.5.3 Clocks

The SWJ-DP uses the external TCK pin as its clock source. This clock must be provided by the external JTAG master device.

Some of the JTAG Instructions are used to access an Access Port (SMAP or AHB-AP). These instructions require the CPU clock to be running.

If the CPU clock is not present because the CPU is in a Power Save Mode where this clock is not provided, the Power Manager(PM) will automatically restore the CPU clock on detection of a debug access.

The RCSYS clock is used as CPU clock when the external reset is applied to ensure correct Access Port operations.

8.7.6 Module Initialization

This module is enabled as soon as a TCK falling edge is detected when RESET_N is not asserted (refer to Section 8.7.7 below). Moreover, the module is synchronously reseted as long as the TAP machine is in the TEST_LOGIC_RESET (TLR) state. It is advised asserting TMS at least 5 TCK clock periods after the debugger has been detected to ensure the module is in the TLR state prior to any operation. This module also has the ability to maintain the Cortex-M4 under reset (refer to the Section 8.7.8 ”SMAP Core Reset Request Source” on page 70).

8.7.7 Debugger Hot Plugging

The TCK pin is dedicated to the EDP. After reset has been released, the EDP detects that a debugger has been attached when a TCK falling edge arises.

Figure 8-4. Debugger Hot Plugging Detection Timings Diagram

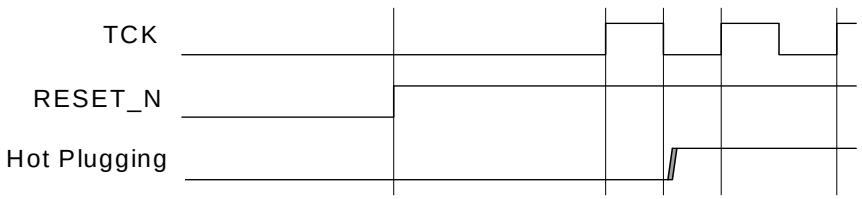
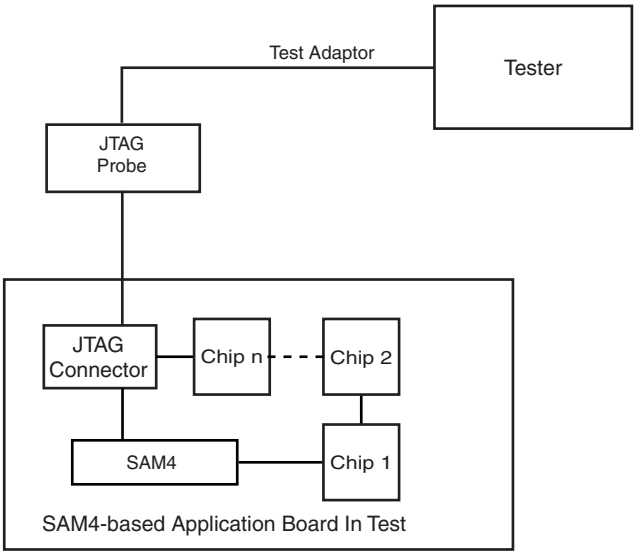


Figure 8-9. Application Test Environment Example



8.11.3 How to initialize test and debug features

To enable the JTAG pins a falling edge event must be detected on the TCK pin at any time after the RESET_N pin is released.

Certain operations requires that the system is prevented from running code after reset is released. This is done by holding low the TCK pin after the RESET_N is released. This makes the SMAP assert the core_hold_reset signal that hold the Cortex-M4 core under reset.

To make the CPU run again, clear the CHR bit in the Status Register (SR.CHR) to de-assert the core_hold_reset signal. Independent of the initial state of the TAP Controller, the Test-Logic-Reset state can always be entered by holding TMS high for 5 TCK clock periods. This sequence should always be applied at the start of a JTAG session and after enabling the JTAG pins to bring the TAP Controller into a defined state before applying JTAG commands. Applying a 0 on TMS for 1 TCK period brings the TAP Controller to the Run-Test/Idle state, which is the starting point for JTAG operations.

8.11.4 How to disable test and debug features

To disable the JTAG pins the TCK pin must be held high while RESET_N pin is released.

8.11.5 Typical JTAG sequence

Assuming Run-Test/Idle is the present state, a typical scenario for using the JTAG interface is:

8.11.5.1 Scanning in JTAG instruction

At the TMS input, apply the sequence 1, 1, 0, 0 at the rising edges of TCK to enter the Shift Instruction Register - Shift-IR state. While in this state, shift the 4 bits of the JTAG instructions into the JTAG instruction register from the TDI input at the rising edge of TCK. The TMS input must be held low during input of the 4 LSBs in order to remain in the Shift-IR state. The JTAG Instruction selects a particular Data Register as path between TDI and TDO and controls the circuitry surrounding the selected Data Register.

8.11.8 Chip erase typical procedure

The chip erase operation is triggered by writing a one in the CE bit in the Control Register (CR.CE). This clears first all volatile memories in the system and second the whole flash array. Note that the User page is not erased in this process. To ensure that the chip erase operation is completed, check the DONE bit in the Status Register (SR.DONE). Also note that the chip erase operation depends on clocks and power management features that can be altered by the CPU. It is important to ensure that it is stopped. The recommended sequence is shown below:

1. At power up, RESET_N is driven low by a debugger. The on-chip regulator holds the system in a POR state until the input supply is above the POR threshold. The system continues to be held in this static state until the internally regulated supplies have reached a safe operating.
2. PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock, and any Bus Clocks that do not have clock gate control). Internal resets are maintained due to the external reset.
   – The debug port and access ports receives a clock and leave the reset state
3. The debugger maintains a low level on TCK and release RESET_N.
   – The SMAP asserts the core_hold_reset signal
4. The Cortex-M4 core remains in reset state, meanwhile the rest of the system is released.
5. The Chip erase operation can be performed by issuing the SMAP Chip Erase command. In this case:
   – volatile memories are cleared first
   – followed by the clearing of the flash array
   – followed by the clearing of the protected state
6. After operation is completed, the chip must be restarted by either controling RESET_N or switching power off/on. Make sure that the TCK pin is high when releasing RESET_N not to halt the core.

8.11.9 Setting the protected state

This is done by issuing a specific flash controller command, for more information, refer to the Flash Controller chapter and to section 8.11.7Flash Programming typical procedure97. The protected state is defined by a highly secure Flash builtin mechanism. Note that for this programmation to propagate, it is required to reset the chip.

Table 9-3. Supply Rise Rates and Order [1]

VDDIO, VDDIN and VDDANA must be connected together and as a consequence, rise synchronously

Symbol	Parameter	Rise Rate			
		Min	Max	Unit	Comment
V_{VDDIO}	DC supply peripheral I/Os	0.0001	2.5	V/µs	
V_{VDDIN}	DC supply peripheral I/Os and internal regulator	0.0001	2.5	V/µs	
V_{VDDANA}	Analog supply voltage	0.0001	2.5	V/µs	

1. These values are based on characterization. These values are not covered by test limits in production.

– All other peripheral clocks stopped
- I/Os are inactive with internal pull-up
- CPU is running on flash with 1 wait state
- Low power cache enabled
- BOD18 and BOD33 disabled

Table 9-8. ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 1

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	205	224	µA/MHz
		85°C		212	231	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	213	244	
		85°C		230	270	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	95	112	
		85°C		100	119	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	100	128	
		85°C		107	138	
SLEEP0	Switching mode	25°C	9 * Main clock cycles	527	627	µA
		85°C		579	739	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	369	445	
		85°C		404	564	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	305	381	
		85°C		334	442	
SLEEP3	Linear mode	25°C		46	55	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	4.7	7.5	
	OSC32K and AST stopped Fast wake-up enable			3.5	6.3	
RETENTION	OSC32K running AST running at 1kHz		1.5µs	2.6	4.8	
	AST and OSC32K stopped			1.5	4	
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

9.6 I/O Pin Characteristics

9.6.1 Normal I/O Pin

Table 9-13. Normal I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			V
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			0.8	mA
			2.7V<V_{VDD}<3.6V			1.6	mA
		ODCR0=1	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	mA
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			0.8	mA
			2.7V<V_{VDD}<3.6V			1.6	mA
		ODCR0=1	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	mA
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, load = 25pF			35	ns
		OSRR0=1				45	ns
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, load = 25pF			19	ns
		OSRR0=1				23	ns
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, load = 25pF			36	ns
		OSRR0=1				47	ns
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, load = 25pF			20	ns
		OSRR0=1				24	ns
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			17	MHz
		OSRR0=1				15	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			27	MHz
		OSRR0=1				23	MHz
I_{LEAK}	Input leakage current(3)		Pull-up resistors disabled		0.01	1	µA
C_{IN}	Input capacitance(2)				5		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization

3. These values are based on characterization. These values are not covered by test limits in production

9.6.2 High-drive I/O Pin : PA02, PC04, PC05, PC06

Table 9-14. High-drive I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.8	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			22	MHz
		OSRR0=1				17	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			35	MHz
		OSRR0=1				26	MHz
I_{LEAK}	Input leakage current(3)	Pull-up resistors disabled			0.01	2	µA
C_{IN}	Input capacitance(2)				10		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.7.9 80MHz RC Oscillator (RC80M) Characteristics

Table 9-32. Internal 80 MHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)	After calibration Note that RC80M is not available in PS1	60	80	100	MHz
I_{RC80M}	Current consumption (2)			330		µA
$t_{STARTUP}$	Startup time(1)		0.57	1.72	3.2	µs
Duty	Duty cycle(2)		45	50	55	%

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.8 Flash Characteristics

Table 9-33 gives the device maximum operating frequency depending on the number of flash wait states and the flash read mode. The FWS bit in the FLASHCALW FCR register controls the number of wait states used when accessing the flash memory.

Table 9-33. Maximum Operating Frequency (1)

PowerScaling Mode	Flash Read Mode	Flash Wait States	Maximum Operating Frequency	Unit
0	Low power (HSDIS) + Flash internal reference: BPM.PMCON.FASTWKUP=1	1	12	MHz
	Low power(HSDIS)	0	18	
		1	36	
1	Low power (HSDIS) + Flash internal reference: BPM.PMCON.FASTWKUP=1	1	12	
	Low power (HSDIS)	0	8	
		1	12	
2	High speed (HSEN)	0	24	
		1	48	

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-34. Flash Characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{FPP}	Page programming time	f_{CLK_AHB} = 48MHz		4.38		ms
t_{FPE}	Page erase time			4.38		
t_{FFP}	Fuse programming time			0.63		
t_{FEA}	Full chip erase time (EA)			5.66		
t_{FCE}	JTAG chip erase time (CHIP_ERASE)	f_{CLK_AHB} = 115kHz		304		

9.9.5 Digital to Analog Converter Characteristics

Table 9-49. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Analog Supply Voltage (1)	on VDDANA	2.4	3	3.6	V
	Digital Supply Voltage(1)	on VDDCORE	1.62	1.8	1.98	V
	Resolution (2)			10		bits
	Clock frequency(1)	Cload = 50pF ; Rload = 5kΩ			500	kHz
	Load(1)	CLoad			50	pF
		RLoad	5			kΩ
INL	Integral Non Linearity (1)	Best fit-line method			±2	LSBs
DNL	Differential Non Linearity (1)	Best fit-line method	-0.9		+1	LSBs
	Zero Error (offset) (1)	CDR[9:0] = 0		1	5	mV
	Gain Error (1)	CDR[9:0] = 1023		5	10	mV
	Total Harmonic Distortion(1)	80% of VDDANA @ fin = 70kHz	-56		7	dB
	Delay to vout (1)	CDR[9:0] = 512/ Cload = 50 pF / Rload = 5 kΩ	2			µs
	Startup time(1)	CDR[9:0] = 512	5		9	µs
	Output Voltage Range	(ADVREFP < VDDANA – 100mV) is mandatory	0		ADVREFP	V
	ADVREFP Voltage Range(1)	(ADVREFP < VDDANA – 100mV) is mandatory	2.3		3.5	V
	ADVREFN Voltage Range(1)	ADVREFP = GND		0		V
	Standby Current(1)	On VDDANA			500	nA
		On VDDCORE			100	
	DC Current consumption(1)	On VDDANA (no Rload)		485	660	µA
		On ADVREFP (CDR[9:0] = 512)		250	295	

1. These values are based on simulation. These values are not covered by test limits in production or characterization
2. These values are based on characterization. These values are not covered by test limits in production

9.9.6 Analog Comparator Characteristics

Table 9-50. Analog Comparator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Positive input voltage range		0.1		VDDIO-0.1	V
	Negative input voltage range		0.1		VDDIO-0.1	
	Offset (1)	V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 0 (2) Fast mode	-12		13	mV
		V_{ACREFN} =0.1V to VDDIO-0.1V, hysteresis = 0(2) Low power mode	-11		12	mV

10. Mechanical Characteristics

10.1 Thermal Considerations

10.1.1 Thermal Data

Table 10-1 summarizes the thermal resistance data depending on the package.

Table 10-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP100	48.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP100	13.3	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	VFBGA100	31.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		VFBGA100	6.9	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	WLCSP64	26.9	°C/W
θ_{JC}	Junction-to-case thermal resistance		WLCSP64	0.2	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP64	49.6	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP64	13.5	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN64	22.0	°C/W
θ_{JC}	Junction-to-case thermal resistance		QFN64	1.3	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP48	51.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP48	13.7	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN48	24.9	°C/W
θ_{JC}	Junction-to-case thermal resistance		QFN48	1.3	

10.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

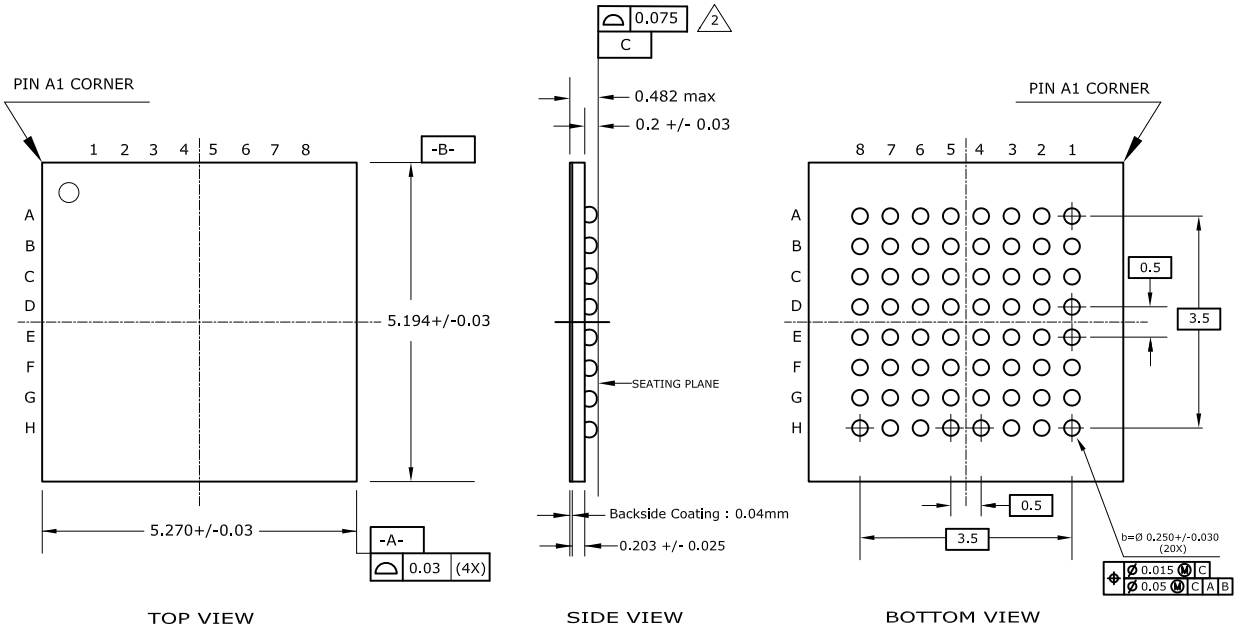
1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 10-1.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 10-1.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in Section 9.5 on page 103.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Figure 10-5. WLCSP64 SAM4LC8 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.75	1.75
A2	GNDANA	1.75	1.25
A3	ADVREFP	1.75	0.75
A4	VDDANA	1.75	0.25
A5	PA09	1.75	-0.25
A6	CAPL	1.75	-0.75
A7	CAPH	1.75	-1.25
A8	PA12	1.75	-1.75
B1	PB03	1.25	1.75
B2	XIN32	1.25	1.25
B3	XOUT32	1.25	0.75
B4	PA08	1.25	0.25
B5	PB06	1.25	-0.25
B6	PA10	1.25	-0.75
B7	PA11	1.25	-1.25
B8	VLCD	1.25	-1.75
C1	VDDIN	0.75	1.75
C2	PB01	0.75	1.25
C3	PA05	0.75	0.75
C4	PA06	0.75	0.25
C5	PA07	0.75	-0.25
C6	PB07	0.75	-0.75

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	0.75	-1.25
C8	BIAS1	0.75	-1.75
D1	VDDOUT	0.25	1.75
D2	PB00	0.25	1.25
D3	PA04	0.25	0.75
D4	PB05	0.25	0.25
D5	PB12	0.25	-0.25
D6	PB08	0.25	-0.75
D7	PA14	0.25	-1.25
D8	BIAS2	0.25	-1.75
E1	GNDIN	-0.25	1.75
E2	PA03	-0.25	1.25
E3	PB02	-0.25	0.75
E4	RESET_N	-0.25	0.25
E5	PB13	-0.25	-0.25
E6	PB09	-0.25	-0.75
E7	PA15	-0.25	-1.25
E8	GNDIO0	-0.25	-1.75
F1	VDDCORE	-0.75	1.75
F2	TCK	-0.75	1.25
F3	PA02	-0.75	0.75
F4	PB14	-0.75	0.25

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.75	-0.25
F6	PB10	-0.75	-0.75
F7	PA16	-0.75	-1.25
F8	VLCDIN	-0.75	-1.75
G1	GNDIO1	-1.25	1.75
G2	PA26	-1.25	1.25
G3	PA24	-1.25	0.75
G4	PA00	-1.25	0.25
G5	PA01	-1.25	-0.25
G6	PA19	-1.25	-0.75
G7	PA18	-1.25	-1.25
G8	PA17	-1.25	-1.75
H1	VDDIO1	-1.75	1.75
H2	PA25	-1.75	1.25
H3	PA23	-1.75	0.75
H4	PB15	-1.75	0.25
H5	PA21	-1.75	-0.25
H6	VDDIO0	-1.75	-0.75
H7	PA20	-1.75	-1.25
H8	PB11	-1.75	-1.75

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-14. Device and Package Maximum Weight

14.8	mg

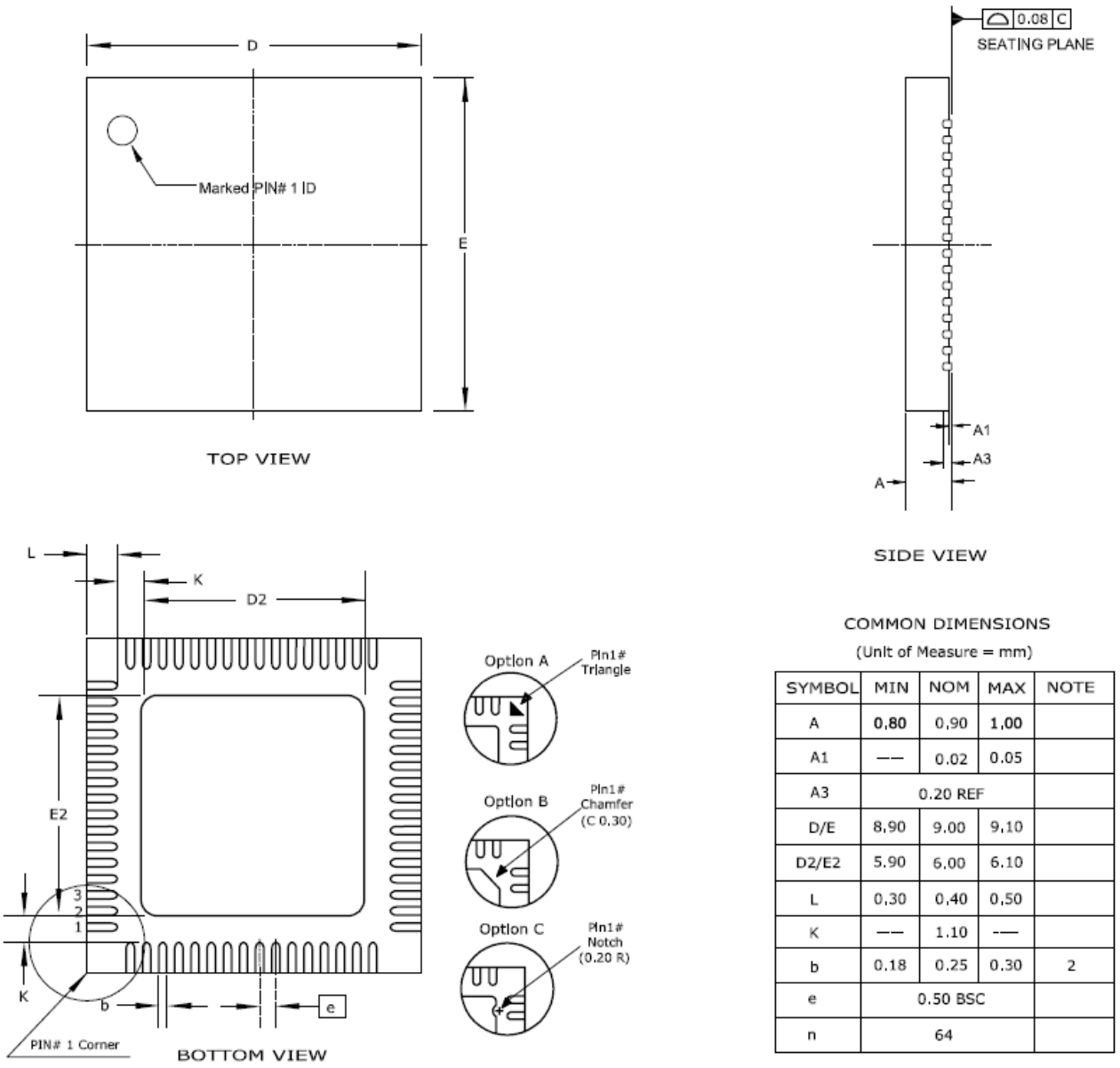
Table 10-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-16. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

Figure 10-8. QFN-64 Package Drawing



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	—	0.02	0.05	
A3		0.20 REF		
D/E	8.90	9.00	9.10	
D2/E2	5.90	6.00	6.10	
L	0.30	0.40	0.50	
K	—	1.10	—	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		64		

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 10-23. Device and Package Maximum Weight

200	mg

Table 10-24. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3