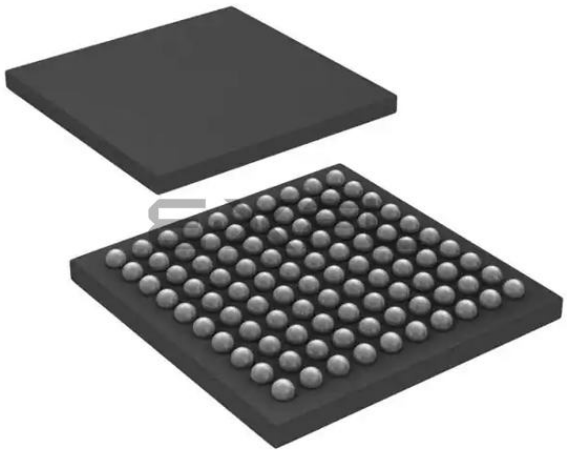

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	80
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls2ca-cfur

Figure 3-5. ATSAM4LC TQFP48/QFN48 Pinout

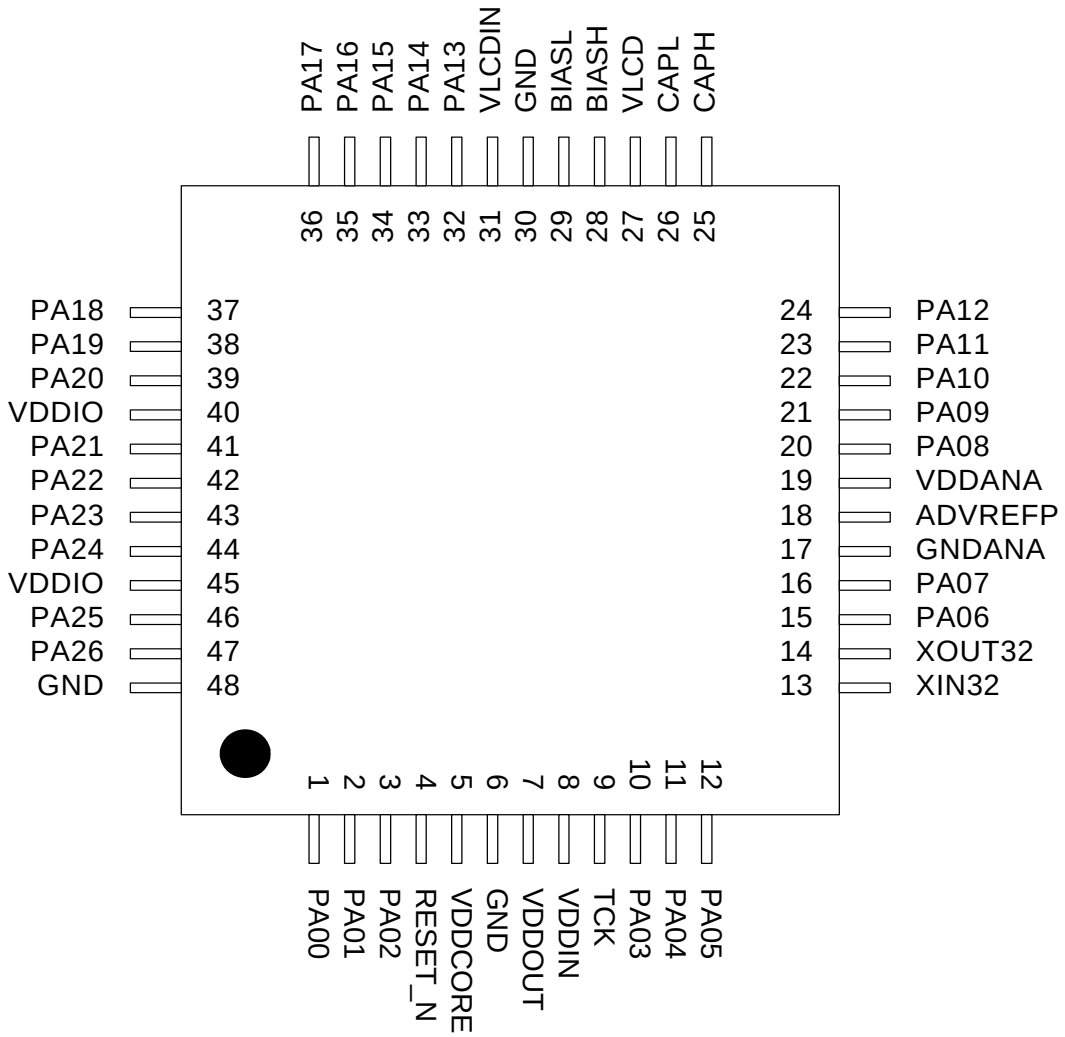
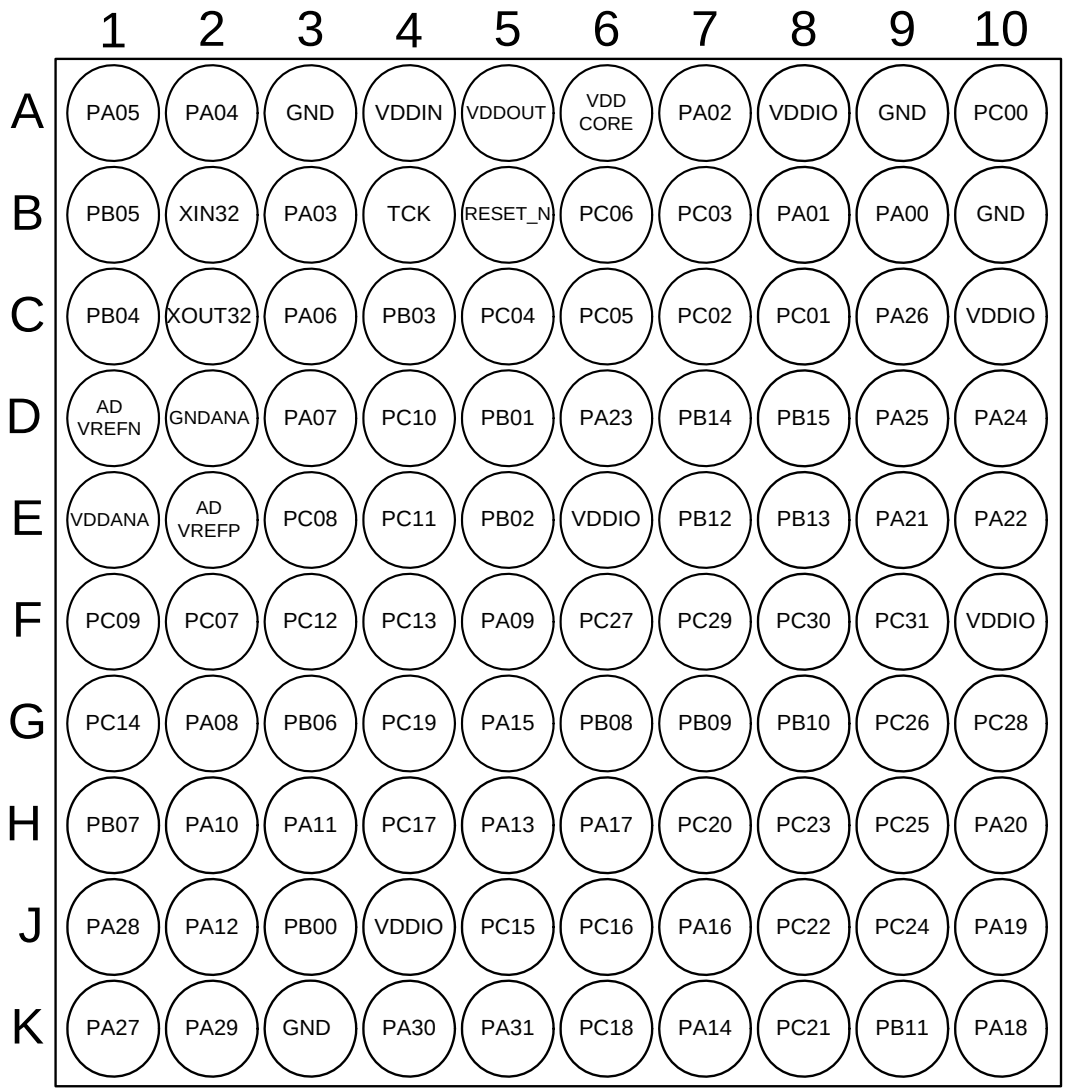


Figure 3-7. ATSAM4LS VFBGA100 Pinout



3.2 Peripheral Multiplexing on I/O lines

3.2.1 Multiplexed Signals

Each GPIO line can be assigned to one of the peripheral functions. The following tables (Section 3-1 ”100-pin GPIO Controller Function Multiplexing” on page 19 to Section 3-4 ”48-pin GPIO Controller Function Multiplexing” on page 28) describes the peripheral signals multiplexed to the GPIO lines.

Peripheral functions that are not relevant in some parts of the family are grey-shaded.

For description of differents Supply voltage source, refer to the Section 6. ”Power and Startup Considerations” on page 46.

Table 3-1. 100-pin GPIO Controller Function Multiplexing (Sheet 1 of 4)

ATSAM4LC		ATSAM4LS		Pin	GPIO	Supply	GPIO Functions						
QFN	VFBGA	QFN	VFBGA				A	B	C	D	E	F	G
5	B9	5	B9	PA00	0	VDDIO							
6	B8	6	B8	PA01	1	VDDIO							
12	A7	12	A7	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
19	B3	19	B3	PA03	3	VDDIN		SPI MISO					
24	A2	24	A2	PA04	4	VDDANA	ADCIFE AD0	USART0 CLK	EIC EXTINT2	GLOC IN1			CATB SENSE0
25	A1	25	A1	PA05	5	VDDANA	ADCIFE AD1	USART0 RXD	EIC EXTINT3	GLOC IN2	ADCIFE TRIGGER		CATB SENSE1
30	C3	30	C3	PA06	6	VDDANA	DACC VOUT	USART0 RTS	EIC EXTINT1	GLOC IN0	ACIFC ACAN0		CATB SENSE2
31	D3	31	D3	PA07	7	VDDANA	ADCIFE AD2	USART0 TXD	EIC EXTINT4	GLOC IN3	ACIFC ACAP0		CATB SENSE3
44	G2	44	G2	PA08	8	LCDA	USART0 RTS	TC0 A0	PEVC PAD EVT0	GLOC OUT0		LCDCA SEG23	CATB SENSE4
47	F5	47	F5	PA09	9	LCDA	USART0 CTS	TC0 B0	PEVC PAD EVT1	PARC PCDATA0		LCDCA COM3	CATB SENSE5
48	H2	48	H2	PA10	10	LCDA	USART0 CLK	TC0 A1	PEVC PAD EVT2	PARC PCDATA1		LCDCA COM2	CATB SENSE6
49	H3	49	H3	PA11	11	LCDA	USART0 RXD	TC0 B1	PEVC PAD EVT3	PARC PCDATA2		LCDCA COM1	CATB SENSE7
50	J2	50	J2	PA12	12	LCDA	USART0 TXD	TC0 A2		PARC PCDATA3		LCDCA COM0	CATB DIS
63	H5	63	H5	PA13	13	LCDA	USART1 RTS	TC0 B2	SPI NPCS1	PARC PCDATA4		LCDCA SEG5	CATB SENSE8
64	K7	64	K7	PA14	14	LCDA	USART1 CLK	TC0 CLK0	SPI NPCS2	PARC PCDATA5		LCDCA SEG6	CATB SENSE9
65	G5	65	G5	PA15	15	LCDA	USART1 RXD	TC0 CLK1	SPI NPCS3	PARC PCDATA6		LCDCA SEG7	CATB SENSE10

Table 4-2. Interrupt Request Signal Map (Sheet 3 of 3)

Line	Module	Signal
48	External Interrupt Controller	EIC 4
49	External Interrupt Controller	EIC 5
50	External Interrupt Controller	EIC 6
51	External Interrupt Controller	EIC 7
52	External Interrupt Controller	EIC 8
53	Inter-IC Sound (I2S) Controller	IISC
54	Serial Peripheral Interface	SPI
55	Timer/Counter	TC00
56	Timer/Counter	TC01
57	Timer/Counter	TC02
58	Timer/Counter	TC10
59	Timer/Counter	TC11
60	Timer/Counter	TC12
61	Two-wire Master Interface	TWIM0
62	Two-wire Slave Interface	TWIS0
63	Two-wire Master Interface	TWIM1
64	Two-wire Slave Interface	TWIS1
65	Universal Synchronous Asynchronous Receiver Transmitter	USART0
66	Universal Synchronous Asynchronous Receiver Transmitter	USART1
67	Universal Synchronous Asynchronous Receiver Transmitter	USART2
68	Universal Synchronous Asynchronous Receiver Transmitter	USART3
69	ADC controller interface	ADCIFE
70	DAC Controller	DACC
71	Analog Comparator Interface	ACIFC
72	Audio Bitstream DAC	ABDACB
73	True Random Number Generator	TRNG
74	Parallel Capture	PARC
75	Capacitive Touch Module B	CATB
77	Two-wire Master Interface	TWIM2
78	Two-wire Master Interface	TWIM3
79	LCD Controller A	LCDCA

Memory	Start Address	Size
		ATSAM4Lx8
AESA	0x400B0000	256 bytes
Peripheral Bridge C	0x400E0000	64 Kbytes
Peripheral Bridge D	0x400F0000	64 Kbytes

Table 5-2. Flash Memory Parameters

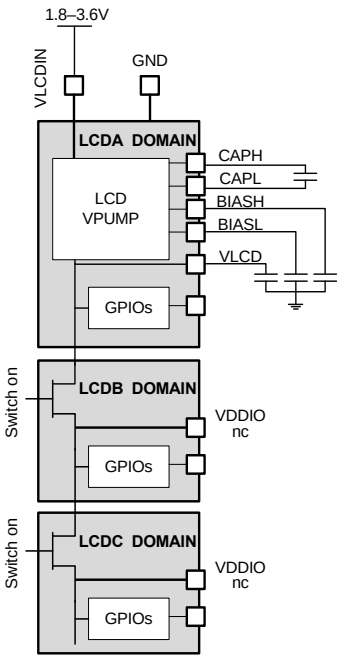
Device	Flash Size (*FLASH_PW*)	Number of Pages (*FLASH_P*)	Page Size (*FLASH_W*)
ATSAM4Lx8	512 Kbytes	1024	512 bytes
ATSAM4Lx4	256 Kbytes	512	512 bytes
ATSAM4Lx2	128 Kbytes	256	512 bytes

connected to an external voltage source (1.8-3.6V). LCDB cluster is not available in 64 and 48 pin packages

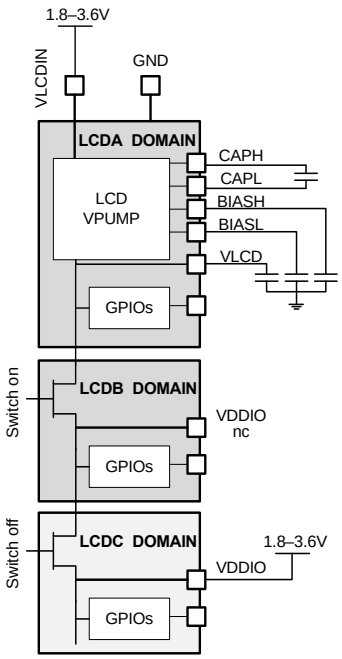
Table 6-1. LCD powering when using the internal voltage pump

Package	Segments in use	VDDIO LCDB	VDDIO LCDC
100-pin packages	[1,24]	1.8-3.6V	1.8-3.6V
	[1, 32]	nc	1.8-3.6V
	[1, 40]	nc	nc
64-pin packages	[1,15]	-	1.8-3.6V
	[1, 23]	-	nc
48-pin packages	[1,9]	-	1.8-3.6V
	[1,13]	-	nc

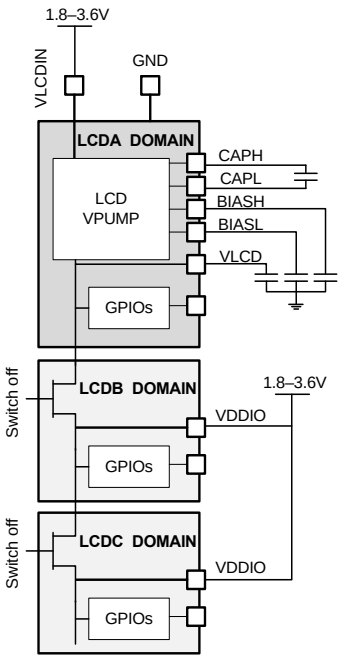
Up to 4x40 segments
No GPIO in LCD clusters



Up to 4x32 segments
Up to 8 GPIOs in LCDC clusters



Up to 4x24 segments
Up to 16 GPIOs in LCDB & LCDC clusters



7.1.3 BACKUP Mode

The BACKUP mode allows achieving the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time.

The Core domain is powered-off. The internal SRAM and register contents of the Core domain are lost. The Backup domain is kept powered-on. The 32kHz clock (RC32K or OSC32K) is kept running if enabled to feed modules that require clocking.

In BACKUP mode, the configuration of the I/O lines is preserved. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677 to have more details.

7.1.3.1 Entering BACKUP Mode

The Backup mode is entered by using the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 1.

7.1.3.2 Exiting BACKUP Mode

Exit from BACKUP mode happens if a reset occurs or if an enabled wake up event occurs.

The reset sources are:

- BOD33 reset
- BOD18 reset
- WDT reset
- External reset in RESET_N pin

The wake up sources are:

- EIC lines (level transition only)
- BOD33 interrupt
- BOD18 interrupt
- AST alarm, periodic, overflow
- WDT interrupt

The RC32K or OSC32K should be used as clock source for modules if required. The PMCON.CK32S is used to select one of these two 32kHz clock sources.

Exiting the BACKUP mode is triggered by:

- a reset source: an internal reset sequence is performed according to the reset source. Once VDDCORE is stable and has the correct value according to RUN0 mode, the internal reset is released and program execution starts. The corresponding reset source is flagged in the Reset Cause register (RCAUSE) of the PM.
- a wake up source: the Backup domain is not reset. An internal reset is generated to the Core domain, and the system switches back to the previous RUN mode. Once VDDCORE is stable and has the correct value, the internal reset in the Core domain is released and program execution starts. The BKUP bit is set in the Reset Cause register (RCAUSE) of the PM. It allows the user to discriminate between the reset cause and a wake up cause from the BACKUP mode. The wake up cause can be found in the Backup Wake up Cause register (BPM.BKUPWCAUSE).

8.5 Product dependencies

8.5.1 I/O Lines

Refer to Section 1.1.5.1 ”I/O Lines” on page 5.

8.5.2 Power management

Refer to Section 1.1.5.2 ”Power Management” on page 5.

8.5.3 Clocks

Refer to Section 1.1.5.3 ”Clocks” on page 5.

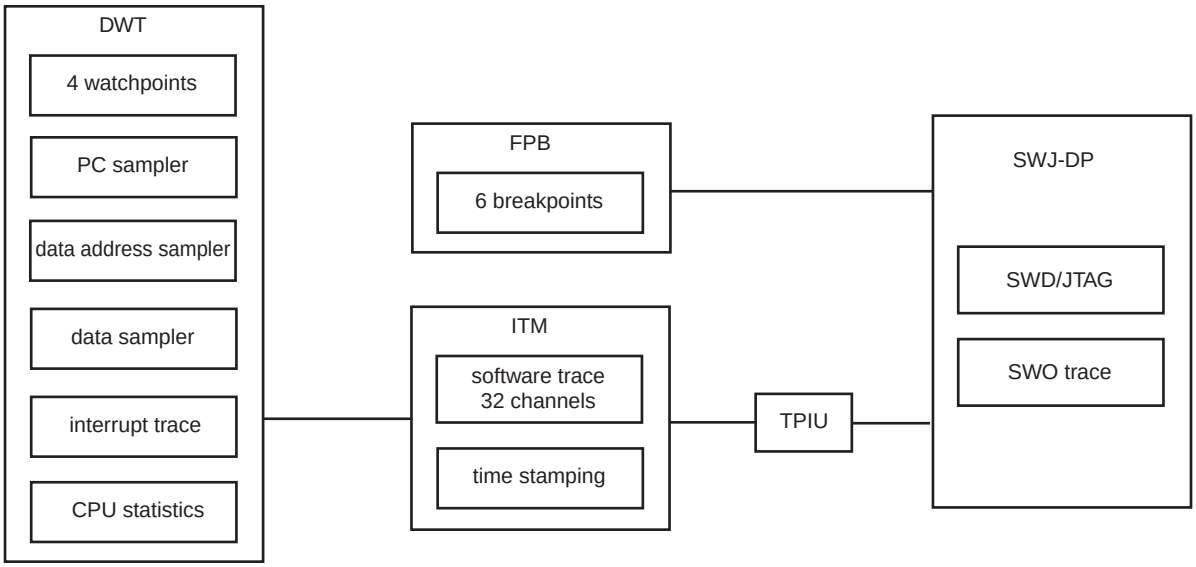
8.6 Core debug

Figure 8-2 shows the Debug Architecture used in the SAM4L. The Cortex-M4 embeds four functional units for debug:

- FPB (Flash Patch Breakpoint)
- DWT (Data Watchpoint and Trace)
- ITM (Instrumentation Trace Macrocell)
- TPIU (Trace Port Interface Unit)

The debug architecture information that follows is mainly dedicated to developers of SWJ-DP Emulators/Probes and debugging tool vendors for Cortex-M4 based microcontrollers. For further details on SWJ-DP see the Cortex-M4 technical reference manual.

Figure 8-2. Debug Architecture



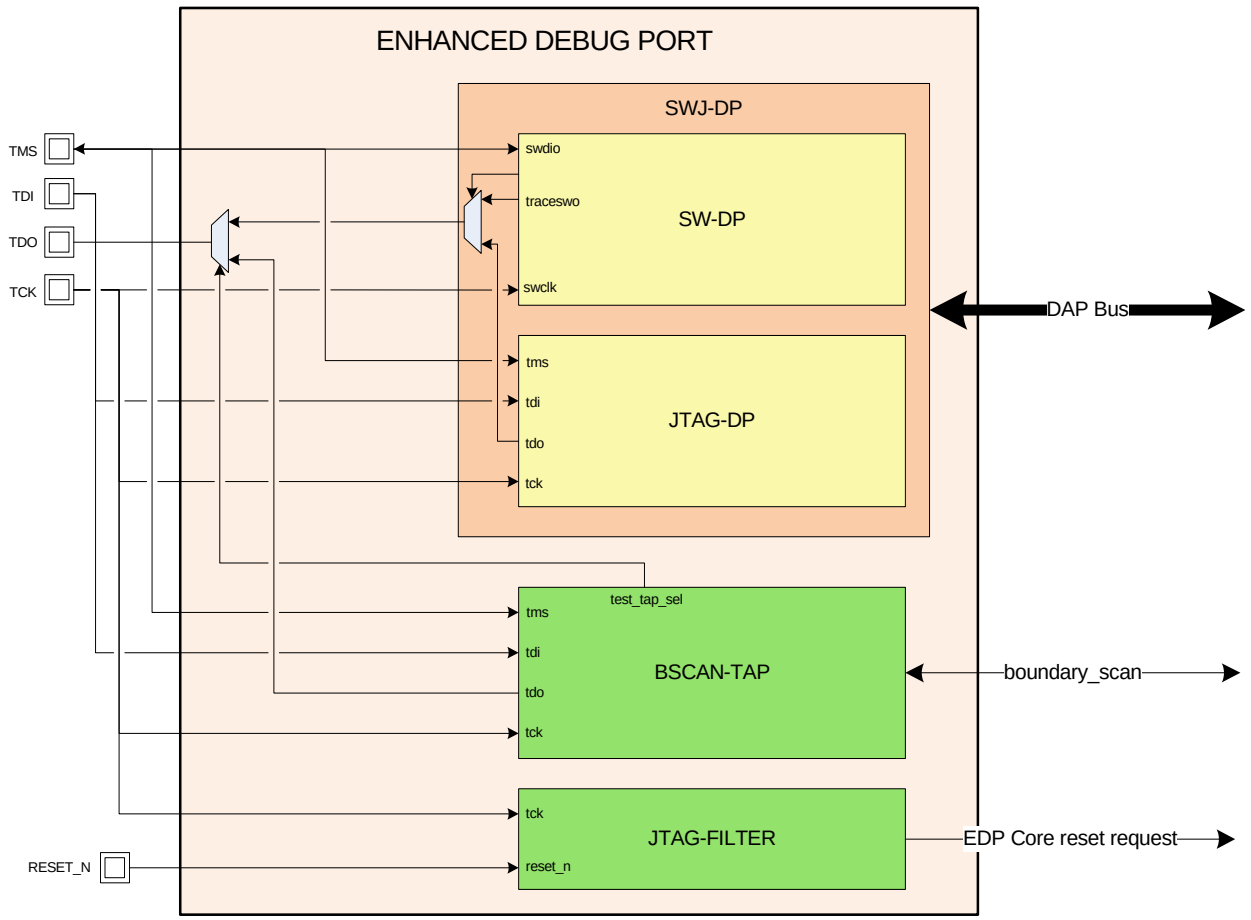
8.6.1 FPB (Flash Patch Breakpoint)

The FPB:

- Implements hardware breakpoints
- Patches (on the fly) code and data being fetched by the Cortex-M4 core from code space with data in the system space. Definition of code and system spaces can be found in the System Address Map section of the ARMv7-M Architecture Reference Manual.

8.7.3 Block Diagram

Figure 8-3. Enhanced Debug Port Block Diagram



8.7.4 I/O Lines Description

Table 8-1. I/O Lines Description

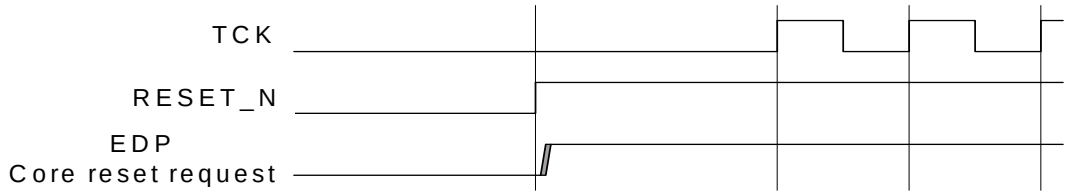
Name	JTAG Debug Port		SWD Debug Port	
	Type	Description	Type	Description
TCK/SWCLK	I	Debug Clock	I	Serial Wire Clock
TDI	I	Debug Data in	-	NA
TDO/TRACESWO	O	Debug Data Out	O	Trace asynchronous Data Out
TMS/SWDIO	I	Debug Mode Select	I/O	Serial Wire Input/Output
RESET_N	I	Reset	I	Reset

The Debug Port pins assignation is then forced to the EDP function even if they were already assigned to another module. This allows to connect a debugger at any time without reseting the device. The connection is non-intrusive meaning that the chip will continue its execution without being disturbed. The CPU can of course be halted later on by issuing Cortex-M4 OCD features.

8.7.8 SMAP Core Reset Request Source

The EDP has the ability to send a request to the SMAP for a Cortex-M4 Core reset. The procedure to do so is to hold TCK low until RESET_N is released. This mechanism aims at halting the CPU to prevent it from changing the system configuration while the SMAP is operating.

Figure 8-5. SMAP Core Reset Request Timings Diagram



The SMAP can de-assert the core reset request for this operation, refer to Section 2.8.8 ”Cortex-M4 Core Reset Source” on page 57.

8.7.9 SWJ-DP

The Cortex-M4 embeds a SWJ-DP Debug port which is the standard CoreSight™ debug port. It combines Serial Wire Debug Port (SW-DP), from 2 to 3 pins and JTAG debug Port(JTAG-DP), 5 pins.

By default, the JTAG Debug Port is active. If the host debugger wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables JTAG-DP and enables SW-DP.

When the EDP has been switched to Serial Wire mode, TDO/TRACESWO can be used for trace (for more information refer to the section below). The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP.

The SWJ-DP provides access to the AHB-AP and SMAP access ports which have the following APSEL value:

Figure 8-6. Access Ports APSEL

Acces Port (AP)	APSEL
AHB-AP	0
SMAP	1

Refer to the ARM Debug Interface v5.1 Architecture Specification for more details on SWJ-DP.

8.9.11.7 Module Version

Name: VERSION

Access Type: Read-Only

Offset: 0x28

Reset Value: -

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	VARIANT			

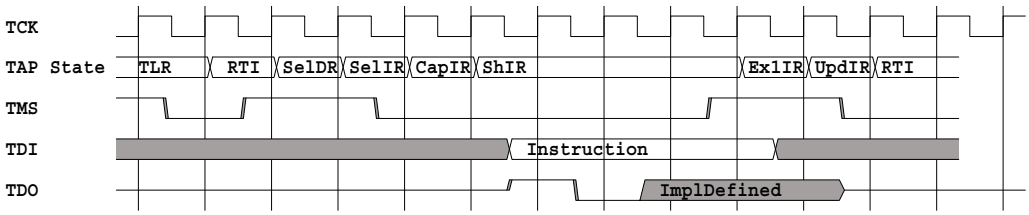
15	14	13	12	11	10	9	8
-	-	-	-	VERSION			

7	6	5	4	3	2	1	0
VERSION							

- **VARIANT: Variant number**
  Reserved. No functionality associated.
- **VERSION: Version number**
  Version number of the module. No functionality associated.

Apply the TMS sequence 1, 1, 0 to re-enter the Run-Test/Idle state. The instruction is latched onto the parallel output from the shift register path in the Update-IR state. The Exit-IR, Pause-IR, and Exit2-IR states are only used for navigating the state machine.

Figure 8-10. Scanning in JTAG instruction



8.11.5.2 Scanning in/out data

At the TMS input, apply the sequence 1, 0, 0 at the rising edges of TCK to enter the Shift Data Register - Shift-DR state. While in this state, upload the selected Data Register (selected by the present JTAG instruction in the JTAG Instruction Register) from the TDI input at the rising edge of TCK. In order to remain in the Shift-DR state, the TMS input must be held low. While the Data Register is shifted in from the TDI pin, the parallel inputs to the Data Register captured in the Capture-DR state is shifted out on the TDO pin.

Apply the TMS sequence 1, 1, 0 to re-enter the Run-Test/Idle state. If the selected Data Register has a latched parallel-output, the latching takes place in the Update-DR state. The Exit-DR, Pause-DR, and Exit2-DR states are only used for navigating the state machine.

As shown in the state diagram, the Run-Test/Idle state need not be entered between selecting JTAG instruction and using Data Registers.

8.11.6 Boundary-Scan

The Boundary-Scan chain has the capability of driving and observing the logic levels on the digital I/O pins, as well as the boundary between digital and analog logic for analog circuitry having off-chip connections. At system level, all ICs having JTAG capabilities are connected serially by the TDI/TDO signals to form a long shift register. An external controller sets up the devices to drive values at their output pins, and observe the input values received from other devices. The controller compares the received data with the expected result. In this way, Boundary-Scan provides a mechanism for testing interconnections and integrity of components on Printed Circuits Boards by using the 4 TAP signals only.

The four IEEE 1149.1 defined mandatory JTAG instructions IDCODE, BYPASS, SAMPLE/PRELOAD, and EXTEST can be used for testing the Printed Circuit Board. Initial scanning of the data register path will show the ID-code of the device, since IDCODE is the default JTAG instruction. It may be desirable to have the device in reset during test mode. If not reset, inputs to the device may be determined by the scan operations, and the internal software may be in an undetermined state when exiting the test mode. Entering reset, the outputs of any Port Pin will instantly enter the high impedance state, making the HIGHZ instruction redundant. If needed, the BYPASS instruction can be issued to make the shortest possible scan chain through the device. The device can be set in the reset state by pulling the external RESET_N pin low.

The EXTEST instruction is used for sampling external pins and loading output pins with data. The data from the output latch will be driven out on the pins as soon as the EXTEST instruction is loaded into the JTAG IR-register. Therefore, the SAMPLE/PRELOAD should also be used for setting initial values to the scan ring, to avoid damaging the board when issuing the EXTEST

Table 9-12. Typical Current Consumption by Peripheral in Power Scaling Mode 1 [1]

Peripheral	Typ Consumption Active	Unit
IISC	0.5	µA/MHz
SPI	1.1	
TC	3.1	
TWIM	0.8	
TWIS	0.7	
USART	4.4	
ADCIFE[2]	1.6	
DACC	0.6	
ACIFC [2]	1.6	
GLOC	0.1	
ABDACB	0.3	
TRNG	0.3	
PARC	0.3	
CATB	1.5	
LCDCA	2.2	
PDCA	0.4	
CRCCU	0.3	
USBC	0.9	
PEVC	2.8	
CHIPID	0.1	
SCIF	3.1	
FREQM	0.2	
GPIO	3.4	
BPM	0.4	
BSCIF	2.3	
AST	0.8	
WDT	0.8	
EIC	0.3	
PICOUART	0.2	

1. These numbers are valid for the measured condition only and must not be extrapolated to other frequencies
2. Includes the current consumption on VDDANA and ADVREFP.

9.6.3 USB I/O Pin : PA25, PA26

Table 9-15. USB I/O Pin Characteristics in GPIO configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V		20		mA
			2.7V<V_{VDD}<3.6V		30		
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V		20		mA
			2.7V<V_{VDD}<3.6V		30		
F_{PINMAX}	Maximum frequency(2)	ODCR0=0 OSRR0=0	load = 25pF			20	MHz
I_{LEAK}	Input leakage current(3)	Pull-up resistors disabled			0.01	1	µA
C_{IN}	Input capacitance(2)				5		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.6.4 TWI Pin : PA21, PA22, PA23, PA24, PB14, PB15

Table 9-16. TWI Pin Characteristics in TWI configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.3 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.7 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
I_{OL}	Output low-level current (3)	DRIVEL=0				0.5	mA
		DRIVEL=1				1.0	
		DRIVEL=2				1.6	
		DRIVEL=3				3.1	
		DRIVEL=4				6.2	
		DRIVEL=5				9.3	
		DRIVEL=6				15.5	
		DRIVEL=7				21.8	

Table 9-20. High Drive TWI Pin Characteristics in GPIO configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-up resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			3.4	mA
			2.7V<V_{VDD}<3.6V			6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			5.2	mA
			2.7V<V_{VDD}<3.6V			8	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			3.4	mA
			2.7V<V_{VDD}<3.6V			6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			5.2	mA
			2.7V<V_{VDD}<3.6V			8	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		18		ns
		OSRR0=1			110		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		10		ns
		OSRR0=1			50		
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		19		ns
		OSRR0=1			140		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		12		ns
		OSRR0=1			63		

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Table 9-21. Common High Drive TWI Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LEAK}	Input leakage current (1)	Pull-up resistors disabled		0.01	2	µA
C_{IN}	Input capacitance(1)			10		pF

1. These values are based on simulation. These values are not covered by test limits in production or characterization

Table 9-27. Digital Frequency Locked Loop Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{STARTUP}$	Startup time(1)	Within 90% of final values			100	µs
t_{LOCK}	Lock time(1)	f_{REF} = 32kHz, FINE lock, SSG disabled(2)		600		
		f_{REF} = 32kHz, ACCURATE lock, dithering clock = RCSYS/2, SSG disabled(2)		1100		

1. These values are based on simulation. These values are not covered by test limits in production or characterization.
2. Spread Spectrum Generator (SSG) is disabled by writing a zero to the EN bit in the SCIF.DFLL0SSG register.

9.7.5 32kHz RC Oscillator (RC32K) Characteristics

Table 9-28. 32kHz RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)	Calibrated against a 32.768kHz reference Temperature compensation disabled	20	32.768	44	kHz
I_{RC32K}	Current consumption (2)	Without temperature compensation		0.5		µA
		Temperature compensation enabled		2		µA
$t_{STARTUP}$	Startup time(1)			1		cycle

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.7.6 System RC Oscillator (RCSYS) Characteristics

Table 9-29. System RC Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)	Calibrated at 85°C	110	113.6	116	kHz
I_{RCSYS}	Current consumption (2)				12	µA
$t_{STARTUP}$	Startup time(1)		25	38	63	µs
Duty	Duty cycle(1)		49.6	50	50.3	%

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-39. VREG Electrical Characteristics in Switching mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	DC output current(1)	$V_{VDDCORE}$ > 1.65V			55	mA
	Output DC load regulation(1) Transient load regulation	I_{OUT} = 0 to 50mA, V_{VDDIN} = 3V	-136	-101	-82	mV
	Output DC regulation(1)	I_{OUT} = 50 mA, V_{VDDIN} = 2V to 3.6V	-20	38	99	mV
I_Q	Quescient current(1)	V_{VDDIN} = 2V, I_{OUT} = 0 mA	97	186	546	µA
		V_{VDDIN} > 2.2V, I_{OUT} = 0 mA	97	111	147	
P_{EFF}	Power efficiency(1)	I_{OUT} = 5mA, 50mA Reference power not included	82.7	88.3	95	%

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-40. Decoupling Requirements in Switching Mode

Symbol	Parameter	Technology	Typ	Units
C_{IN1}	Input regulator capacitor 1		33	nF
C_{IN2}	Input regulator capacitor 2		100	
C_{IN3}	Input regulator capacitor 3		10	µF
C_{OUT1}	Output regulator capacitor 1	X7R MLCC	100	nF
C_{OUT2}	Output regulator capacitor 2	X7R MLCC (ex : GRM31CR71A475)	4.7	µF
L_{EXT}	External inductance	(ex: Murata LQH3NPN220MJ0)	22	µH
R_{DCLEXT}	Serial resistance of L_{EXT}		0.7	Ω
$ISAT_{LEXT}$	Saturation current of L_{EXT}		300	mA

Note: 1. Refer to Section 6. on page 46.

Where $SPIn$ is the MISO delay, SPI6 or SPI9 depending on CPOL and NCPHA. t_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for t_{SETUP} . f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

9.10.4 TWIM/TWIS Timing

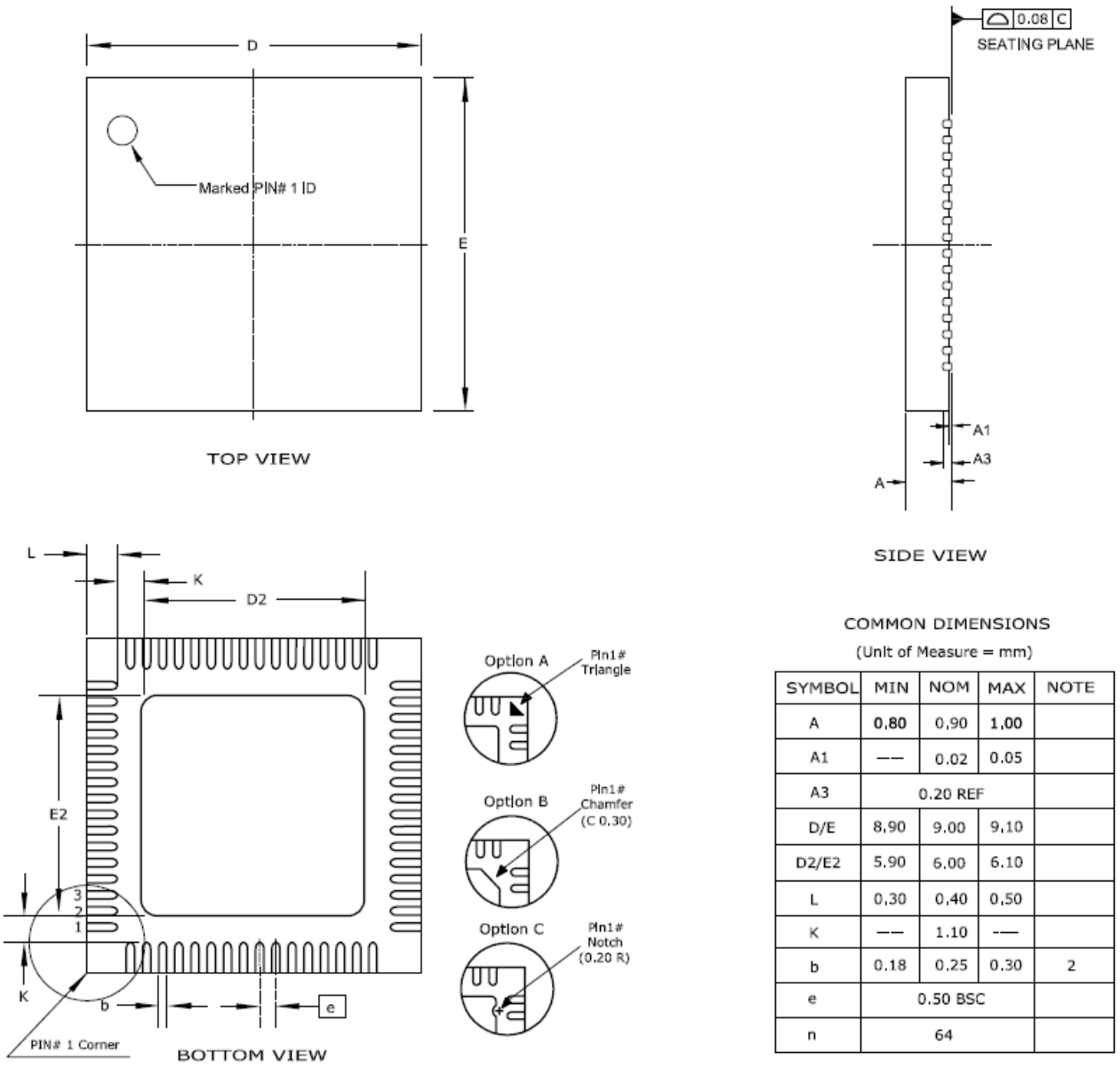
Figure 9-64 shows the TWI-bus timing requirements and the compliance of the device with them. Some of these requirements (t_r and t_f) are met by the device without requiring user intervention. Compliance with the other requirements (t_{HD-STA}, t_{SU-STA}, t_{SU-STO}, t_{HD-DAT}, $t_{SU-DAT-TWI}$, $t_{LOW-TWI}$, t_{HIGH}, and f_{TWCK}) requires user intervention through appropriate programming of the relevant TWIM and TWIS user interface registers. refer to the TWIM and TWIS sections for more information.

Table 9-64. TWI-Bus Timing Requirements

Symbol	Parameter	Mode	Minimum		Maximum		Unit
			Requirement	Device	Requirement	Device	
t_r	TWCK and TWD rise time	Standard(1)	-		1000		ns
		Fast(1)	$20 + 0.1C_b$		300		
t_f	TWCK and TWD fall time	Standard	-		300		ns
		Fast	$20 + 0.1C_b$		300		
t_{HD-STA}	(Repeated) START hold time	Standard	4	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STA}	(Repeated) START set-up time	Standard	4.7	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STO}	STOP set-up time	Standard	4.0	$4t_{clkpb}$	-		µs
		Fast	0.6				
t_{HD-DAT}	Data hold time	Standard	0.3(2)	$2t_{clkpb}$	3.45()	$15t_{prescaled} + t_{clkpb}$	µs
		Fast			0.9()		
$t_{SU-DAT-TWI}$	Data set-up time	Standard	250	$2t_{clkpb}$	-		ns
		Fast	100				
t_{SU-DAT}		-	-	t_{clkpb}	-		-
$t_{LOW-TWI}$	TWCK LOW period	Standard	4.7	$4t_{clkpb}$	-		µs
		Fast	1.3				
t_{LOW}		-	-	t_{clkpb}	-		-
t_{HIGH}	TWCK HIGH period	Standard	4.0	$8t_{clkpb}$	-		µs
		Fast	0.6				
f_{TWCK}	TWCK frequency	Standard	-		100	$\frac{1}{12t_{clkpb}}$	kHz
		Fast			400		

Notes: 1. Standard mode: $f_{TWCK} \leq 100$ kHz ; fast mode: $f_{TWCK} > 100$ kHz .

Figure 10-8. QFN-64 Package Drawing



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	—	0.02	0.05	
A3		0.20 REF		
D/E	8.90	9.00	9.10	
D2/E2	5.90	6.00	6.10	
L	0.30	0.40	0.50	
K	—	1.10	—	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		64		

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 10-23. Device and Package Maximum Weight

200	mg

Table 10-24. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3