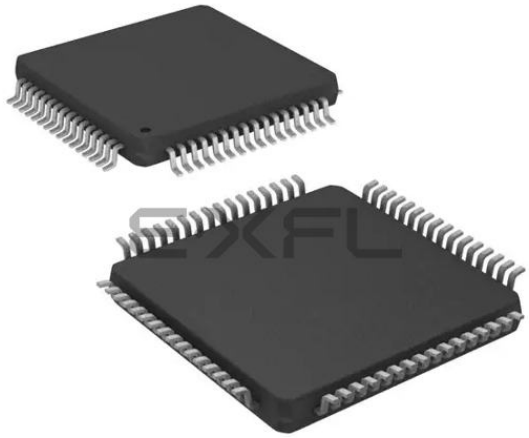

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 7x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls4ba-aur

  - PLL up to 240MHz for device clock and for USB
  - Digital Frequency Locked Loop (DFLL) with wide input range
  - Up to 16 peripheral DMA (PDCA) channels
- Peripherals
  - USB 2.0 Device and Embedded Host: 12 Mbps, up to 8 bidirectional Endpoints and Multi-packet Ping-pong Mode. On-Chip Transceiver
  - Liquid Crystal Display (LCD) Module with Capacity up to 40 Segments and up to 4 Common Terminals
  - One USART with ISO7816, IrDA®, RS-485, SPI, Manchester and LIN Mode
  - Three USART with SPI Mode
  - One PicoUART for extended UART wake-up capabilities in all sleep modes
  - Windowed Watchdog Timer (WDT)
  - Asynchronous Timer (AST) with Real-time Clock Capability, Counter or Calendar Mode Supported
  - Frequency Meter (FREQM) for Accurate Measuring of Clock Frequency
  - Six 16-bit Timer/Counter (TC) Channels with capture, waveform, compare and PWM mode
  - One Master/Slave Serial Peripheral Interface (SPI) with Chip Select Signals
  - Four Master and Two Slave Two-wire Interfaces (TWI), up to 3.4Mbit/s I^2C-compatible
  - One Advanced Encryption System (AES) with 128-bit key length
  - One 16-channel ADC 300Ksps (ADC) with up to 12 Bits Resolution
  - One DAC 500Ksps (DACC) with up to 10 Bits Resolution
  - Four Analog Comparators (ACIFC) with Optional Window Detection
  - Capacitive Touch Module (CATB) supporting up to 32 buttons
  - Audio Bitstream DAC (ABDACB) Suitable for Stereo Audio
  - Inter-IC Sound (IISC) Controller, Compliant with Inter-IC Sound (I^2S) Specification
  - Peripheral Event System for Direct Peripheral to Peripheral Communication
  - 32-bit Cyclic Redundancy Check Calculation Unit (CRCCU)
  - Random generator (TRNG)
  - Parallel Capture Module (PARC)
  - Glue Logic Controller (GLOC)
- I/O
  - Up to 75 I/O lines with external interrupt capability (edge or level sensitivity), debouncing, glitch filtering and slew-rate control
  - Up to Six High-drive I/O Pins
- Single 1.68-3.6V Power Supply
- Packages
  - 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm/100-ball VFBGA, 7x7 mm, pitch 0.65 mm
  - 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm/64-pad QFN 9x9 mm, pitch 0.5 mm
  - 64-ball WLCSP, 4,314x4,434 mm, pitch 0.5 mm for SAM4LC4/2 and SAM4LS4/2 series
  - 64-ball WLCSP, 5,270x5,194 mm, pitch 0.5 mm for SAM4LC8 and SAM4LS8 series
  - 48-lead LQFP, 7 x 7 mm, pitch 0.5 mm/48-pad QFN 7x7 mm, pitch 0.5 mm

Table 2-2. ATSAM4LC Configuration Summary

Feature	ATSAM4LC8/4/2C	ATSAM4LC8/4/2B	ATSAM4LC8/4/2A
Oscillators	Digital Frequency Locked Loop 20-150MHz (DFLL) Phase Locked Loop 48-240MHz (PLL) Crystal Oscillator 0.6-30MHz (OSC0) Crystal Oscillator 32kHz (OSC32K) RC Oscillator 80MHz (RC80M) RC Oscillator 4,8,12MHz (RCFAST) RC Oscillator 115kHz (RCSYS) RC Oscillator 32kHz (RC32K)		
ADC	15-channel	7-channel	3-channel
DAC	1-channel		
Analog Comparators	4	2	1
CATB Sensors	32	32	26
USB	1		
Audio Bitstream DAC	1		
IIS Controller	1		
Packages	TQFP/VFBGA	TQFP/QFN/ WLCSP	TQFP/QFN

.

Table 2-3. ATSAM4LS Configuration Summary

Feature	ATSAM4LS8/4/2C	ATSAM4LS8/4/2B	ATSAM4LS8/4/2A
Number of Pins	100	64	48
Max Frequency	48MHz		
Flash	512/256/128KB		
SRAM	64/32/32KB		
SEGMENT LCD	NA		
GPIO	80	48	32
High-drive pins	6	3	1
External Interrupts	8 + 1 NMI		
TWI	2 Masters + 2 Masters/Slaves		1 Master + 1 Master/Slave
USART	4		3 in LC sub series 4 in LS sub series
PICOUART	1		0
Peripheral DMA Channels	16		
AESA	NA		
Peripheral Event System	1		
SPI	1		
Asynchronous Timers	1		

Table 3-3. 64-pin GPIO Controller Function Multiplexing for WLCSP package (Sheet 3 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
WLCSP	WLCSP				A	B	C	D	E	F	G
E5	E5	PB13	45	LCDC	USART0 CLK	SPI NPCS1	PEVC PAD EVT1	TC0 CLK0	SCIF GCLK3	LCDCA SEG33	CATB SENSE0
F4	F4	PB14	46	LCDC	USART0 RXD	SPI MISO	TWIM3 TWD	TC0 CLK1	SCIF GCLK IN0	LCDCA SEG36	CATB SENSE1
H4	H4	PB15	47	LCDC	USART0 TXD	SPI MOSI	TWIM3 TWCK	TC0 CLK2	SCIF GCLK IN1	LCDCA SEG37	CATB SENSE2

5.2 Embedded Memories

- **Internal high-speed flash**
  - **512Kbytes (ATSAM4Lx8)**
  - **256Kbytes (ATSAM4Lx4)**
  - **128Kbytes (ATSAM4Lx2)**
    - **Pipelined flash architecture, allowing burst reads from sequential flash locations, hiding penalty of 1 wait state access**
    - **Pipelined flash architecture typically reduces the cycle penalty of 1 wait state operation compared to 0 wait state operation**
    - **100 000 write cycles, 15-year data retention capability**
    - **Sector lock capabilities, bootloader protection, security bit**
    - **32 fuses, erased during chip erase**
    - **User page for data to be preserved during chip erase**
- **Internal high-speed SRAM, single-cycle access at full speed**
  - **64Kbytes (ATSAM4Lx8)**
  - **32Kbytes (ATSAM4Lx4, ATSAM4Lx2)**

5.3 Physical Memory Map

The system bus is implemented as a bus matrix. All system bus addresses are fixed, and they are never remapped in any way, not even during boot. The 32-bit physical address space is mapped as follows:

Table 5-1. ATSAM4L8/L4/L2 Physical Memory Map

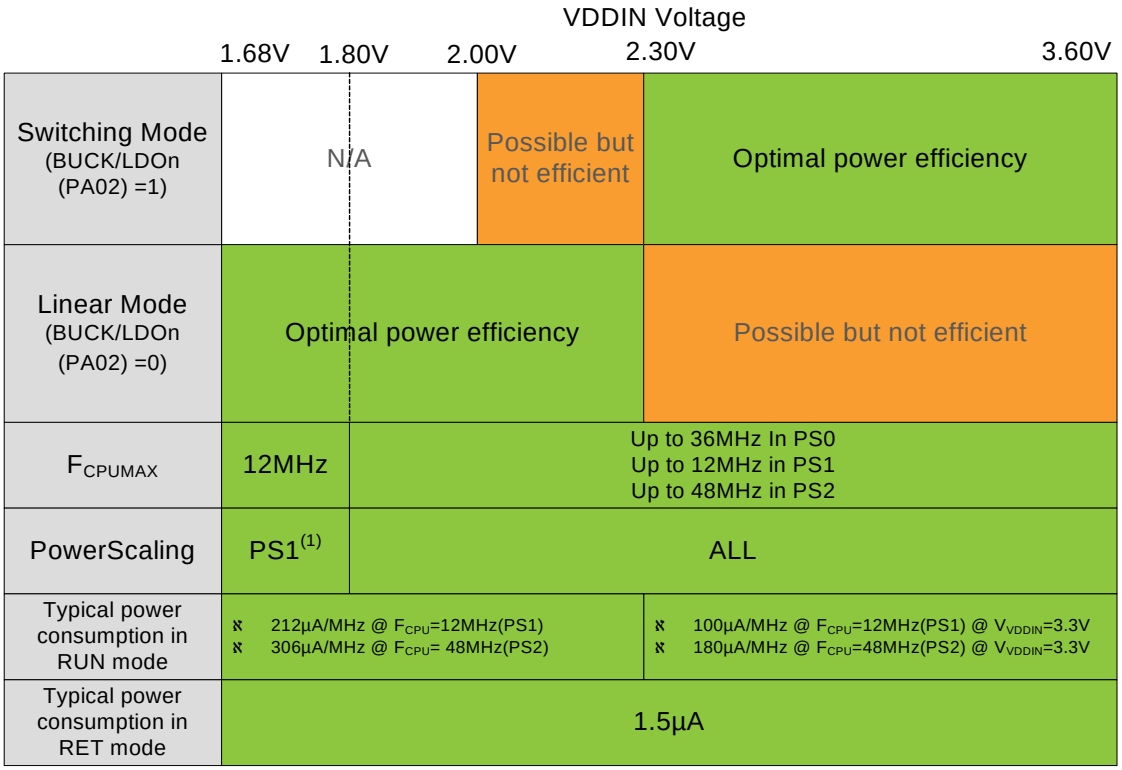
Memory	Start Address	Size	Size
		ATSAM4Lx4	ATSAM4Lx2
Embedded Flash	0x00000000	256Kbytes	128Kbytes
Embedded SRAM	0x20000000	32Kbytes	32Kbytes
Cache SRAM	0x21000000	4Kbytes	4Kbytes
Peripheral Bridge A	0x40000000	64Kbytes	64Kbytes
Peripheral Bridge B	0x400A0000	64Kbytes	64Kbytes
AESA	0x400B0000	256 bytes	256 bytes
Peripheral Bridge C	0x400E0000	64Kbytes	64Kbytes
Peripheral Bridge D	0x400F0000	64Kbytes	64Kbytes

Memory	Start Address	Size
		ATSAM4Lx8
Embedded Flash	0x00000000	512Kbytes
Embedded SRAM	0x20000000	64Kbytes
Cache SRAM	0x21000000	4Kbytes
Peripheral Bridge A	0x40000000	64Kbytes
Peripheral Bridge B	0x400A0000	64Kbytes

6.2.2 Typical Powering Schematics

The ATSAM4L8/L4/L2 supports the Single supply mode from 1.68V to 3.6V. Depending on the input voltage range and on the final application frequency, it is recommended to use the following table in order to choose the most efficient power strategy

Figure 6-3. Efficient power strategy:



Note 1. The SAM4L boots in PS0 on RCSYS(115kHz), then the application must switch to PS1 before running on higher frequency (<12MHz)

7.1.3 BACKUP Mode

The BACKUP mode allows achieving the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time.

The Core domain is powered-off. The internal SRAM and register contents of the Core domain are lost. The Backup domain is kept powered-on. The 32kHz clock (RC32K or OSC32K) is kept running if enabled to feed modules that require clocking.

In BACKUP mode, the configuration of the I/O lines is preserved. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677 to have more details.

7.1.3.1 Entering BACKUP Mode

The Backup mode is entered by using the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 1.

7.1.3.2 Exiting BACKUP Mode

Exit from BACKUP mode happens if a reset occurs or if an enabled wake up event occurs.

The reset sources are:

- BOD33 reset
- BOD18 reset
- WDT reset
- External reset in RESET_N pin

The wake up sources are:

- EIC lines (level transition only)
- BOD33 interrupt
- BOD18 interrupt
- AST alarm, periodic, overflow
- WDT interrupt

The RC32K or OSC32K should be used as clock source for modules if required. The PMCON.CK32S is used to select one of these two 32kHz clock sources.

Exiting the BACKUP mode is triggered by:

- a reset source: an internal reset sequence is performed according to the reset source. Once VDDCORE is stable and has the correct value according to RUN0 mode, the internal reset is released and program execution starts. The corresponding reset source is flagged in the Reset Cause register (RCAUSE) of the PM.
- a wake up source: the Backup domain is not reset. An internal reset is generated to the Core domain, and the system switches back to the previous RUN mode. Once VDDCORE is stable and has the correct value, the internal reset in the Core domain is released and program execution starts. The BKUP bit is set in the Reset Cause register (RCAUSE) of the PM. It allows the user to discriminate between the reset cause and a wake up cause from the BACKUP mode. The wake up cause can be found in the Backup Wake up Cause register (BPM.BKUPWCAUSE).

7.1.5 Power Save Mode Summary Table

The following table shows a summary of the main Power Save modes:

Table 7-2. Power Save mode Configuration Summary

Mode	Mode Entry	Wake up sources	Core domain	Backup domain
SLEEP	WFI SCR.SLEEPDEEP bit = 0 BPM.PMCON.BKUP bit = 0	Any interrupt	CPU clock OFF Other clocks OFF depending on the BPM.PMCON.SLEEP field see "SLEEP mode" on page 56	Clocks OFF depending on the BPM.PMCON.SLEEP field see "SLEEP mode" on page 56
WAIT	WFI SCR.SLEEPDEEP bit = 1 BPM.PMCON.RET bit = 0 BPM.PMCON.BKUP bit = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running
RETENTION	WFI SCR.SLEEPDEEP bit = 1 BPM.PMCON.RET bit = 1 BPM.PMCON.BKUP bit = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running
BACKUP	WFI + SCR.SLEEPDEEP bit = 1 + BPM.PMCON.BKUP bit = 1	EIC interrupt BOD33, BOD18 interrupt and reset AST alarm, periodic, overflow WDT interrupt and reset external reset on RESET_N pin	OFF (not powered)	All clocks are OFF except RC32K or OSC32K if running

7.2 Power Scaling

The Power Scaling technique consists of adjusting the internal regulator output voltage (voltage scaling) to reduce the power consumption. According to the requirements in terms of performance, operating modes, and current consumption, the user can select the Power Scaling configuration that fits the best with its application.

The Power Scaling configuration field (PMCON.PS) is provided in the Backup Power Manager (BPM) module.

In RUN mode, the user can adjust on the fly the Power Scaling configuration

The Figure 7.1 summarizes the different combination of the Power Scaling configuration which can be applied according to the Power Save Mode.

Power scaling from a current power configuration to a new power configuration is done by halting the CPU execution

Power scaling occurs after a WFI instruction. The system is halted until the new power configuration is stabilized. After handling the PM interrupt, the system resumes from WFI.

To scale the power, the following sequence is required:

- Check the BPM.SR.PSOK bit to make sure the current power configuration is stabilized.

8.7.14.4 CLAMP

This instruction selects the Bypass register as Data Register. The device output pins are driven from the boundary-scan chain.

Starting in Run-Test/Idle, the CLAMP instruction is accessed the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. In Update-IR: The data from the boundary-scan chain is applied to the output pins.
5. Return to Run-Test/Idle.
6. Select the DR Scan path.
7. In Capture-DR: A logic ‘0’ is loaded into the Bypass Register.
8. In Shift-DR: Data is scanned from TDI to TDO through the Bypass register.
9. Return to Run-Test/Idle.

Table 8-8. CLAMP Details

Instructions	Details
IR input value	**0101** (0x5)
IR output value	p00s
DR Size	1
DR input value	x
DR output value	x

8.9.11.5 Length Register

Name: LENGTH

Access Type: Read/Write

Offset: 0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
LENGTH							

23	22	21	20	19	18	17	16
LENGTH							

15	14	13	12	11	10	9	8
LENGTH							

7	6	5	4	3	2	1	0
LENGTH						-	-

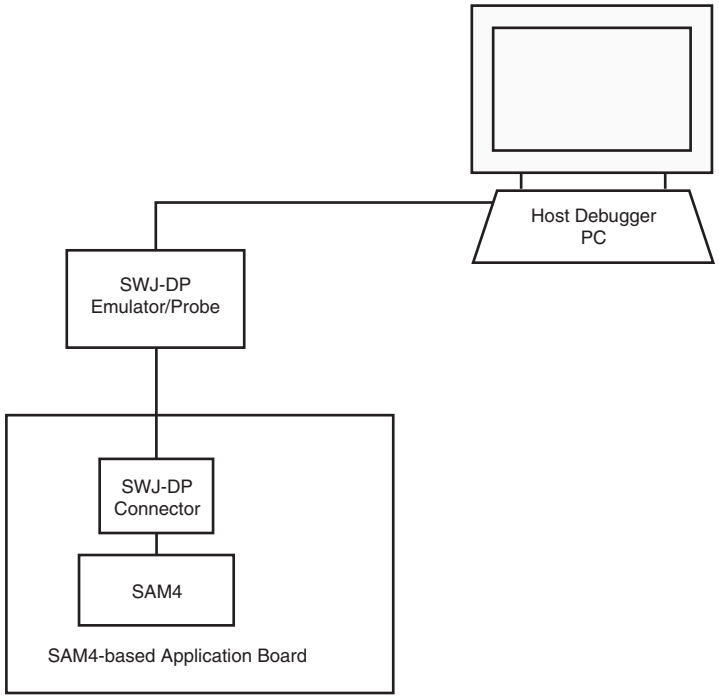
- **LENGTH: Length Value, Bits 1-0 are always zero**

8.11 Functional Description

8.11.1 Debug Environment

Figure 8-8 shows a complete debug environment example. The SWJ-DP interface is used for standard debugging functions, such as downloading code and single-stepping through the program and viewing core and peripheral registers.

Figure 8-8. Application Debug Environment Example



8.11.2 Test Environment

Figure 8-9 shows a test environment example (JTAG Boundary scan). Test vectors are sent and interpreted by the tester. In this example, the “board in test” is designed using a number of JTAG-compliant devices. These devices can be connected to form a single scan chain.

9. Electrical Characteristics

9.1 Absolute Maximum Ratings*

Table 9-1. Absolute Maximum Ratings

Operating temperature ..... -40°C to +85°C
Storage temperature ..... -60°C to +150°C
Voltage on input pins with respect to ground .....-0.3V to V_{VDD} (1)+0.3V
Total DC output current on all I/O pins VDDIO ..... 120 mA
Total DC output current on all I/O pins VDDIN ..... 100 mA
Total DC output current on all I/O pins VDDANA..... 50 mA
Maximum operating voltage VDDIO, VDDIN 3.6V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details

9.2 Operating Conditions

All the electrical characteristics are applicable to the following conditions unless otherwise specified :

- operating voltage range 1,68V to 3,6V for VDDIN, VDDIO & VDDANA
- Power Scaling 0 and 2 modes
- operating temperature range: TA = -40°C to 85°C and for a junction temperature up to TJ = 100°C.

Typical values are base on TA = 25°c and VDDIN,VDDIO,VDDANA = 3,3V unless otherwise specified

9.3 Supply Characteristics

Table 9-2. Supply Characteristics

Symbol	Conditions	Voltage		
		Min	Max	Unit
V_{VDDIO}, V_{VDDIN}, V_{VDDANA}	PS1 (FCPU<=12MHz) Linear mode	1.68	3.6	V
	PS0 & PS2 (FCPU>12MHz) Linear mode	1.8		
	Switching mode	2.0 (1)		

1. Below 2.3V, linear mode is more power efficient than switching mode.

Refer to Section 6. ”Power and Startup Considerations” on page 46 for details about Power Supply

Table 9-5. Maximum Clock Frequencies in Power Scaling Mode 1 and RUN Mode

Symbol	Parameter	Description	Max	Units
f_{CPU}	CPU clock frequency		12	MHz
f_{PBA}	PBA clock frequency		12	
f_{PBB}	PBB clock frequency		12	
f_{PBC}	PBC clock frequency		12	
f_{PBD}	PBD clock frequency		12	
f_{GCLK0}	GCLK0 clock frequency	DFLLIF main reference, GCLK0 pin	16.6	
f_{GCLK1}	GCLK1 clock frequency	DFLLIF dithering and SSGreference, GCLK1 pin	16.6	
f_{GCLK2}	GCLK2 clock frequency	AST, GCLK2 pin	6.6	
f_{GCLK3}	GCLK3 clock frequency	CATB, GCLK3 pin	17.3	
f_{GCLK4}	GCLK4 clock frequency	FLO and AESA	16.6	
f_{GCLK5}	GCLK5 clock frequency	GLOC, TC0 and RC32KIFB_REF	26.6	
f_{GCLK6}	GCLK6 clock frequency	ABDACB and IISC	16.6	
f_{GCLK7}	GCLK7 clock frequency	USBC	16.6	
f_{GCLK8}	GCLK8 clock frequency	TC1 and PEVC[0]	16.6	
f_{GCLK9}	GCLK9 clock frequency	PLL0 and PEVC[1]	16.6	
f_{GCLK10}	GCLK10 clock frequency	ADCIFE	16.6	
f_{GCLK11}	GCLK11 clock frequency	Master generic clock. Can be used as source for other generic clocks	51.2	
f_{OSC0}	OSC0 output frequency	Oscillator 0 in crystal mode	16	
		Oscillator 0 in digital clock mode	16	
f_{PLL}	PLL output frequency	Phase Locked Loop	N/A	
f_{DFLL}	DFLL output frequency	Digital Frequency Locked Loop	N/A	
f_{RC80M}	RC80M output frequency	Internal 80MHz RC Oscillator	N/A	

3. These values are based on characterization. These values are not covered by test limits in production

9.6.2 High-drive I/O Pin : PA02, PC04, PC05, PC06

Table 9-14. High-drive I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.8	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			22	MHz
		OSRR0=1				17	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			35	MHz
		OSRR0=1				26	MHz
I_{LEAK}	Input leakage current(3)	Pull-up resistors disabled			0.01	2	µA
C_{IN}	Input capacitance(2)				10		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.7.7 1MHz RC Oscillator (RC1M) Characteristics

Table 9-30. RC1M Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)		0.91	1	1.12	MHz
I_{RC1M}	Current consumption (2)			35		µA
Duty	Duty cycle(1)		48.6	49.9	54.4	%

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.7.8 4/8/12MHz RC Oscillator (RCFAST) Characteristics

Table 9-31. RCFAST Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)	Calibrated, FRANGE=0	4	4.3	4.6	MHz
		Calibrated, FRANGE=1	7.8	8.2	8.5	
		Calibrated, FRANGE=2	11.3	12	12.3	
I_{RCFAST}	Current consumption (2)	Calibrated, FRANGE=0		90	110	µA
		Calibrated, FRANGE=1		130	150	
		Calibrated, FRANGE=2		180	205	
Duty	Duty cycle(1)	Calibrated, FRANGE=0	48.8	49.6	50.1	%
		Calibrated, FRANGE=1	47.8	49.2	50.1	
		Calibrated, FRANGE=2	46.7	48.8	50.0	
$t_{STARTUP}$	Startup time(1)	Calibrated, FRANGE=2	0.1	0.31	0.71	µs

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-39. VREG Electrical Characteristics in Switching mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	DC output current(1)	$V_{VDDCORE}$ > 1.65V			55	mA
	Output DC load regulation(1) Transient load regulation	I_{OUT} = 0 to 50mA, V_{VDDIN} = 3V	-136	-101	-82	mV
	Output DC regulation(1)	I_{OUT} = 50 mA, V_{VDDIN} = 2V to 3.6V	-20	38	99	mV
I_Q	Quescient current(1)	V_{VDDIN} = 2V, I_{OUT} = 0 mA	97	186	546	µA
		V_{VDDIN} > 2.2V, I_{OUT} = 0 mA	97	111	147	
P_{EFF}	Power efficiency(1)	I_{OUT} = 5mA, 50mA Reference power not included	82.7	88.3	95	%

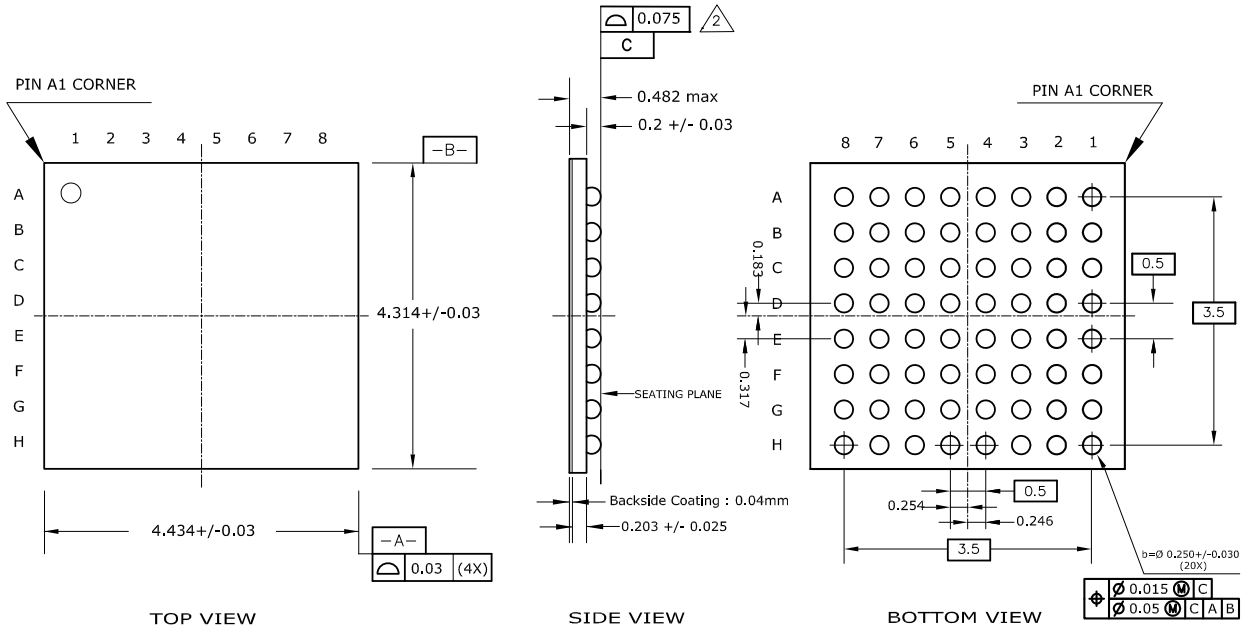
1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-40. Decoupling Requirements in Switching Mode

Symbol	Parameter	Technology	Typ	Units
C_{IN1}	Input regulator capacitor 1		33	nF
C_{IN2}	Input regulator capacitor 2		100	
C_{IN3}	Input regulator capacitor 3		10	µF
C_{OUT1}	Output regulator capacitor 1	X7R MLCC	100	nF
C_{OUT2}	Output regulator capacitor 2	X7R MLCC (ex : GRM31CR71A475)	4.7	µF
L_{EXT}	External inductance	(ex: Murata LQH3NPN220MJ0)	22	µH
R_{DCLEXT}	Serial resistance of L_{EXT}		0.7	Ω
$ISAT_{LEXT}$	Saturation current of L_{EXT}		300	mA

Note: 1. Refer to Section 6. on page 46.

Figure 10-3. WLCSP64 SAM4LC4/2 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.746	1.683
A2	GNDANA	1.246	1.683
A3	ADVREFP	0.746	1.683
A4	VDDANA	0.246	1.683
A5	PA09	-0.254	1.683
A6	CAPL	-0.754	1.683
A7	CAPH	-1.254	1.683
A8	PA12	-1.754	1.683
B1	PB03	1.746	1.183
B2	XIN32	1.246	1.183
B3	XOUT32	0.746	1.183
B4	PA08	0.246	1.183
B5	PB06	-0.254	1.183
B6	PA10	-0.754	1.183
B7	PA11	-1.254	1.183
B8	VLCD	-1.754	1.183
C1	VDDIN	1.746	0.683
C2	PB01	1.246	0.683
C3	PA05	0.746	0.683
C4	PA06	0.246	0.683
C5	PA07	-0.254	0.683
C6	PB07	-0.754	0.683

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	-1.254	0.683
C8	BIAS1	-1.754	0.683
D1	VDDOUT	1.746	0.183
D2	PB00	1.246	0.183
D3	PA04	0.746	0.183
D4	PB05	0.246	0.183
D5	PB12	-0.254	0.183
D6	PB08	-0.754	0.183
D7	PA14	-1.254	0.183
D8	BIAS2	-1.754	0.183
E1	GNDIN	1.746	-0.317
E2	PA03	1.246	-0.317
E3	PB02	0.746	-0.317
E4	RESET_N	0.246	-0.317
E5	PB13	-0.254	-0.317
E6	PB09	-0.754	-0.317
E7	PA15	-1.254	-0.317
E8	GNDIO0	-1.754	-0.317
F1	VDDCORE	1.746	-0.817
F2	TCK	1.246	-0.817
F3	PA02	0.746	-0.817
F4	PB14	0.246	-0.817

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.254	-0.817
F6	PB10	-0.754	-0.817
F7	PA16	-1.254	-0.817
F8	VLCDIN	-1.754	-0.817
G1	GNDIO1	1.746	-1.317
G2	PA26	1.246	-1.317
G3	PA24	0.746	-1.317
G4	PA00	0.246	-1.317
G5	PA01	-0.254	-1.317
G6	PA19	-0.754	-1.317
G7	PA18	-1.254	-1.317
G8	PA17	-1.754	-1.317
H1	VDDIO1	1.746	-1.817
H2	PA25	1.246	-1.817
H3	PA23	0.746	-1.817
H4	PB15	0.246	-1.817
H5	PA21	-0.254	-1.817
H6	VDDIO0	-0.754	-1.817
H7	PA20	-1.254	-1.817
H8	PB11	-1.754	-1.817

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-8. Device and Package Maximum Weight

14.8	mg

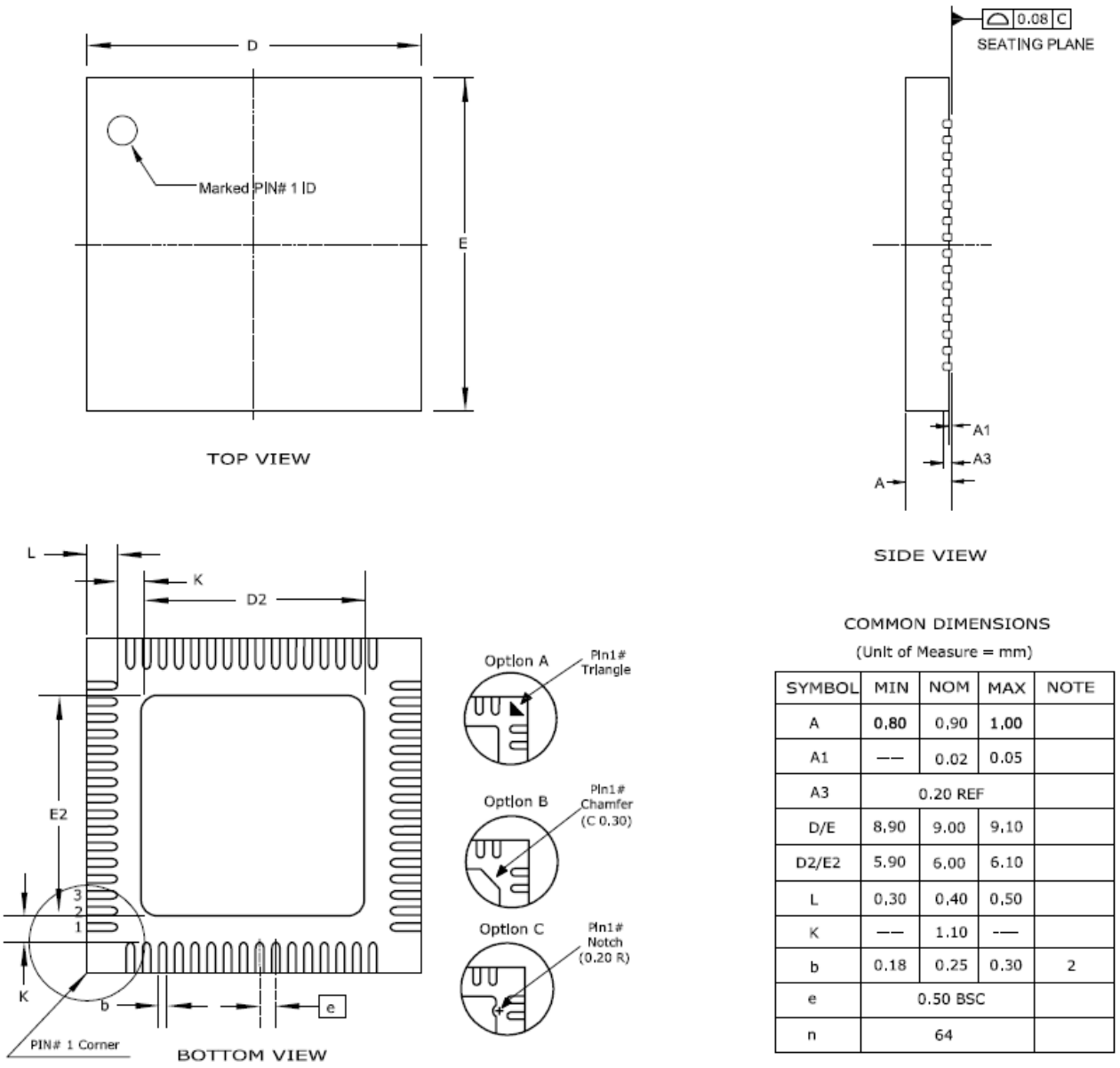
Table 10-9. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-10. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

Figure 10-8. QFN-64 Package Drawing



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	—	0.02	0.05	
A3		0.20 REF		
D/E	8.90	9.00	9.10	
D2/E2	5.90	6.00	6.10	
L	0.30	0.40	0.50	
K	—	1.10	—	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		64		

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 10-23. Device and Package Maximum Weight

200	mg

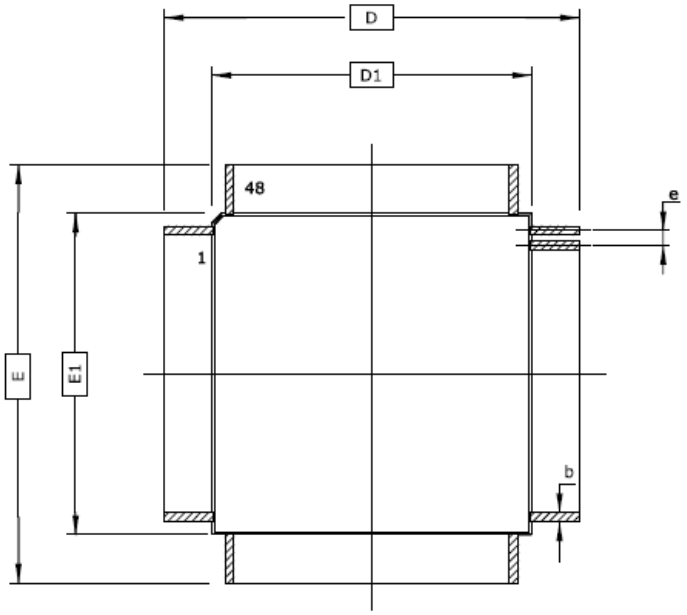
Table 10-24. Package Characteristics

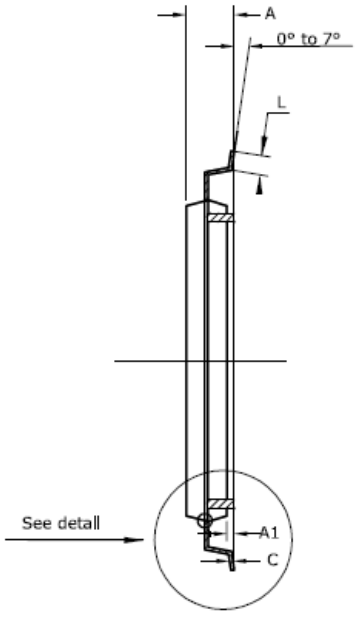
Moisture Sensitivity Level	MSL3

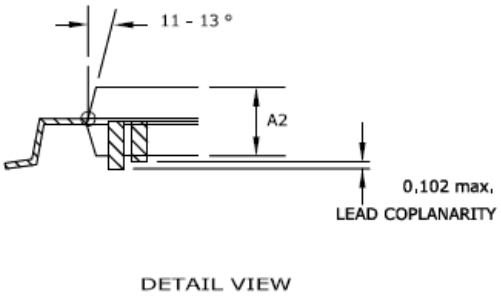
Table 10-25. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

Figure 10-9. TQFP-48 (ATSAM4LC4/2 and ATSAM4LS4/2 Only) Package Drawing







COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1,20	
A1	0,05	---	0,15	
A2	0,95	---	1,05	
C	0,09	---	0,20	
D/E	9.00 BSC			
D1/E1	7.00 BSC			
L	0,45	---	0,75	
b	0,17	---	0,27	
e	0,50 BSC			

Table 10-26. Device and Package Maximum Weight

140	mg

Table 10-27. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-28. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

13. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

13.1 Rev. A – 09/12

1. Initial revision.

13.2 Rev. B – 10/12

1. Fixed ordering code
2. Changed BOD18CTRL and BOD33CTRL ACTION field from “Reserved” to ‘No action”

13.3 Rev. C – 02/13

1. Fixed ball pitch for VFBGA100 package
2. Added VFBGA100 and WLCSP64 pinouts
3. Added Power Scaling Mode 2 for high frequency support
4. Minor update on several modules chapters
5. Major update on Electrical characteristics
6. Updated errata
7. Fixed GPIO multiplexing pin numbers

13.4 Rev. D – 03/13

1. Removed WLCSP package information
2. Added errata text for detecting whether a part supports PS2 mode or not
3. Removed temperature sensor feature (not supported by production flow)
4. Fixed MUX selection on Positive ADC input channel table
5. Added information about TWI instances capabilities
6. Added some details on errata Corrupted data in flash may happen after flash page write operations.171

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