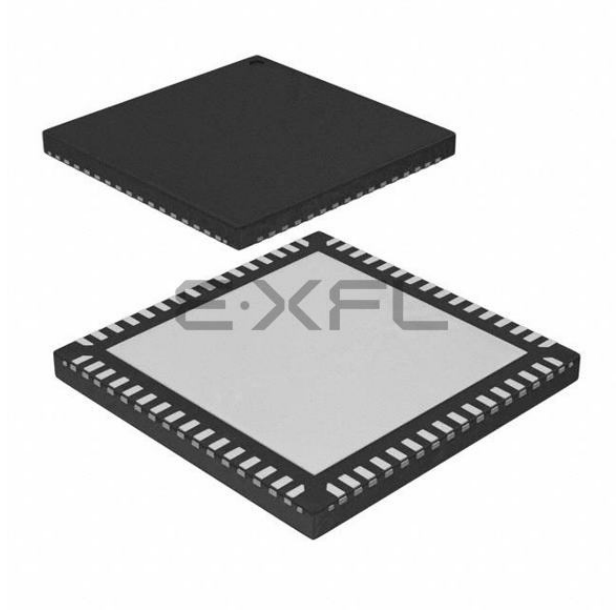

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 7x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls4ba-mu

Figure 3-2. ATSAM4LC VFBGA100 Pinout

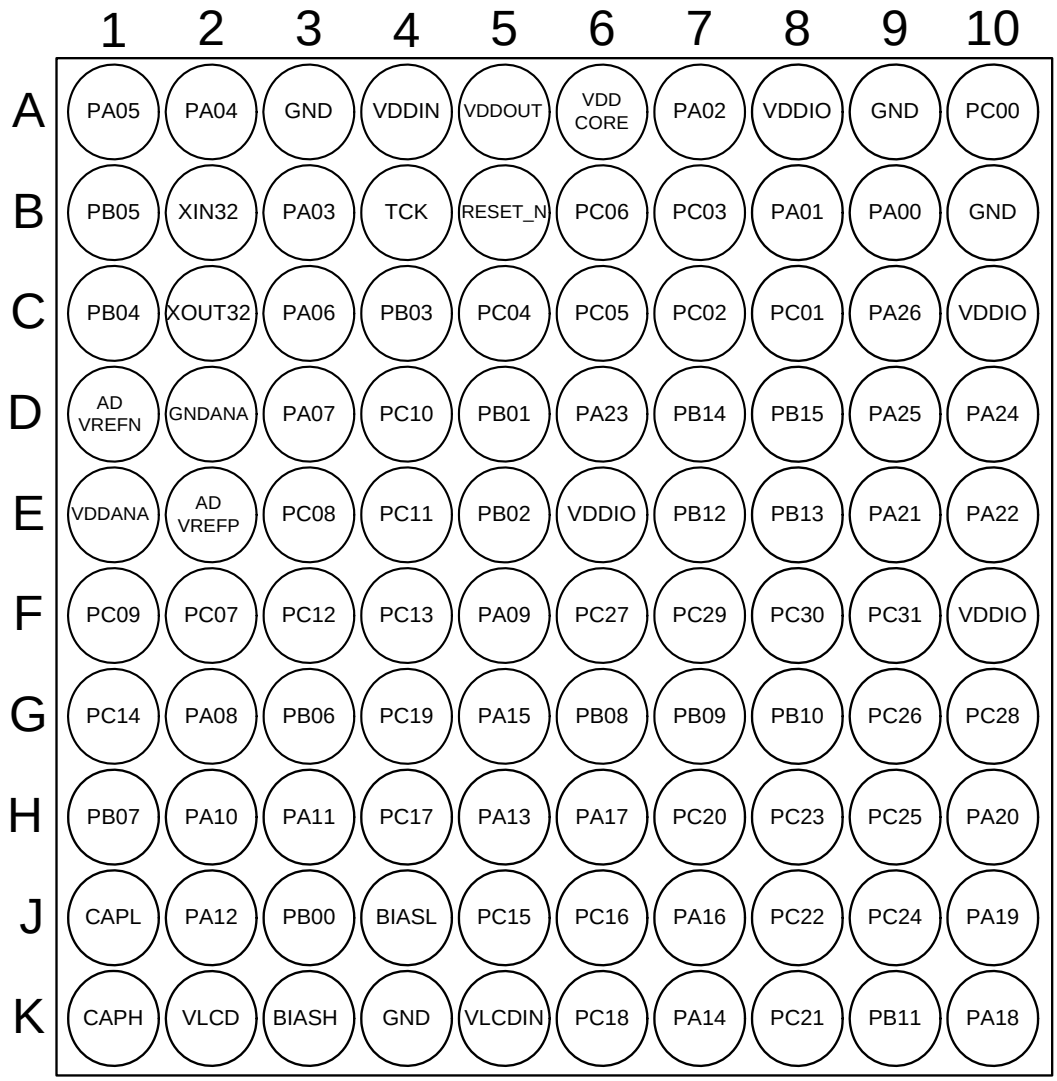


Table 4-2. Interrupt Request Signal Map (Sheet 3 of 3)

Line	Module	Signal
48	External Interrupt Controller	EIC 4
49	External Interrupt Controller	EIC 5
50	External Interrupt Controller	EIC 6
51	External Interrupt Controller	EIC 7
52	External Interrupt Controller	EIC 8
53	Inter-IC Sound (I2S) Controller	IISC
54	Serial Peripheral Interface	SPI
55	Timer/Counter	TC00
56	Timer/Counter	TC01
57	Timer/Counter	TC02
58	Timer/Counter	TC10
59	Timer/Counter	TC11
60	Timer/Counter	TC12
61	Two-wire Master Interface	TWIM0
62	Two-wire Slave Interface	TWIS0
63	Two-wire Master Interface	TWIM1
64	Two-wire Slave Interface	TWIS1
65	Universal Synchronous Asynchronous Receiver Transmitter	USART0
66	Universal Synchronous Asynchronous Receiver Transmitter	USART1
67	Universal Synchronous Asynchronous Receiver Transmitter	USART2
68	Universal Synchronous Asynchronous Receiver Transmitter	USART3
69	ADC controller interface	ADCIFE
70	DAC Controller	DACC
71	Analog Comparator Interface	ACIFC
72	Audio Bitstream DAC	ABDACB
73	True Random Number Generator	TRNG
74	Parallel Capture	PARC
75	Capacitive Touch Module B	CATB
77	Two-wire Master Interface	TWIM2
78	Two-wire Master Interface	TWIM3
79	LCD Controller A	LCDCA

At power-up or after a reset, the ATSAM4L8/L4/L2 is in the RUN0 mode. Only the necessary clocks are enabled allowing software execution. The Power Manager (PM) can be used to adjust the clock frequencies and to enable and disable the peripheral clocks.

When the CPU is entering a Power Save Mode, the CPU stops executing code. The user can choose between four Power Save Modes to optimize power consumption:

- SLEEP mode: the Cortex-M4 core is stopped, optionally some clocks are stopped, peripherals are kept running if enabled by the user.
- WAIT mode: all clock sources are stopped, the core and all the peripherals are stopped except the modules running with the 32kHz clock if enabled. This is the lowest power configuration where SleepWalking is supported.
- RETENTION mode: similar to the WAIT mode in terms of clock activity. This is the lowest power configuration where the logic is retained.
- BACKUP mode: the Core domain is powered off, the Backup domain is kept powered.

A wake up source exits the system to the RUN mode from which the Power Save Mode was entered.

A reset source always exits the system from the Power Save Mode to the RUN0 mode.

The configuration of the I/O lines are maintained in all Power Save Modes. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677.

7.1.1 SLEEP mode

The SLEEP mode allows power optimization with the fastest wake up time.

The CPU is stopped. To further reduce power consumption, the user can switch off modules-clocks and synchronous clock sources through the BPM.PMCON.SLEEP field (See Table 7-1). The required modules will be halted regardless of the bit settings of the mask registers in the Power Manager (PM.AHBMASK, PM.APBxMASK).

Table 7-1. SLEEP mode Configuration

BPM.PSAVE.SLEEP	CPU clock	AHB clocks	APB clocks GCLK	Clock sources: OSC, RCFAST, RC80M, PLL, DFLL	RCSYS	OSC32K RC32K(2)	Wake up Sources
0	Stop	Run	Run	Run	Run	Run	Any interrupt
1	Stop	Stop	Run	Run	Run	Run	Any interrupt(1)
2	Stop	Stop	Stop	Run	Run	Run	Any interrupt(1)
3	Stop	Stop	Stop	Stop	Run	Run	Any interrupt(1)

Notes: 1. from modules with clock running.
2. OSC32K and RC32K will only remain operational if pre-enabled.

7.1.1.1 Entering SLEEP mode

The SLEEP mode is entered by executing the WFI instruction.

Additionally, if the SLEEPONEXIT bit in the Cortex-M4 System Control Register (SCR) is set, the SLEEP mode will also be entered when the Cortex-M4 exits the lowest priority ISR. This

7.1.3 BACKUP Mode

The BACKUP mode allows achieving the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time.

The Core domain is powered-off. The internal SRAM and register contents of the Core domain are lost. The Backup domain is kept powered-on. The 32kHz clock (RC32K or OSC32K) is kept running if enabled to feed modules that require clocking.

In BACKUP mode, the configuration of the I/O lines is preserved. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677 to have more details.

7.1.3.1 Entering BACKUP Mode

The Backup mode is entered by using the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 1.

7.1.3.2 Exiting BACKUP Mode

Exit from BACKUP mode happens if a reset occurs or if an enabled wake up event occurs.

The reset sources are:

- BOD33 reset
- BOD18 reset
- WDT reset
- External reset in RESET_N pin

The wake up sources are:

- EIC lines (level transition only)
- BOD33 interrupt
- BOD18 interrupt
- AST alarm, periodic, overflow
- WDT interrupt

The RC32K or OSC32K should be used as clock source for modules if required. The PMCON.CK32S is used to select one of these two 32kHz clock sources.

Exiting the BACKUP mode is triggered by:

- a reset source: an internal reset sequence is performed according to the reset source. Once VDDCORE is stable and has the correct value according to RUN0 mode, the internal reset is released and program execution starts. The corresponding reset source is flagged in the Reset Cause register (RCAUSE) of the PM.
- a wake up source: the Backup domain is not reset. An internal reset is generated to the Core domain, and the system switches back to the previous RUN mode. Once VDDCORE is stable and has the correct value, the internal reset in the Core domain is released and program execution starts. The BKUP bit is set in the Reset Cause register (RCAUSE) of the PM. It allows the user to discriminate between the reset cause and a wake up cause from the BACKUP mode. The wake up cause can be found in the Backup Wake up Cause register (BPM.BKUPWCAUSE).

- Set the clock frequency to be supported in both power configurations.
- Set the high speed read mode of the FLASH to be supported in both power scaling configurations
  - Only relevant when entering or exiting BPM.PMCON.PS=2
- Configure the BPM.PMCON.PS field to the new power configuration.
- Set the BPM.PMCON.PSCREQ bit to one.
- Disable all the interrupts except the PM WCAUSE interrupt and enable only the PSOK asynchronous event in the AWEN register of PM.
- Execute the WFI instruction.
- WAIT for PM interrupt.

The new power configuration is reached when the system is waken up by the PM interrupt thanks to the PSOK event.

By default, all features are available in all Power Scaling modes. However some specific features are not available in PS1 (BPM.PMCON.PS=1) mode :

- USB
- DFLL
- PLL
- Programming/Erasing in Flash

  - Fix the ATB ID to 1
- Write 0x1 into the Trace Enable Register:
  - Enable the Stimulus port 0
- Write 0x1 into the Trace Privilege Register:
  - Stimulus port 0 only accessed in privileged mode (Clearing a bit in this register will result in the corresponding stimulus port being accessible in user mode.)
- Write into the Stimulus port 0 register: TPIU (Trace Port Interface Unit)

  The TPIU acts as a bridge between the on-chip trace data and the Instruction Trace Macrocell (ITM).

  The TPIU formats and transmits trace data off-chip at frequencies asynchronous to the core.

Asynchronous Mode:

The TPIU is configured in asynchronous mode, trace data are output using the single TRACESWO pin. The TRACESWO signal is multiplexed with the TDO signal of the JTAG Debug Port. As a consequence, asynchronous trace mode is only available when the Serial Wire Debug mode is selected since TDO signal is used in JTAG debug mode.

Two encoding formats are available for the single pin output:

- Manchester encoded stream. This is the reset value.
- NRZ_based UART byte structure

5.4.3. How to Configure the TPIU

This example only concerns the asynchronous trace mode.

- Set the TRCENA bit to 1 into the Debug Exception and Monitor Register (0xE000EDFC) to enable the use of trace and debug blocks.
- Write 0x2 into the Selected Pin Protocol Register
  - Select the Serial Wire Output – NRZ
- Write 0x100 into the Formatter and Flush Control Register
- Set the suitable clock prescaler value into the Async Clock Prescaler Register to scale the baud rate of the asynchronous output (this can be done automatically by the debugging tool).

8.7.10 SW-DP and JTAG-DP Selection Mechanism

After reset, the SWJ-DP is in JTAG mode but it can be switched to the Serial Wire mode. Debug port selection mechanism is done by sending specific **SWDIOTMS** sequence. The JTAG-DP is selected by default after reset.

- Switch from JTAG-DP to SW-DP. The sequence is:
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
  - Send the 16-bit sequence on **SWDIOTMS** = 0111100111100111 (0x79E7 MSB first)
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
- Switch from SWD to JTAG. The sequence is:
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
  - Send the 16-bit sequence on **SWDIOTMS** = 0011110011100111 (0x3CE7 MSB first)

Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1

Note that the BSCAN-TAP is not available when the debug port is switched to Serial Mode. Boundary scan instructions are not available.

8.7.11 JTAG-DP and BSCAN-TAP Selection Mechanism

After the DP has been enabled, the BSCAN-TAP and the JTAG-DP run simultaneously has long as the SWJ-DP remains in JTAG mode. Each TAP captures simultaneously the JTAG instructions that are shifted. If an instruction is recognized by the BSCAN-TAP, then the BSCAN-TAP TDO is selected instead of the SWJ-DP TDO. TDO selection changes dynamically depending on the current instruction held in the BSCAN-TAP instruction register.

8.9.11.1 Control Register

Name: CR

Access Type: Write-Only

Offset: 0x00

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	CE	FSPR	CRC	DIS	EN

Writing a zero to a bit in this register has no effect.

- **CE: Chip Erase**
  Writing a one to this bit triggers the FLASH Erase All (EA) operation which clears all volatile memories, the whole flash array, the general purpose fuses and the protected state. The Status register DONE field indicates the completion of the operation.
  Reading this bit always returns 0
- **FSPR: Flash User Page Read**
  Writing a one to this bit triggers a read operation in the User page. The word pointed by the ADDR register in the page is read and written to the DATA register. ADDR is post incremented allowing a burst of reads without modifying ADDR. SR.DONE must be read high prior to reading the DATA register.
  Reading this bit always returns 0
- **CRC: Cyclic Redundancy Code**
  Writing a one triggers a CRC calculation over a memory area defined by the ADDR and LENGTH registers. Reading this bit always returns 0
  Note: This feature is restricted while in protected state
- **DIS: Disable**
  Writing a one to this bit disables the module. Disabling the module resets the whole module immediately.
- **EN: Enable**
  Writing a one to this bit enables the module.

8.9.11.5 Length Register

Name: LENGTH

Access Type: Read/Write

Offset: 0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
LENGTH							

23	22	21	20	19	18	17	16
LENGTH							

15	14	13	12	11	10	9	8
LENGTH							

7	6	5	4	3	2	1	0
LENGTH						-	-

- **LENGTH: Length Value, Bits 1-0 are always zero**

8.9.11.8 Chip Identification Register

Name: CIDR

Access Type: Read-Only

Offset: 0xF0

Reset Value: -

31	30	29	28	27	26	25	24
EXT	NVPTYP			ARCH			

23	22	21	20	19	18	17	16
ARCH				SRAMSIZ			

15	14	13	12	11	10	9	8
NVPSIZ2				NVPSIZ			

7	6	5	4	3	2	1	0
EPROC				VERSION			

Note: Refer to section CHIPID for more information on this register.

8.9.11.9 *Chip Identification Extension Register*

Name: EXID

Access Type: Read-Only

Offset: 0xF4

Reset Value: -

31	30	29	28	27	26	25	24
EXID							

23	22	21	20	19	18	17	16
EXID							

15	14	13	12	11	10	9	8
EXID							

7	6	5	4	3	2	1	0
EXID							

Note: Refer to section CHIPID for more information on this register.

9. Electrical Characteristics

9.1 Absolute Maximum Ratings*

Table 9-1. Absolute Maximum Ratings

Operating temperature ..... -40°C to +85°C
Storage temperature ..... -60°C to +150°C
Voltage on input pins with respect to ground .....-0.3V to V_{VDD} (1)+0.3V
Total DC output current on all I/O pins VDDIO ..... 120 mA
Total DC output current on all I/O pins VDDIN ..... 100 mA
Total DC output current on all I/O pins VDDANA..... 50 mA
Maximum operating voltage VDDIO, VDDIN 3.6V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details

9.2 Operating Conditions

All the electrical characteristics are applicable to the following conditions unless otherwise specified :

- operating voltage range 1,68V to 3,6V for VDDIN, VDDIO & VDDANA
- Power Scaling 0 and 2 modes
- operating temperature range: TA = -40°C to 85°C and for a junction temperature up to TJ = 100°C.

Typical values are base on TA = 25°c and VDDIN,VDDIO,VDDANA = 3,3V unless otherwise specified

9.3 Supply Characteristics

Table 9-2. Supply Characteristics

Symbol	Conditions	Voltage		
		Min	Max	Unit
V_{VDDIO}, V_{VDDIN}, V_{VDDANA}	PS1 (FCPU<=12MHz) Linear mode	1.68	3.6	V
	PS0 & PS2 (FCPU>12MHz) Linear mode	1.8		
	Switching mode	2.0 (1)		

1. Below 2.3V, linear mode is more power efficient than switching mode.

Refer to Section 6. ”Power and Startup Considerations” on page 46 for details about Power Supply

9.4 Maximum Clock Frequencies

Table 9-4. Maximum Clock Frequencies in Power Scaling Mode 0/2 and RUN Mode

Symbol	Parameter	Description	Max	Units
f_{CPU}	CPU clock frequency		48	MHz
f_{PBA}	PBA clock frequency		48	
f_{PBB}	PBB clock frequency		48	
f_{PBC}	PBC clock frequency		48	
f_{PBD}	PBD clock frequency		48	
f_{GCLK0}	GCLK0 clock frequency	DFLLIF main reference, GCLK0 pin	50	
f_{GCLK1}	GCLK1 clock frequency	DFLLIF dithering and SSG reference, GCLK1 pin	50	
f_{GCLK2}	GCLK2 clock frequency	AST, GCLK2 pin	20	
f_{GCLK3}	GCLK3 clock frequency	CATB, GCLK3 pin	50	
f_{GCLK4}	GCLK4 clock frequency	FLO and AESA	50	
f_{GCLK5}	GCLK5 clock frequency	GLOC, TC0 and RC32KIFB_REF	80	
f_{GCLK6}	GCLK6 clock frequency	ABDACB and IISC	50	
f_{GCLK7}	GCLK7 clock frequency	USBC	50	
f_{GCLK8}	GCLK8 clock frequency	TC1 and PEVC[0]	50	
f_{GCLK9}	GCLK9 clock frequency	PLL0 and PEVC[1]	50	
f_{GCLK10}	GCLK10 clock frequency	ADCIFE	50	
f_{GCLK11}	GCLK11 clock frequency	Master generic clock. Can be used as source for other generic clocks	150	
f_{OSC0}	OSC0 output frequency	Oscillator 0 in crystal mode	30	
		Oscillator 0 in digital clock mode	50	
f_{PLL}	PLL output frequency	Phase Locked Loop	240	
f_{DFLL}	DFLL output frequency	Digital Frequency Locked Loop	220	
f_{RC80M}	RC80M output frequency	Internal 80MHz RC Oscillator	80	

- Operating conditions, internal core supply (Figure 9-2)
  - V_{VDDIN} = 3.3V
  - $V_{VDDCORE}$ = 1.2 V, supplied by the internal regulator in switching mode
- T_A = 25°C
- Oscillators
  - OSC0 (crystal oscillator) stopped
  - OSC32K (32KHz crystal oscillator) running with external 32KHz crystal
  - RCFAST running @ 12MHz
- Clocks
  - RCFAST used as main clock source
  - CPU, AHB, and PB clocks undivided
- I/Os are inactive with internal pull-up
- Flash enabled in normal mode
- CPU in SLEEP0 mode
- BOD18 and BOD33 disabled

Consumption active is the added current consumption when the module clock is turned on

9.6.5 High Drive TWI Pin : PB00, PB01

Table 9-19. High Drive TWI Pin Characteristics in TWI configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)	PB00, PB01			40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.3 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.7 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	DRIVEL=0				0.5	mA
		DRIVEL=1				1.0	
		DRIVEL=2				1.6	
		DRIVEL=3				3.1	
		DRIVEL=4				6.2	
		DRIVEL=5				9.3	
		DRIVEL=6				15.5	
		DRIVEL=7				21.8	
I_{CS}	Current Source(2)	DRIVEH=0			0.5		mA
		DRIVEH=1			1		
		DRIVEH=2			1.5		
		DRIVEH=3			3		
f_{MAX}	Max frequency(2)	HsMode with Current source; DRIVEx=3, SLEW=0 Cbus = 400pF, V_{VDD} = 1.68V		3.5	6.4		MHz
t_{RISE}	Rise time(2)	HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			28	38	ns
t_{FALL}	Fall time(2)	Standard Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	ns
		HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Table 9-46. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDDANA	Supply voltage [1]		1.6		3.6	V
	Reference range [2]	Differential mode	1.0		VDDANA -0.6	V
		Unipolar and Window modes	1.0		1.0	
		Using divide by two function (differential)	2.0		VDDANA	
	Absolute min, max input voltage[2]		-0,1		VDDANA +0.1	V
	Start up time[2]	ADC with reference already enabled		12	24	Cycles
		No gain compensation Reference buffer			5	µs
		Gain compensation Reference buffer			60	Cycles
R_{SAMPLE}	Input channel source resistance[2]				0.5	kΩ
C_{SAMPLE}	Sampling capacitance[2]		2.9	3.6	4.3	pF
	Reference input source resistance[2]	Gain compensation			2	kΩ
		No gain compensation			1	MΩ
	ADC reference settling time[2]	After changing reference/mode [3]		5	60	Cycles

1. These values are based on characterization. These values are not covered by test limits in production
2. These values are based on simulation. These values are not covered by test limits in production
3. Requires refresh/flush otherwise conversion time (latency) + 1

Table 9-47. Differential mode, gain=1

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Accuracy without compensation [1]			7		ENOB
	Accuracy after compensation[1]	(INL, gain and offset)			11	ENOB
INL	Integral Non Linearity [2]	After calibration, Gain compensation		1.2	1.7	LSBs
DNL	Differential Non Linearity[2]	After calibration		0.7	1.0	LSBs
	Gain error [2]	External reference	-5.0	-1.0	5.0	mV
		VDDANA/1.6	-40		40	
		VDDANA/2.0	-40		40	
		Bandgap After calibration	-30		30	
	Gain error drift vs voltage[1]	External reference	-2		2	mV/V
	Gain error drift vs temperature[1]	After calibration + bandgap drift If using onchip bandgap			0.08	mV/°K
	Offset error [2]	External reference	-5.0		5.0	mV
		VDDANA/1.6	-10		10	
		VDDANA/2.0	-10		10	
		Bandgap After calibration	-10		10	
	Offset error drift vs voltage[1]		-4		4	mV/V

Figure 9-16. SPI Slave Mode, NPCS Timing

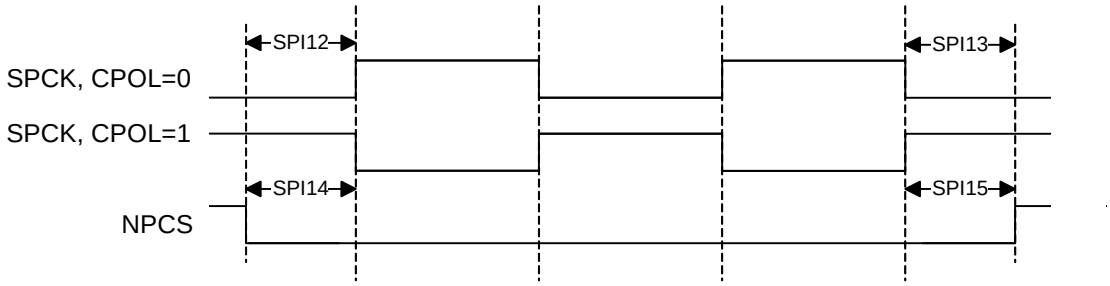


Table 9-63. SPI Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
SPI6	SPCK falling to MISO delay	V_{VDDIO} from 2.85V to 3.6V, maximum external capacitor = 40pF	19	47	ns
SPI7	MOSI setup time before SPCK rises		0		
SPI8	MOSI hold time after SPCK rises		5.4		
SPI9	SPCK rising to MISO delay		19	46	
SPI10	MOSI setup time before SPCK falls		0		
SPI11	MOSI hold time after SPCK falls		5.3		
SPI12	NPCS setup time before SPCK rises		4		
SPI13	NPCS hold time after SPCK falls		2.5		
SPI14	NPCS setup time before SPCK falls		6		
SPI15	NPCS hold time after SPCK rises		1.1		

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{CLKSPI}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, SPI7 + SPI8 or SPI10 + SPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

2. A device must internally provide a hold time of at least 300 ns for TWD with reference to the falling edge of TWCK.

Notations:

C_b = total capacitance of one bus line in pF

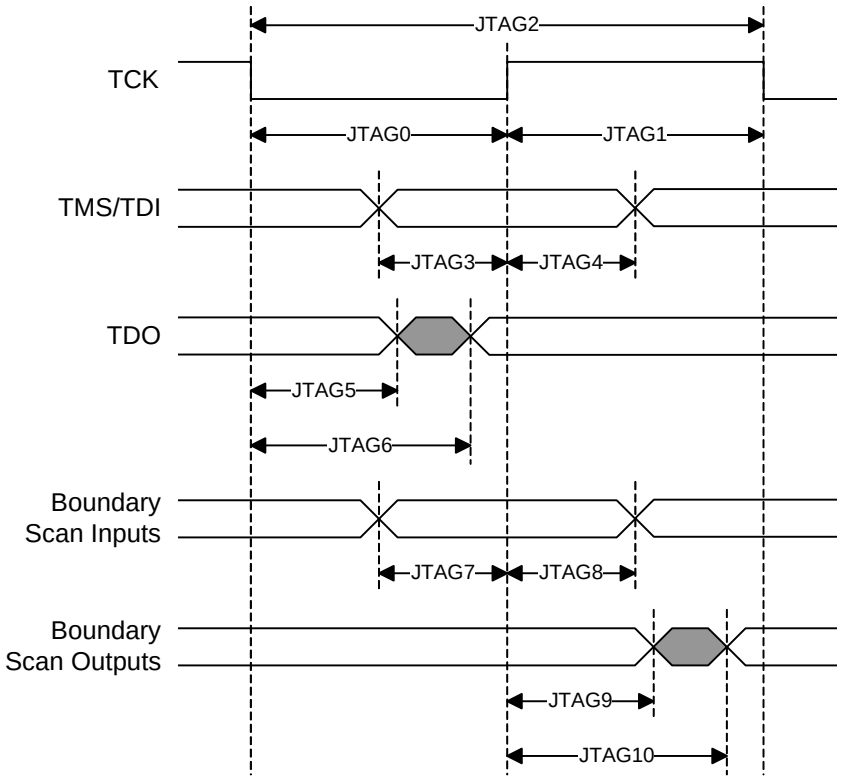
t_{clkpb} = period of TWI peripheral bus clock

$t_{prescaled}$ = period of TWI internal prescaled clock (see chapters on TWIM and TWIS)

The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period ($t_{LOW-TWI}$) of TWCK.

9.10.5 JTAG Timing

Figure 9-17. JTAG Interface Signals



13. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

13.1 Rev. A – 09/12

1. Initial revision.

13.2 Rev. B – 10/12

1. Fixed ordering code
2. Changed BOD18CTRL and BOD33CTRL ACTION field from “Reserved” to ‘No action”

13.3 Rev. C – 02/13

1. Fixed ball pitch for VFBGA100 package
2. Added VFBGA100 and WLCSP64 pinouts
3. Added Power Scaling Mode 2 for high frequency support
4. Minor update on several modules chapters
5. Major update on Electrical characteristics
6. Updated errata
7. Fixed GPIO multiplexing pin numbers

13.4 Rev. D – 03/13

1. Removed WLCSP package information
2. Added errata text for detecting whether a part supports PS2 mode or not
3. Removed temperature sensor feature (not supported by production flow)
4. Fixed MUX selection on Positive ADC input channel table
5. Added information about TWI instances capabilities
6. Added some details on errata Corrupted data in flash may happen after flash page write operations.171

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