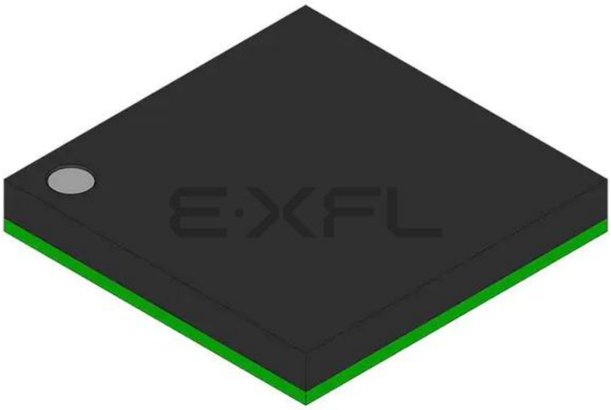

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 7x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-XFBGA, WLCSP
Supplier Device Package	64-WLCSP (4.31x4.43)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/atsam4ls4ba-uur

Figure 3-3. ATSAM4LC WLCSP64 Pinout

	1	2	3	4	5	6	7	8
A	PB04	GNDANA	AD VREFP	VDDANA	PA09	CAPL	CAPH	PA12
B	PB03	XIN32	XOUT32	PA08	PB06	PA10	PA11	VLCD
C	VDDIN	PB01	PA05	PA06	PA07	PB07	PA13	BIASH
D	VDDOUT	PB00	PA04	PB05	PB12	PB08	PA14	BIASL
E	GND	PA03	PB02	RESET_N	PB13	PB09	PA15	GND
F	VDD CORE	TCK	PA02	PB14	PA22	PB10	PA16	VLCDIN
G	GND	PA26	PA24	PA00	PA01	PA19	PA18	PA17
H	VDDIO	PA25	PA23	PB15	PA21	VDDIO	PA20	PB11

Table 3-1. 100-pin GPIO Controller Function Multiplexing (Sheet 4 of 4)

ATSAM4LC		ATSAM4LS		Pin	GPIO	Supply	GPIO Functions						
QFN	VFBGA	QFN	VFBGA				A	B	C	D	E	F	G
59	J6	59	J6	PC16	80	LCDA	TC1 B0			GLOC IN5		LCDCA SEG1	CATB SENSE17
60	H4	60	H4	PC17	81	LCDA	TC1 A1			GLOC IN6		LCDCA SEG2	CATB SENSE18
61	K6	61	K6	PC18	82	LCDA	TC1 B1			GLOC IN7		LCDCA SEG3	CATB SENSE19
62	G4	62	G4	PC19	83	LCDA	TC1 A2			GLOC OUT1		LCDCA SEG4	CATB SENSE20
68	H7	68	H7	PC20	84	LCDA	TC1 B2					LCDCA SEG10	CATB SENSE21
69	K8	69	K8	PC21	85	LCDA	TC1 CLK0			PARC PCCK		LCDCA SEG11	CATB SENSE22
70	J8	70	J8	PC22	86	LCDA	TC1 CLK1			PARC PCEN1		LCDCA SEG12	CATB SENSE23
71	H8	71	H8	PC23	87	LCDA	TC1 CLK2			PARC PCEN2		LCDCA SEG13	CATB DIS
79	J9	79	J9	PC24	88	LCDB	USART1 RTS	EIC EXTINT1	PEVC PAD EVT0	PARC PCDATA0		LCDCA SEG24	CATB SENSE24
80	H9	80	H9	PC25	89	LCDB	USART1 CLK	EIC EXTINT2	PEVC PAD EVT1	PARC PCDATA1		LCDCA SEG25	CATB SENSE25
81	G9	81	G9	PC26	90	LCDB	USART1 RXD	EIC EXTINT3	PEVC PAD EVT2	PARC PCDATA2	SCIF GCLK0	LCDCA SEG26	CATB SENSE26
82	F6	82	F6	PC27	91	LCDB	USART1 TXD	EIC EXTINT4	PEVC PAD EVT3	PARC PCDATA3	SCIF GCLK1	LCDCA SEG27	CATB SENSE27
83	G10	83	G10	PC28	92	LCDB	USART3 RXD	SPI MISO	GLOC IN4	PARC PCDATA4	SCIF GCLK2	LCDCA SEG28	CATB SENSE28
84	F7	84	F7	PC29	93	LCDB	USART3 TXD	SPI MOSI	GLOC IN5	PARC PCDATA5	SCIF GCLK3	LCDCA SEG29	CATB SENSE29
85	F8	85	F8	PC30	94	LCDB	USART3 RTS	SPI SCK	GLOC IN6	PARC PCDATA6	SCIF GCLK IN0	LCDCA SEG30	CATB SENSE30
86	F9	86	F9	PC31	95	LCDB	USART3 CLK	SPI NPCS0	GLOC OUT1	PARC PCDATA7	SCIF GCLK IN1	LCDCA SEG31	CATB SENSE31

Table 3-2. 64-pin GPIO Controller Function Multiplexing (Sheet 1 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
QFP QFN	QFP QFN				A	B	C	D	E	F	G
1	1	PA00	0	VDDIO							
2	2	PA01	1	VDDIO							
3	3	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
10	10	PA03	3	VDDIN		SPI MISO					

3.3 Signals Description

The following table gives details on signal names classified by peripheral.

Table 3-8. Signal Descriptions List (Sheet 1 of 4)

Signal Name	Function	Type	Active Level	Comments
Audio Bitstream DAC - ABDACB				
CLK	D/A clock output	Output		
DAC1 - DAC0	D/A bitstream outputs	Output		
DACN1 - DACN0	D/A inverted bitstream outputs	Output		
Analog Comparator Interface - ACIFC				
ACAN1 - ACAN0	Analog Comparator A negative references	Analog		
ACAP1 - ACAP0	Analog Comparator A positive references	Analog		
ACBN1 - ACBN0	Analog Comparator B negative references	Analog		
ACBP1 - ACBP0	Analog Comparator B positive references	Analog		
ADC controller interface - ADCIFE				
AD14 - AD0	Analog inputs	Analog		
ADVREFP	Positive voltage reference	Analog		
TRIGGER	External trigger	Input		
Backup System Control Interface - BSCIF				
XIN32	32 kHz Crystal Oscillator Input	Analog/ Digital		
XOUT32	32 kHz Crystal Oscillator Output	Analog		
Capacitive Touch Module B - CATB				
DIS	Capacitive discharge line	Output		
SENSE31 - SENSE0	Capacitive sense lines	I/O		
DAC Controller - DACC				
DAC external trigger	DAC external trigger	Input		
DAC voltage output	DAC voltage output	Analog		
Enhanced Debug Port For ARM Products - EDP				
TCK/SWCLK	JTAG / SW Debug Clock	Input		
TDI	JTAG Debug Data In	Input		
TDO/TRACESWO	JTAG Debug Data Out / SW Trace Out	Output		
TMS/SWDIO	JTAG Debug Mode Select / SW Data	I/O		
External Interrupt Controller - EIC				
EXTINT8 - EXTINT0	External interrupts	Input		
Glue Logic Controller - GLOC				
IN7 - IN0	Lookup Tables Inputs	Input		
OUT1 - OUT0	Lookup Tables Outputs	Output		

Memory	Start Address	Size
		ATSAM4Lx8
AESA	0x400B0000	256 bytes
Peripheral Bridge C	0x400E0000	64Kbytes
Peripheral Bridge D	0x400F0000	64Kbytes

Table 5-2. Flash Memory Parameters

Device	Flash Size (*FLASH_PW*)	Number of Pages (*FLASH_P*)	Page Size (*FLASH_W*)
ATSAM4Lx8	512Kbytes	1024	512 bytes
ATSAM4Lx4	256Kbytes	512	512 bytes
ATSAM4Lx2	128Kbytes	256	512 bytes

6.2.2 Typical Powering Schematics

The ATSAM4L8/L4/L2 supports the Single supply mode from 1.68V to 3.6V. Depending on the input voltage range and on the final application frequency, it is recommended to use the following table in order to choose the most efficient power strategy

Figure 6-3. Efficient power strategy:

VDDIN Voltage	1.68V – 1.80V	1.80V – 2.00V	2.00V – 2.30V	2.30V – 3.60V
Switching Mode (BUCK/LDOn (PA02) =1)	N/A		Possible but not efficient	Optimal power efficiency
Linear Mode (BUCK/LDOn (PA02) =0)	Optimal power efficiency			Possible but not efficient
F_{CPUMAX}	12MHz	Up to 36MHz In PS0 Up to 12MHz in PS1 Up to 48MHz in PS2		
PowerScaling	PS1(1)	ALL		
Typical power consumption in RUN mode	ℵ 212µA/MHz @ F_{CPU}=12MHz(PS1) ℵ 306µA/MHz @ F_{CPU}= 48MHz(PS2)			ℵ 100µA/MHz @ F_{CPU}=12MHz(PS1) @ V_{VDDIN}=3.3V ℵ 180µA/MHz @ F_{CPU}=48MHz(PS2) @ V_{VDDIN}=3.3V
Typical power consumption in RET mode	1.5µA			

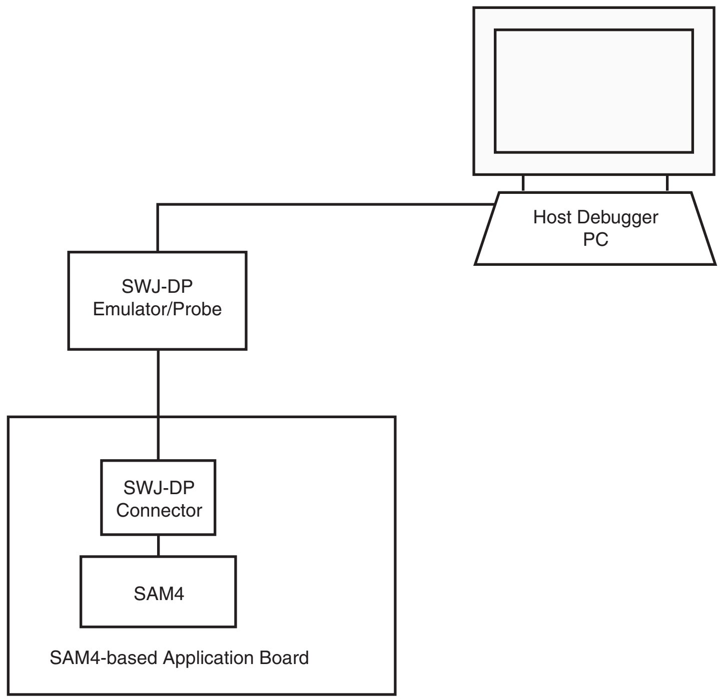
Note 1. The SAM4L boots in PS0 on RCSYS(115kHz), then the application must switch to PS1 before running on higher frequency (<12MHz)

8.11 Functional Description

8.11.1 Debug Environment

Figure 8-8 shows a complete debug environment example. The SWJ-DP interface is used for standard debugging functions, such as downloading code and single-stepping through the program and viewing core and peripheral registers.

Figure 8-8. Application Debug Environment Example



8.11.2 Test Environment

Figure 8-9 shows a test environment example (JTAG Boundary scan). Test vectors are sent and interpreted by the tester. In this example, the "board in test" is designed using a number of JTAG-compliant devices. These devices can be connected to form a single scan chain.

9.4 Maximum Clock Frequencies

Table 9-4. Maximum Clock Frequencies in Power Scaling Mode 0/2 and RUN Mode

Symbol	Parameter	Description	Max	Units
f_{CPU}	CPU clock frequency		48	MHz
f_{PBA}	PBA clock frequency		48	
f_{PBB}	PBB clock frequency		48	
f_{PBC}	PBC clock frequency		48	
f_{PBD}	PBD clock frequency		48	
f_{GCLK0}	GCLK0 clock frequency	DFLLIF main reference, GCLK0 pin	50	
f_{GCLK1}	GCLK1 clock frequency	DFLLIF dithering and SSG reference, GCLK1 pin	50	
f_{GCLK2}	GCLK2 clock frequency	AST, GCLK2 pin	20	
f_{GCLK3}	GCLK3 clock frequency	CATB, GCLK3 pin	50	
f_{GCLK4}	GCLK4 clock frequency	FLO and AESA	50	
f_{GCLK5}	GCLK5 clock frequency	GLOC, TC0 and RC32KIFB_REF	80	
f_{GCLK6}	GCLK6 clock frequency	ABDACB and IISC	50	
f_{GCLK7}	GCLK7 clock frequency	USBC	50	
f_{GCLK8}	GCLK8 clock frequency	TC1 and PEVC[0]	50	
f_{GCLK9}	GCLK9 clock frequency	PLL0 and PEVC[1]	50	
f_{GCLK10}	GCLK10 clock frequency	ADCIFE	50	
f_{GCLK11}	GCLK11 clock frequency	Master generic clock. Can be used as source for other generic clocks	150	
f_{OSC0}	OSC0 output frequency	Oscillator 0 in crystal mode	30	
		Oscillator 0 in digital clock mode	50	
f_{PLL}	PLL output frequency	Phase Locked Loop	240	
f_{DFLL}	DFLL output frequency	Digital Frequency Locked Loop	220	
f_{RC80M}	RC80M output frequency	Internal 80MHz RC Oscillator	80	

Table 9-6. ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max [1]	Unit
SLEEP0	Switching mode	25°C	9 * Main clock cycles	3817	4033	µA
		85°C		3934	4174	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	2341	2477	
		85°C		2437	2585	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	1758	1862	
		85°C		1847	1971	
SLEEP3	Linear mode	25°C		51	60	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	5.9	8.7	
	OSC32K and AST stopped Fast wake-up enable			4.7	7.6	
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.1	5.1	
	AST and OSC32K stopped			2.2	4.2	
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-7. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max [1]	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	319	343	µA/MHz
		85°C		326	350	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	343	387	
		85°C		351	416	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	181	198	
		85°C		186	203	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	192	232	
		85°C		202	239	

Table 9-17. TWI Pin Characteristics in GPIO configuration [1]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{RISE}	Rise time[2]	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		18		ns
		OSRR0=1			110		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		10		ns
		OSRR0=1			50		
t_{FALL}	Fall time[2]	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		19		ns
		OSRR0=1			140		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		12		ns
		OSRR0=1			63		

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Table 9-18. Common TWI Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LEAK}	Input leakage current [1]	Pull-up resistors disabled		0.01	1	µA
C_{IN}	Input capacitance[2]			5		pF

1. These values are based on simulation. These values are not covered by test limits in production or characterization

9.6.5 High Drive TWI Pin : PB00, PB01

Table 9-19. High Drive TWI Pin Characteristics in TWI configuration [(1)]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance [(2)]	PB00, PB01			40		kΩ
$R_{PULLDOWN}$	Pull-down resistance[(2)]				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.3 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.7 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			V
I_{OL}	Output low-level current [(3)]	DRIVEL=0				0.5	mA
		DRIVEL=1				1.0	
		DRIVEL=2				1.6	
		DRIVEL=3				3.1	
		DRIVEL=4				6.2	
		DRIVEL=5				9.3	
		DRIVEL=6				15.5	
		DRIVEL=7				21.8	
I_{CS}	Current Source[(2)]	DRIVEH=0			0.5		mA
		DRIVEH=1			1		
		DRIVEH=2			1.5		
		DRIVEH=3			3		
f_{MAX}	Max frequency[(2)]	HsMode with Current source; DRIVEx=3, SLEW=0 Cbus = 400pF, V_{VDD} = 1.68V		3.5	6.4		MHz
t_{RISE}	Rise time[(2)]	HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			28	38	ns
t_{FALL}	Fall time[(2)]	Standard Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	ns
		HsMode Mode, DRIVEx=3, SLEW=0 Cbus = 400pF, Rp = 440Ohm, V_{VDD} = 1.68V			50	95	

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.7 Oscillator Characteristics

9.7.1 Oscillator 0 (OSC0) Characteristics

9.7.1.1 Digital Clock Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN.

Table 9-22. Digital Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CPXIN}	XIN clock frequency [(1)]				50	MHz
t_{CPXIN}	XIN clock duty cycle[(1)]		40		60	%
$t_{STARTUP}$	Startup time			N/A		cycles

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.7.1.2 Crystal Oscillator Characteristics

The following table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT as shown in Figure 9-3. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can be found in the crystal datasheet. The capacitance of the external capacitors (C_{LEXT}) can then be computed as follows:

$$C_{LEXT} = 2(C_L - C_{STRAY} - C_{SHUNT})$$

where C_{STRAY} is the capacitance of the pins and PCB, C_{SHUNT} is the shunt capacitance of the crystal.

Table 9-23. Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Crystal oscillator frequency [(1)]		0.6		30	MHz
ESR	Crystal Equivalent Series Resistance [(2)]	f = 0.455MHz, C_{LEXT} = 100pF SCIF.OSCCTRL.GAIN = 0			17000	Ω
		f = 2MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 0			2000	
		f = 4MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 1			1500	
		f = 8MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 2			300	
		f = 16MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 3			350	
		f = 30MHz, C_{LEXT} = 18pF SCIF.OSCCTRL.GAIN = 4			45	

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-35. Flash Endurance and Data Retention [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{FARRAY}	Array endurance (write/page)	f_{CLK_AHB} > 10MHz	100k			cycles
N_{FFUSE}	General Purpose fuses endurance (write/bit)	f_{CLK_AHB} > 10MHz	10k			cycles
t_{RET}	Data retention		15			years

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.10.3 SPI Timing

9.10.3.1 Master mode

Figure 9-12. SPI Master Mode with (CPOL= NCPHA= 0) or (CPOL= NCPHA= 1)

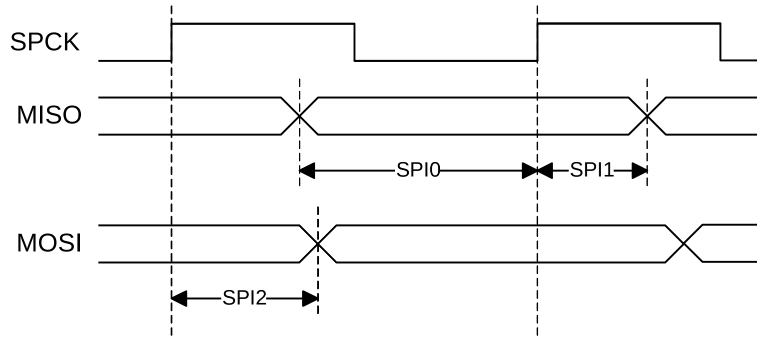


Figure 9-13. SPI Master Mode with (CPOL= 0 and NCPHA= 1) or (CPOL= 1 and NCPHA= 0)

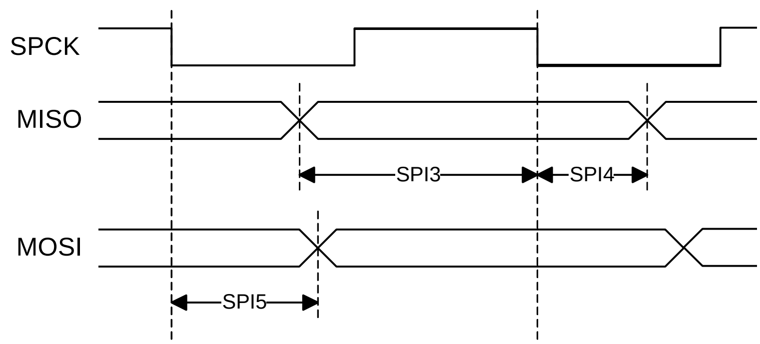


Table 9-62. SPI Timing, Master Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
SPI0	MISO setup time before SPCK rises	V_{VDDIO} from 2.85V to 3.6V, maximum external capacitor = 40pF	9		ns
SPI1	MISO hold time after SPCK rises		0		
SPI2	SPCK rising to MOSI delay		9	21	
SPI3	MISO setup time before SPCK falls		7.3		
SPI4	MISO hold time after SPCK falls		0		
SPI5	SPCK falling to MOSI delay		9	22	

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

Maximum SPI Frequency, Master Output

Figure 9-16. SPI Slave Mode, NPCS Timing

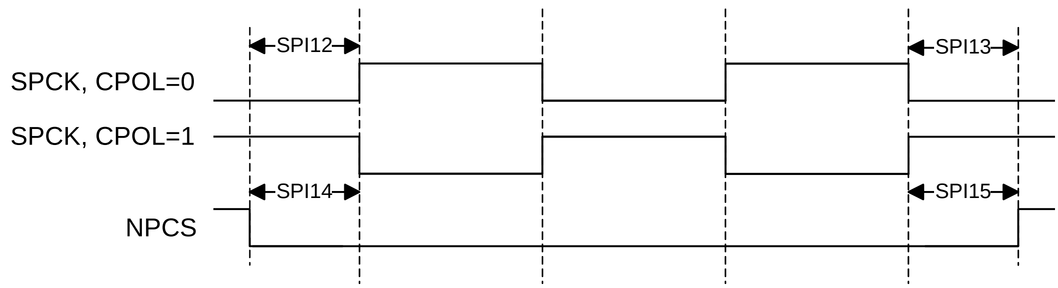


Table 9-63. SPI Timing, Slave Mode[(1)]

Symbol	Parameter	Conditions	Min	Max	Units
SPI6	SPCK falling to MISO delay	V_{VDDIO} from 2.85V to 3.6V, maximum external capacitor = 40pF	19	47	ns
SPI7	MOSI setup time before SPCK rises		0		
SPI8	MOSI hold time after SPCK rises		5.4		
SPI9	SPCK rising to MISO delay		19	46	
SPI10	MOSI setup time before SPCK falls		0		
SPI11	MOSI hold time after SPCK falls		5.3		
SPI12	NPCS setup time before SPCK rises		4		
SPI13	NPCS hold time after SPCK falls		2.5		
SPI14	NPCS setup time before SPCK falls		6		
SPI15	NPCS hold time after SPCK rises		1.1		

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{CLKSPI}, \frac{1}{SPIn})$$

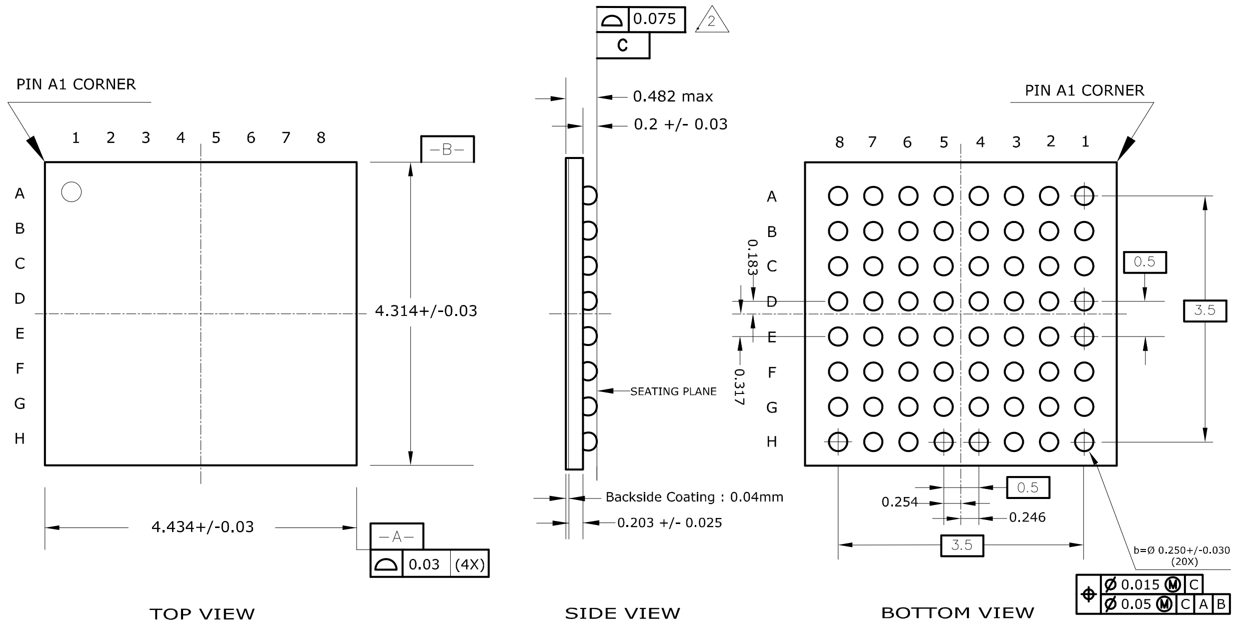
Where $SPIn$ is the MOSI setup and hold time, SPI7 + SPI8 or SPI10 + SPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

Figure 10-4. WLCSP64 SAM4LS4/2 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.746	1.683
A2	GNDANA	1.246	1.683
A3	ADVREFP	0.746	1.683
A4	VDDANA	0.246	1.683
A5	PA09	-0.254	1.683
A6	PA28	-0.754	1.683
A7	PA27	-1.254	1.683
A8	PA12	-1.754	1.683
B1	PB03	1.746	1.183
B2	XIN32	1.246	1.183
B3	XOUT32	0.746	1.183
B4	PA08	0.246	1.183
B5	PB06	-0.254	1.183
B6	PA10	-0.754	1.183
B7	PA11	-1.254	1.183
B8	PA29	-1.754	1.183
C1	VDDIN	1.746	0.683
C2	PB01	1.246	0.683
C3	PA05	0.746	0.683
C4	PA06	0.246	0.683
C5	PA07	-0.254	0.683
C6	PB07	-0.754	0.683

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	-1.254	0.683
C8	GNDIO0	-1.754	0.683
D1	VDDOUT	1.746	0.183
D2	PB00	1.246	0.183
D3	PA04	0.746	0.183
D4	PB05	0.246	0.183
D5	PB12	-0.254	0.183
D6	PB08	-0.754	0.183
D7	PA14	-1.254	0.183
D8	VLCDIN	-1.754	0.183
E1	GNDIN	1.746	-0.317
E2	PA03	1.246	-0.317
E3	PB02	0.746	-0.317
E4	RESET_N	0.246	-0.317
E5	PB13	-0.254	-0.317
E6	PB09	-0.754	-0.317
E7	PA15	-1.254	-0.317
E8	PA30	-1.754	-0.317
F1	VDDCORE	1.746	-0.817
F2	TCK	1.246	-0.817
F3	PA02	0.746	-0.817
F4	PB14	0.246	-0.817

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.254	-0.817
F6	PB10	-0.754	-0.817
F7	PA16	-1.254	-0.817
F8	PA31	-1.754	-0.817
G1	GNDIO1	1.746	-1.317
G2	PA26	1.246	-1.317
G3	PA24	0.746	-1.317
G4	PA00	0.246	-1.317
G5	PA01	-0.254	-1.317
G6	PA19	-0.754	-1.317
G7	PA18	-1.254	-1.317
G8	PA17	-1.754	-1.317
H1	VDDIO1	1.746	-1.817
H2	PA25	1.246	-1.817
H3	PA23	0.746	-1.817
H4	PB15	0.246	-1.817
H5	PA21	-0.254	-1.817
H6	VDDIO0	-0.754	-1.817
H7	PA20	-1.254	-1.817
H8	PB11	-1.754	-1.817

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-11. Device and Package Maximum Weight

14.8	mg

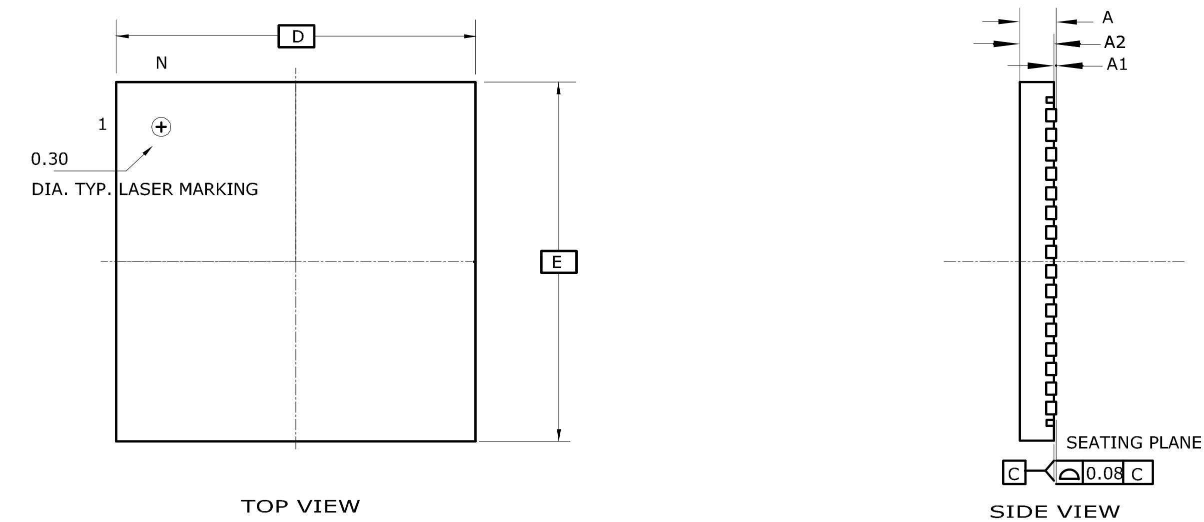
Table 10-12. Package Characteristics

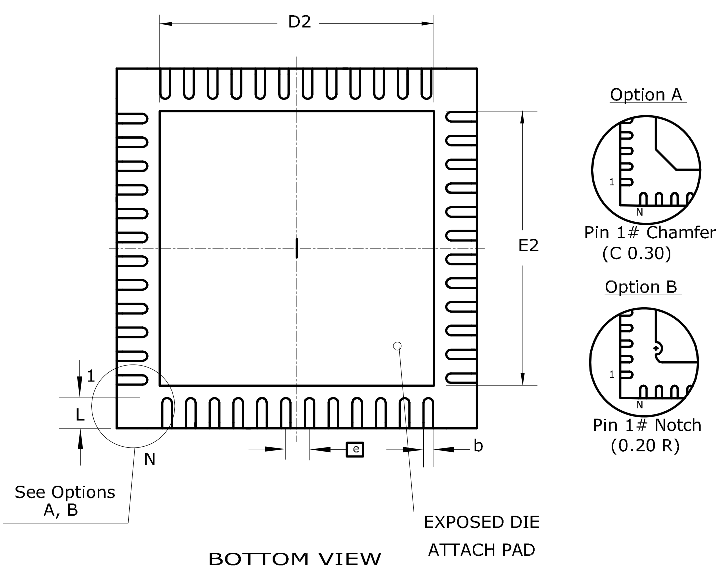
Moisture Sensitivity Level	MSL3

Table 10-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

Figure 10-11. QFN-48 Package Drawing for ATSAM4LC8 and ATSAM4LS8





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A2	0.75	-----	1.00	
D/E		7 BSC		
D2/E2	5.50	5.60	5.70	
L	0.30	0.40	0.50	
b	0.17	-----	0.30	2
e		0.50 BSC		
n		48		

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 10-32. Device and Package Maximum Weight

140	mg

Table 10-33. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-34. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

10.3 Soldering Profile

Table 10-35 gives the recommended soldering profile from J-STD-20.

Table 10-35. Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150-200°C
Time Maintained Above 217°C	60-150 s
Time within 5·C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp-down Rate	6°C/s max
Time 25·C to Peak Temperature	8 minutes max

A maximum of three reflow passes is allowed per component.

Table 11-5. ATSAM4LS4 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LS4CA-AU-ES	256	32	TQFP100	ES	Green	N/A
ATSAM4LS4CA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LS4CA-AUR				Reel		
ATSAM4LS4CA-CFU			VFBGA100	Tray		Industrial -40°C to 85°C
ATSAM4LS4CA-CFUR				Reel		
ATSAM4LS4BA-AU-ES			TQFP64	ES		N/A
ATSAM4LS4BA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LS4BA-AUR				Reel		
ATSAM4LS4BA-MU-ES			QFN64	ES		N/A
ATSAM4LS4BA-MU				Tray		Industrial -40°C to 85°C
ATSAM4LS4BA-MUR				Reel		
ATSAM4LS4BA-UUR			WLCSP64	Reel		Industrial -40°C to 85°C
ATSAM4LS4AA-AU-ES			TQFP48	ES		N/A
ATSAM4LS4AA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LS4AA-AUR				Reel		
ATSAM4LS4AA-MU-ES			QFN48	ES		N/A
ATSAM4LS4AA-MU				Tray		Industrial -40°C to 85°C
ATSAM4LS4AA-MUR				Reel		

Table 11-6. ATSAM4LS2 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LS2CA-AU	128	32	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS2CA-AUR				Reel		
ATSAM4LS2CA-CFU			VFBGA100	Tray		
ATSAM4LS2CA-CFUR				Reel		
ATSAM4LS2BA-AU			TQFP64	Tray		
ATSAM4LS2BA-AUR				Reel		
ATSAM4LS2BA-MU			QFN64	Tray		
ATSAM4LS2BA-MUR				Reel		
ATSAM4LS2BA-UUR			WLCSP64	Reel		
ATSAM4LS2AA-AU			TQFP48	Tray		
ATSAM4LS2AA-AUR				Reel		
ATSAM4LS2AA-MU			QFN48	Tray		
ATSAM4LS2AA-MUR				Reel		

12. Errata

12.1 ATSAM4L4 /2 Rev. B & ATSAM4L8 Rev. A

12.1.1 General

PS2 mode is not supported by Engineering Samples
PS2 mode support is supported only by parts with calibration version higher than 0.
Fix/Workaround
The calibration version can be checked by reading a 32-bit word at address 0x0080020C. The calibration version bitfield is 4-bit wide and located from bit 4 to bit 7 in this word. Any value higher than 0 ensures that the part supports the PS2 mode

12.1.2 SCIF

PLLCOUNT value larger than zero can cause PLLEN glitch
Initializing the PLLCOUNT with a value greater than zero creates a glitch on the PLLEN signal during asynchronous wake up.
Fix/Workaround
The lock-masking mechanism for the PLL should not be used.
The PLLCOUNT field of the PLL Control Register should always be written to zero.

12.1.3 WDT

WDT Control Register does not have synchronization feedback
When writing to the Timeout Prescale Select (PSEL), Time Ban Prescale Select (TBAN), Enable (EN), or WDT Mode (MODE) fieldss of the WDT Control Register (CTRL), a synchronizer is started to propagate the values to the WDT clcok domain. This synchronization takes a finite amount of time, but only the status of the synchronization of the EN bit is reflected back to the user. Writing to the synchronized fields during synchronization can lead to undefined behavior.
Fix/Workaround
-When writing to the affected fields, the user must ensure a wait corresponding to 2 clock cycles of both the WDT peripheral bus clock and the selected WDT clock source.
-When doing writes that changes the EN bit, the EN bit can be read back until it reflects the written value.

12.1.4 SPI

SPI data transfer hangs with CSR0.CSAAT==1 and MR.MODFDIS==0
When CSR0.CSAAT==1 and mode fault detection is enabled (MR.MODFDIS==0), the SPI module will not start a data transfer.
Fix/Workaround
Disable mode fault detection by writing a one to MR.MODFDIS.

SPI disable does not work in SLAVE mode
SPI disable does not work in SLAVE mode.

13. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

13.1 Rev. A – 09/12

1. Initial revision.

13.2 Rev. B – 10/12

1. Fixed ordering code
2. Changed BOD18CTRL and BOD33CTRL ACTION field from “Reserved” to ‘No action”

13.3 Rev. C – 02/13

1. Fixed ball pitch for VFBGA100 package
2. Added VFBGA100 and WLCSP64 pinouts
3. Added Power Scaling Mode 2 for high frequency support
4. Minor update on several modules chapters
5. Major update on Electrical characteristics
6. Updated errata
7. Fixed GPIO multiplexing pin numbers

13.4 Rev. D – 03/13

1. Removed WLCSP package information
2. Added errata text for detecting whether a part supports PS2 mode or not
3. Removed temperature sensor feature (not supported by production flow)
4. Fixed MUX selection on Positive ADC input channel table
5. Added information about TWI instances capabilities
6. Added some details on errata Corrupted data in flash may happen after flash page write operations.171