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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	80
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls4ca-au

Table 2-2. ATSAM4LC Configuration Summary

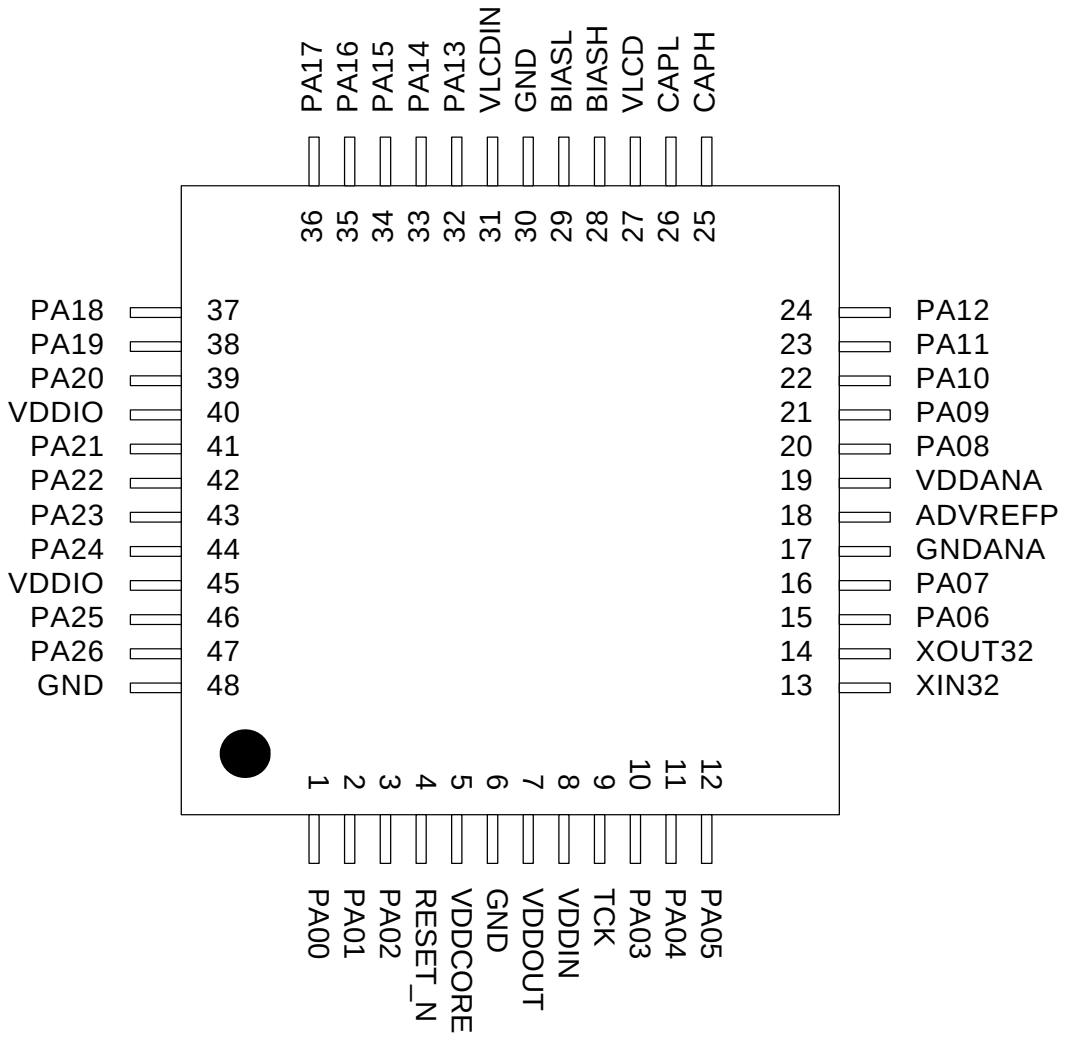
Feature	ATSAM4LC8/4/2C	ATSAM4LC8/4/2B	ATSAM4LC8/4/2A
Oscillators	Digital Frequency Locked Loop 20-150MHz (DFLL) Phase Locked Loop 48-240MHz (PLL) Crystal Oscillator 0.6-30MHz (OSC0) Crystal Oscillator 32kHz (OSC32K) RC Oscillator 80MHz (RC80M) RC Oscillator 4,8,12MHz (RCFAST) RC Oscillator 115kHz (RCSYS) RC Oscillator 32kHz (RC32K)		
ADC	15-channel	7-channel	3-channel
DAC	1-channel		
Analog Comparators	4	2	1
CATB Sensors	32	32	26
USB	1		
Audio Bitstream DAC	1		
IIS Controller	1		
Packages	TQFP/VFBGA	TQFP/QFN/ WLCSP	TQFP/QFN

.

Table 2-3. ATSAM4LS Configuration Summary

Feature	ATSAM4LS8/4/2C	ATSAM4LS8/4/2B	ATSAM4LS8/4/2A
Number of Pins	100	64	48
Max Frequency	48MHz		
Flash	512/256/128KB		
SRAM	64/32/32KB		
SEGMENT LCD	NA		
GPIO	80	48	32
High-drive pins	6	3	1
External Interrupts	8 + 1 NMI		
TWI	2 Masters + 2 Masters/Slaves		1 Master + 1 Master/Slave
USART	4		3 in LC sub series 4 in LS sub series
PICOUART	1		0
Peripheral DMA Channels	16		
AESA	NA		
Peripheral Event System	1		
SPI	1		
Asynchronous Timers	1		

Figure 3-5. ATSAM4LC TQFP48/QFN48 Pinout



3.1.2 ATSAM4LSx Pinout

Figure 3-6. ATSAM4LS TQFP100 Pinout

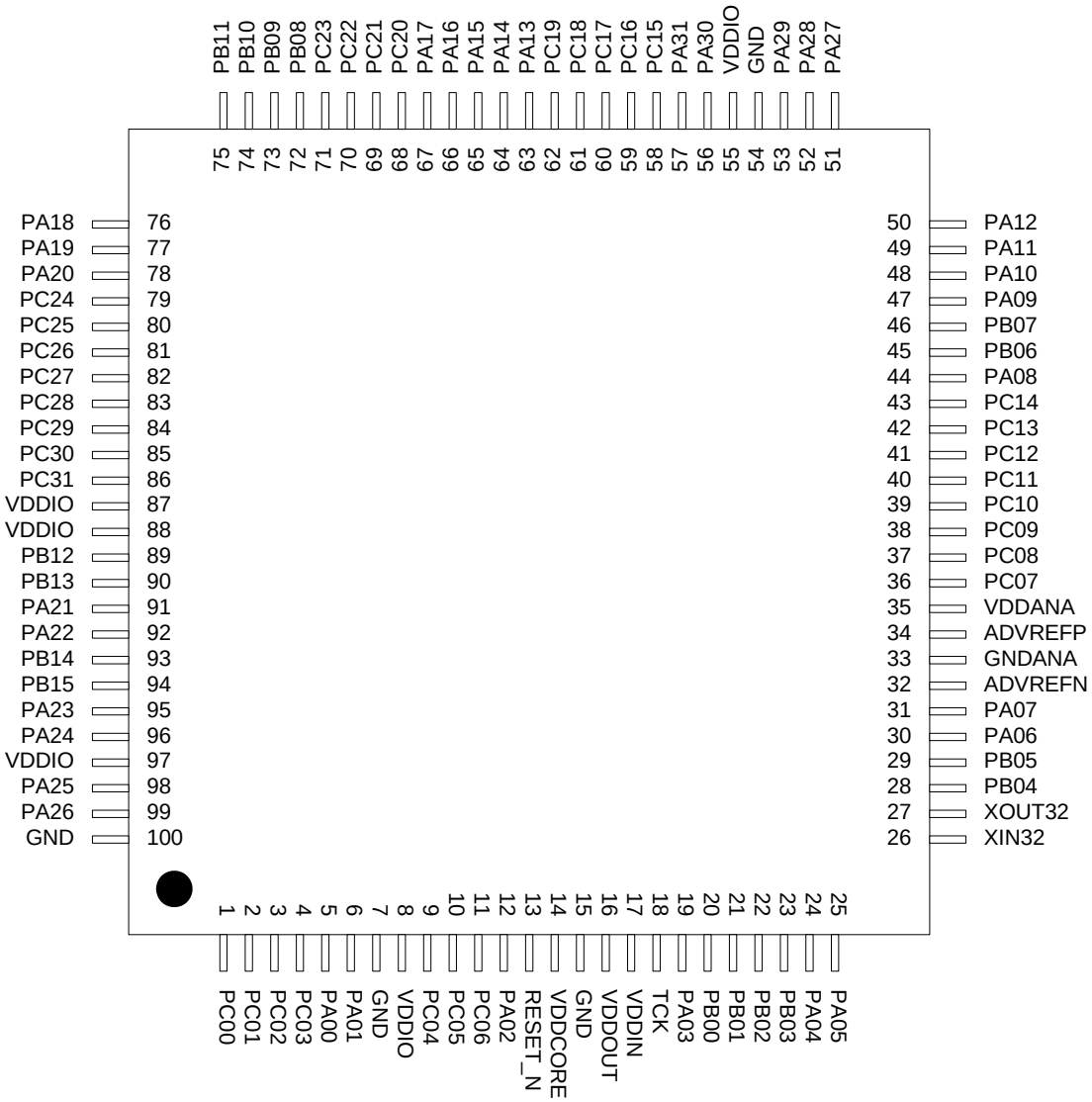


Table 3-8. Signal Descriptions List (Sheet 2 of 4)

Signal Name	Function	Type	Active Level	Comments
Inter-IC Sound (I2S) Controller - IISC				
IMCK	I2S Master Clock	Output		
ISCK	I2S Serial Clock	I/O		
ISDI	I2S Serial Data In	Input		
ISDO	I2S Serial Data Out	Output		
IWS	I2S Word Select	I/O		
LCD Controller - LCDCA				
BIASL	Bias voltage (1/3 VLCD)	Analog		
BIASH	Bias voltage (2/3 VLCD)	Analog		
CAPH	High voltage end of flying capacitor	Analog		
CAPL	Low voltage end of flying capacitor	Analog		
COM3 - COM0	Common terminals	Analog		
SEG39 - SEG0	Segment terminals	Analog		
VLCD	Bias voltage	Analog		
Parallel Capture - PARC				
PCCK	Clock	Input		
PCDATA7 - PCDATA0	Data lines	Input		
PCEN1	Data enable 1	Input		
PCEN2	Data enable 2	Input		
Peripheral Event Controller - PEVC				
PAD_EVT3 - PAD_EVT0	Event Inputs	Input		
Power Manager - PM				
RESET_N	Reset	Input	Low	
System Control Interface - SCIF				
GCLK3 - GCLK0	Generic Clock Outputs	Output		
GCLK_IN1 - GCLK_IN0	Generic Clock Inputs	Input		
XIN0	Crystal 0 Input	Analog/ Digital		
XOUT0	Crystal 0 Output	Analog		
Serial Peripheral Interface - SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS3 - NPCS0	SPI Peripheral Chip Selects	I/O	Low	
SCK	Clock	I/O		
Timer/Counter - TC0, TC1				

Table 3-8. Signal Descriptions List (Sheet 4 of 4)

Signal Name	Function	Type	Active Level	Comments
PA31 - PA00	Parallel I/O Controller I/O Port A	I/O		
PB15 - PB00	Parallel I/O Controller I/O Port B	I/O		
PC31 - PC00	Parallel I/O Controller I/O Port C	I/O		

Note: 1. See "Power and Startup Considerations" section.

3.4 I/O Line Considerations

3.4.1 SW/JTAG Pins

The JTAG pins switch to the JTAG functions if a rising edge is detected on TCK low after the RESET_N pin has been released. The TMS, and TDI pins have pull-up resistors when used as JTAG pins. The TCK pin always has pull-up enabled during reset. The JTAG pins can be used as GPIO pins and multiplexed with peripherals when the JTAG is disabled. Refer to Section 3.2.3 "JTAG Port Connections" on page 29 for the JTAG port connections.

For more details, refer to Section 1.1 "Enhanced Debug Port (EDP)" on page 3.

3.4.2 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIN. As the product integrates a power-on reset detector, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

3.4.3 TWI Pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and-inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as GPIO pins.

3.4.4 GPIO Pins

All the I/O lines integrate a pull-up/pull-down resistor and slew rate controller. Programming these features is performed independently for each I/O line through the GPIO Controllers. After reset, I/O lines default as inputs with pull-up and pull-down resistors disabled and slew rate enabled.

3.4.5 High-drive Pins

The six pins PA02, PB00, PB01, PC04, PC05 and PC06 have high-drive output capabilities. Refer to Section 9.6.2 "High-drive I/O Pin : PA02, PC04, PC05, PC06" on page 115 for electrical characteristics.

3.4.6 USB Pins

When these pins are used for USB, the pins are behaving according to the USB specification. When used as GPIO pins or used for other peripherals, the pins have the same behavior as other normal I/O pins, but the characteristics are different. Refer to Section 9.6.3 "USB I/O Pin : PA25, PA26" on page 116 for electrical characteristics.

These pins are compliant to USB standard only when VDDIO power supply is 3.3V nominal.

3.4.7 ADC Input Pins

These pins are regular I/O pins powered from the VDDANA.

7.1.5 Power Save Mode Summary Table

The following table shows a summary of the main Power Save modes:

Table 7-2. Power Save mode Configuration Summary

Mode	Mode Entry	Wake up sources	Core domain	Backup domain
SLEEP	WFI SCR.SLEEPDEEP bit = 0 BPM.PMCON.BKUP bit = 0	Any interrupt	CPU clock OFF Other clocks OFF depending on the BPM.PMCON.SLEEP field see "SLEEP mode" on page 56	Clocks OFF depending on the BPM.PMCON.SLEEP field see "SLEEP mode" on page 56
WAIT	WFI SCR.SLEEPDEEP bit = 1 BPM.PMCON.RET bit = 0 BPM.PMCON.BKUP bit = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running
RETENTION	WFI SCR.SLEEPDEEP bit = 1 BPM.PMCON.RET bit = 1 BPM.PMCON.BKUP bit = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running
BACKUP	WFI + SCR.SLEEPDEEP bit = 1 + BPM.PMCON.BKUP bit = 1	EIC interrupt BOD33, BOD18 interrupt and reset AST alarm, periodic, overflow WDT interrupt and reset external reset on RESET_N pin	OFF (not powered)	All clocks are OFF except RC32K or OSC32K if running

7.2 Power Scaling

The Power Scaling technique consists of adjusting the internal regulator output voltage (voltage scaling) to reduce the power consumption. According to the requirements in terms of performance, operating modes, and current consumption, the user can select the Power Scaling configuration that fits the best with its application.

The Power Scaling configuration field (PMCON.PS) is provided in the Backup Power Manager (BPM) module.

In RUN mode, the user can adjust on the fly the Power Scaling configuration

The Figure 7.1 summarizes the different combination of the Power Scaling configuration which can be applied according to the Power Save Mode.

Power scaling from a current power configuration to a new power configuration is done by halting the CPU execution

Power scaling occurs after a WFI instruction. The system is halted until the new power configuration is stabilized. After handling the PM interrupt, the system resumes from WFI.

To scale the power, the following sequence is required:

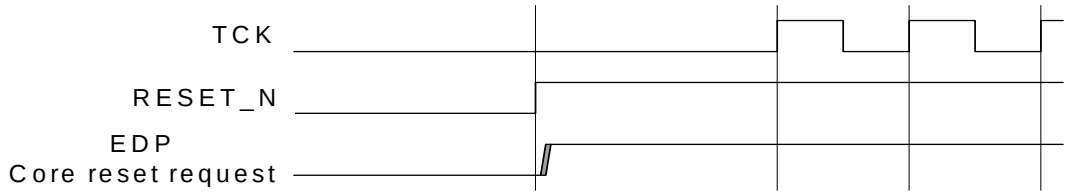
- Check the BPM.SR.PSOK bit to make sure the current power configuration is stabilized.

The Debug Port pins assignation is then forced to the EDP function even if they were already assigned to another module. This allows to connect a debugger at any time without reseting the device. The connection is non-intrusive meaning that the chip will continue its execution without being disturbed. The CPU can of course be halted later on by issuing Cortex-M4 OCD features.

8.7.8 SMAP Core Reset Request Source

The EDP has the ability to send a request to the SMAP for a Cortex-M4 Core reset. The procedure to do so is to hold TCK low until RESET_N is released. This mechanism aims at halting the CPU to prevent it from changing the system configuration while the SMAP is operating.

Figure 8-5. SMAP Core Reset Request Timings Diagram



The SMAP can de-assert the core reset request for this operation, refer to Section 2.8.8 ”Cortex-M4 Core Reset Source” on page 57.

8.7.9 SWJ-DP

The Cortex-M4 embeds a SWJ-DP Debug port which is the standard CoreSight™ debug port. It combines Serial Wire Debug Port (SW-DP), from 2 to 3 pins and JTAG debug Port(JTAG-DP), 5 pins.

By default, the JTAG Debug Port is active. If the host debugger wants to switch to the Serial Wire Debug Port, it must provide a dedicated JTAG sequence on TMS/SWDIO and TCK/SWCLK which disables JTAG-DP and enables SW-DP.

When the EDP has been switched to Serial Wire mode, TDO/TRACESWO can be used for trace (for more information refer to the section below). The asynchronous TRACE output (TRACESWO) is multiplexed with TDO. So the asynchronous trace can only be used with SW-DP, not JTAG-DP.

The SWJ-DP provides access to the AHB-AP and SMAP access ports which have the following APSEL value:

Figure 8-6. Access Ports APSEL

Acces Port (AP)	APSEL
AHB-AP	0
SMAP	1

Refer to the ARM Debug Interface v5.1 Architecture Specification for more details on SWJ-DP.

8.9.11.5 Length Register

Name: LENGTH

Access Type: Read/Write

Offset: 0x10

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
LENGTH							

23	22	21	20	19	18	17	16
LENGTH							

15	14	13	12	11	10	9	8
LENGTH							

7	6	5	4	3	2	1	0
LENGTH						-	-

- **LENGTH: Length Value, Bits 1-0 are always zero**

Table 9-3. Supply Rise Rates and Order [1]

VDDIO, VDDIN and VDDANA must be connected together and as a consequence, rise synchronously

Symbol	Parameter	Rise Rate			
		Min	Max	Unit	Comment
V_{VDDIO}	DC supply peripheral I/Os	0.0001	2.5	V/µs	
V_{VDDIN}	DC supply peripheral I/Os and internal regulator	0.0001	2.5	V/µs	
V_{VDDANA}	Analog supply voltage	0.0001	2.5	V/µs	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-9. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 1

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	222	240	µA/MHz
		85°C		233	276	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	233	276	
		85°C		230	270	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	100	112	
		85°C		100	119	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	104	128	
		85°C		107	138	
SLEEP0	Switching mode	25°C	9 * Main clock cycles	527	627	µA
		85°C		579	739	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	369	445	
		85°C		404	564	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	305	381	
		85°C		334	442	
SLEEP3	Linear mode	25°C		46	55	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	5.5		
	OSC32K and AST stopped Fast wake-up enable			4.3		
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.4		
	AST and OSC32K stopped			2.3		
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-10. Typical Power Consumption running CoreMark on CPU clock sources (1)

Clock Source	Conditions	Regulator	Frequency (MHz)	Typ	Unit

3. These values are based on characterization. These values are not covered by test limits in production

9.6.2 High-drive I/O Pin : PA02, PC04, PC05, PC06

Table 9-14. High-drive I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.8	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	
		ODCR0=1	1.68V<V_{VDD}<2.7V			3.2	mA
			2.7V<V_{VDD}<3.6V			6	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF			20	ns
		OSRR0=1				40	
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF			11	ns
		OSRR0=1				18	
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			22	MHz
		OSRR0=1				17	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			35	MHz
		OSRR0=1				26	MHz
I_{LEAK}	Input leakage current(3)	Pull-up resistors disabled			0.01	2	µA
C_{IN}	Input capacitance(2)				10		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.6.3 USB I/O Pin : PA25, PA26

Table 9-15. USB I/O Pin Characteristics in GPIO configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V		20		mA
			2.7V<V_{VDD}<3.6V		30		
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V		20		mA
			2.7V<V_{VDD}<3.6V		30		
F_{PINMAX}	Maximum frequency(2)	ODCR0=0 OSRR0=0	load = 25pF			20	MHz
I_{LEAK}	Input leakage current(3)	Pull-up resistors disabled			0.01	1	µA
C_{IN}	Input capacitance(2)				5		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

9.6.4 TWI Pin : PA21, PA22, PA23, PA24, PB14, PB15

Table 9-16. TWI Pin Characteristics in TWI configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.3 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.7 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
I_{OL}	Output low-level current (3)	DRIVEL=0				0.5	mA
		DRIVEL=1				1.0	
		DRIVEL=2				1.6	
		DRIVEL=3				3.1	
		DRIVEL=4				6.2	
		DRIVEL=5				9.3	
		DRIVEL=6				15.5	
		DRIVEL=7				21.8	

Table 9-20. High Drive TWI Pin Characteristics in GPIO configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-up resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			3.4	mA
			2.7V<V_{VDD}<3.6V			6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			5.2	mA
			2.7V<V_{VDD}<3.6V			8	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			3.4	mA
			2.7V<V_{VDD}<3.6V			6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			5.2	mA
			2.7V<V_{VDD}<3.6V			8	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		18		ns
		OSRR0=1			110		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		10		ns
		OSRR0=1			50		
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		19		ns
		OSRR0=1			140		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		12		ns
		OSRR0=1			63		

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Table 9-21. Common High Drive TWI Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LEAK}	Input leakage current (1)	Pull-up resistors disabled		0.01	2	µA
C_{IN}	Input capacitance(1)			10		pF

1. These values are based on simulation. These values are not covered by test limits in production or characterization

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-35. Flash Endurance and Data Retention [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{FARRAY}	Array endurance (write/page)	f_{CLK_AHB} > 10MHz	100k			cycles
N_{FFUSE}	General Purpose fuses endurance (write/bit)	f_{CLK_AHB} > 10MHz	10k			
t_{RET}	Data retention		15			years

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Where $SPIn$ is the MISO delay, SPI6 or SPI9 depending on CPOL and NCPHA. t_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for t_{SETUP} . f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

9.10.4 TWIM/TWIS Timing

Figure 9-64 shows the TWI-bus timing requirements and the compliance of the device with them. Some of these requirements (t_r and t_f) are met by the device without requiring user intervention. Compliance with the other requirements (t_{HD-STA}, t_{SU-STA}, t_{SU-STO}, t_{HD-DAT}, $t_{SU-DAT-TWI}$, $t_{LOW-TWI}$, t_{HIGH}, and f_{TWCK}) requires user intervention through appropriate programming of the relevant TWIM and TWIS user interface registers. refer to the TWIM and TWIS sections for more information.

Table 9-64. TWI-Bus Timing Requirements

Symbol	Parameter	Mode	Minimum		Maximum		Unit
			Requirement	Device	Requirement	Device	
t_r	TWCK and TWD rise time	Standard(1)	-		1000		ns
		Fast(1)	$20 + 0.1C_b$		300		
t_f	TWCK and TWD fall time	Standard	-		300		ns
		Fast	$20 + 0.1C_b$		300		
t_{HD-STA}	(Repeated) START hold time	Standard	4	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STA}	(Repeated) START set-up time	Standard	4.7	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STO}	STOP set-up time	Standard	4.0	$4t_{clkpb}$	-		µs
		Fast	0.6				
t_{HD-DAT}	Data hold time	Standard	0.3(2)	$2t_{clkpb}$	3.45()	$15t_{prescaled} + t_{clkpb}$	µs
		Fast			0.9()		
$t_{SU-DAT-TWI}$	Data set-up time	Standard	250	$2t_{clkpb}$	-		ns
		Fast	100				
t_{SU-DAT}		-	-	t_{clkpb}	-		-
$t_{LOW-TWI}$	TWCK LOW period	Standard	4.7	$4t_{clkpb}$	-		µs
		Fast	1.3				
t_{LOW}		-	-	t_{clkpb}	-		-
t_{HIGH}	TWCK HIGH period	Standard	4.0	$8t_{clkpb}$	-		µs
		Fast	0.6				
f_{TWCK}	TWCK frequency	Standard	-		100	$\frac{1}{12t_{clkpb}}$	kHz
		Fast			400		

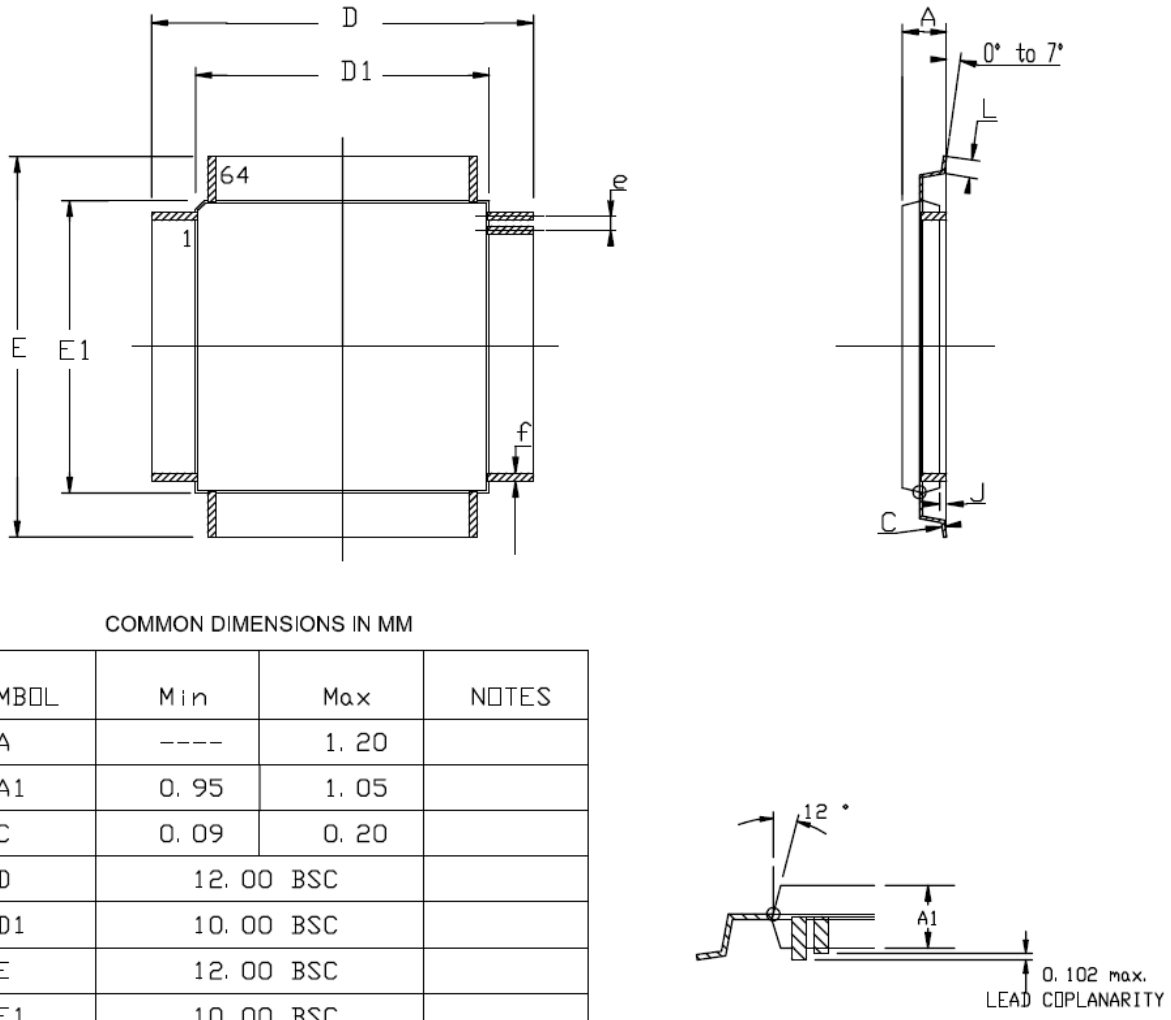
Notes: 1. Standard mode: $f_{TWCK} \leq 100$ kHz ; fast mode: $f_{TWCK} > 100$ kHz .

Table 9-66. SWD Timings[1]

Symbol	Parameter	Conditions	Min	Max	Units
Thigh	SWDCLK High period	V_{VDDIO} from 3.0 V to 3.6 V, maximum external capacitor = 40 pF	10	500 000	ns
Tlow	SWDCLK Low period		10	500 000	
Tos	SWDIO output skew to falling edge SWDCLK		-5	5	
Tis	Input Setup time required between SWDIO		4	-	
Tih	Input Hold time required between SWDIO and rising edge SWDCLK		1	-	

Note: 1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Figure 10-7. TQFP-64 Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

Table 10-20. Device and Package Maximum Weight

300	mg

Table 10-21. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-22. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

11. Ordering Information

Table 11-1. ATSAM4LC8 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LC8CA-AU	512	64	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LC8CA-AUR				Reel		
ATSAM4LC8CA-CFU			VFBGA100	Tray		
ATSAM4LC8CA-CFUR				Reel		
ATSAM4LC8BA-AU			TQFP64	Tray		
ATSAM4LC8BA-AUR				Reel		
ATSAM4LC8BA-MU			QFN64	Tray		
ATSAM4LC8BA-MUR				Reel		
ATSAM4LC8BA-UUR			WLCSP64	Reel		
ATSAM4LC8AA-MU			QFN48	Tray		
ATSAM4LC8AA-MUR				Reel		

Table 11-2. ATSAM4LC4 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LC4CA-AU-ES	256	32	TQFP100	ES	Green	N/A
ATSAM4LC4CA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LC4CA-AUR				Reel		
ATSAM4LC4CA-CFU			VFBGA100	Tray		Industrial -40°C to 85°C
ATSAM4LC4CA-CFUR				Reel		
ATSAM4LC4BA-AU-ES			TQFP64	ES		N/A
ATSAM4LC4BA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LC4BA-AUR				Reel		
ATSAM4LC4BA-MU-ES			QFN64	ES		N/A
ATSAM4LC4BA-MU				Tray		Industrial -40°C to 85°C
ATSAM4LC4BA-MUR				Reel		
ATSAM4LC4BA-UUR			WLCSP64	Reel		Industrial -40°C to 85°C
ATSAM4LC4AA-AU-ES			TQFP48	ES		N/A
ATSAM4LC4AA-AU				Tray		Industrial -40°C to 85°C
ATSAM4LC4AA-AUR				Reel		
ATSAM4LC4AA-MU-ES			QFN48	ES		N/A
ATSAM4LC4AA-MU				Tray		Industrial -40°C to 85°C
ATSAM4LC4AA-MUR				Reel		

Fix/Workaround
Read the last received data, then perform a software reset by writing a one to the Software Reset bit in the Control Register (CR.SWRST).

Disabling SPI has no effect on the SR.TDRE bit
Disabling SPI has no effect on the SR.TDRE bit whereas the write data command is filtered when SPI is disabled. Writing to TDR when SPI is disabled will not clear SR.TDRE. If SPI is disabled during a PDCA transfer, the PDCA will continue to write data to TDR until its buffer is empty, and this data will be lost.
Fix/Workaround
Disable the PDCA, add two NOPs, and disable the SPI. To continue the transfer, enable the SPI and PDCA.

SPI bad serial clock generation on 2nd chip_select when SCBR=1, CPOL=1, and NCPHA=0
When multiple chip selects (CS) are in use, if one of the baudrates equal 1 while one (CSRn.SCBR=1) of the others do not equal 1, and CSRn.CPOL=1 and CSRn.NCPHA=0, then an additional pulse will be generated on SCK.
Fix/Workaround
When multiple CS are in use, if one of the baudrates equals 1, the others must also equal 1 if CSRn.CPOL=1 and CSRn.NCPHA=0.

12.1.5 TC

Channel chaining skips first pulse for upper channel
When chaining two channels using the Block Mode Register, the first pulse of the clock between the channels is skipped.
Fix/Workaround
Configure the lower channel with RA = 0x1 and RC = 0x2 to produce a dummy clock cycle for the upper channel. After the dummy cycle has been generated, indicated by the SR.CPCS bit, reconfigure the RA and RC registers for the lower channel with the real values.

12.1.6 USBC

In USB host mode, entering suspend mode for low speed device can fail when the USB freeze (USBCON.FRZCLK=1) is done just after UHCON.SOFE=0.
Fix/Workaround
When entering suspend mode (UHCON.SOFE is cleared), check that USBFSM.DRDSTATE is not equal to three before freezing the clock (USBCON.FRZCLK=1).

In USB host mode, the asynchronous attach detection (UDINT.HWUPI) can fail when the USB clock freeze (USBCON.FRZCLK=1) is done just after setting the USB-STA.VBUSRQ bit.
Fix/Workaround
After setting USBSTA.VBUSRQ bit, wait until the USBFSM register value is ‘A_WAIT_BCON’ before setting the USBCON.FRZCLK bit.