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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 7x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls8ba-au

Figure 3-4. ATSAM4LC TQFP64/QFN64 Pinout

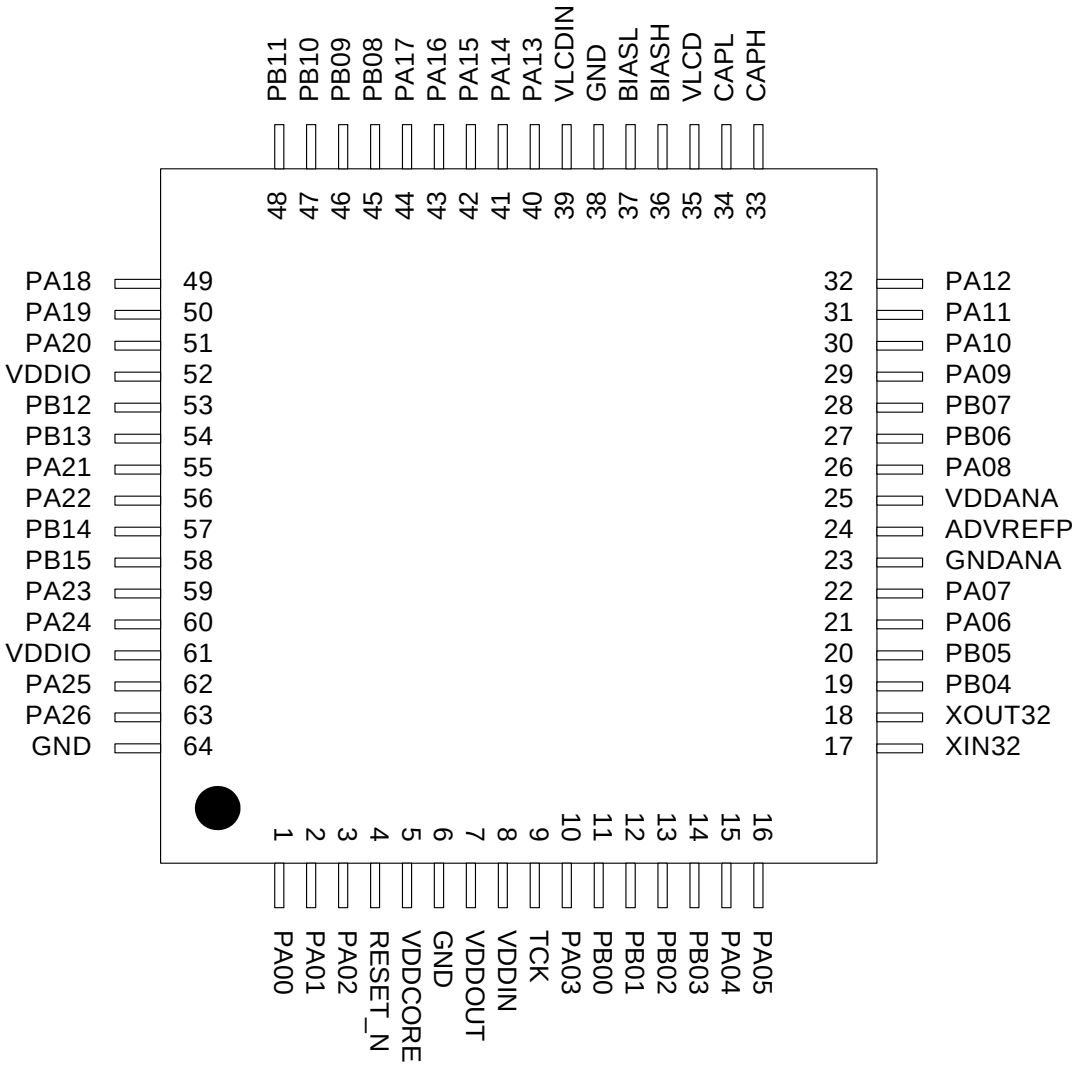


Figure 3-8. ATSAM4LS WLCSP64 Pinout

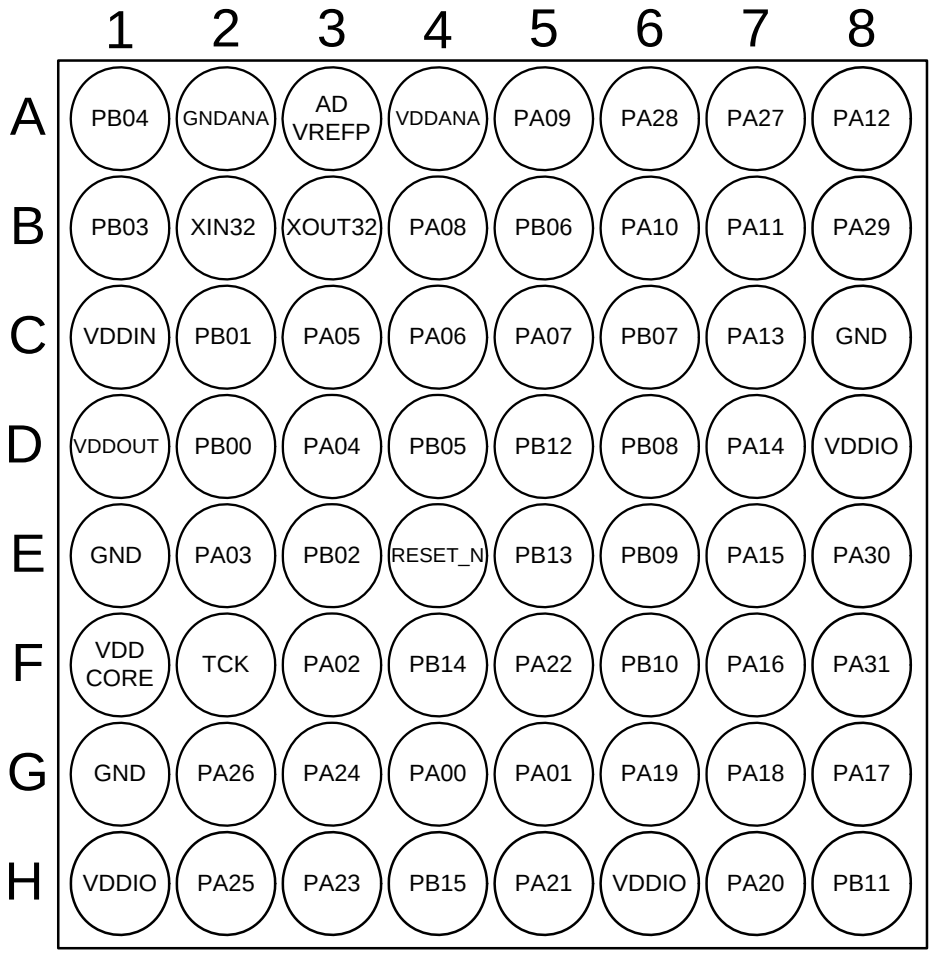


Table 3-2. 64-pin GPIO Controller Function Multiplexing (Sheet 2 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
QFP QFN	QFP QFN				A	B	C	D	E	F	G
15	15	PA04	4	VDDANA	ADCIFE AD0	USART0 CLK	EIC EXTINT2	GLOC IN1			CATB SENSE0
16	16	PA05	5	VDDANA	ADCIFE AD1	USART0 RXD	EIC EXTINT3	GLOC IN2	ADCIFE TRIGGER		CATB SENSE1
21	21	PA06	6	VDDANA	DACC VOUT	USART0 RTS	EIC EXTINT1	GLOC IN0	ACIFC ACAN0		CATB SENSE2
22	22	PA07	7	VDDANA	ADCIFE AD2	USART0 TXD	EIC EXTINT4	GLOC IN3	ACIFC ACAP0		CATB SENSE3
26	26	PA08	8	LCDA	USART0 RTS	TC0 A0	PEVC PAD EVT0	GLOC OUT0		LCDCA SEG23	CATB SENSE4
29	29	PA09	9	LCDA	USART0 CTS	TC0 B0	PEVC PAD EVT1	PARC PCDATA0		LCDCA COM3	CATB SENSE5
30	30	PA10	10	LCDA	USART0 CLK	TC0 A1	PEVC PAD EVT2	PARC PCDATA1		LCDCA COM2	CATB SENSE6
31	31	PA11	11	LCDA	USART0 RXD	TC0 B1	PEVC PAD EVT3	PARC PCDATA2		LCDCA COM1	CATB SENSE7
32	32	PA12	12	LCDA	USART0 TXD	TC0 A2		PARC PCDATA3		LCDCA COM0	CATB DIS
40	40	PA13	13	LCDA	USART1 RTS	TC0 B2	SPI NPCS1	PARC PCDATA4		LCDCA SEG5	CATB SENSE8
41	41	PA14	14	LCDA	USART1 CLK	TC0 CLK0	SPI NPCS2	PARC PCDATA5		LCDCA SEG6	CATB SENSE9
42	42	PA15	15	LCDA	USART1 RXD	TC0 CLK1	SPI NPCS3	PARC PCDATA6		LCDCA SEG7	CATB SENSE10
43	43	PA16	16	LCDA	USART1 TXD	TC0 CLK2	EIC EXTINT1	PARC PCDATA7		LCDCA SEG8	CATB SENSE11
44	44	PA17	17	LCDA	USART2 RTS	ABDACB DAC0	EIC EXTINT2	PARC PCCK		LCDCA SEG9	CATB SENSE12
49	49	PA18	18	LCDA	USART2 CLK	ABDACB DACN0	EIC EXTINT3	PARC PCEN1		LCDCA SEG18	CATB SENSE13
50	50	PA19	19	LCDA	USART2 RXD	ABDACB DAC1	EIC EXTINT4	PARC PCEN2	SCIF GCLK0	LCDCA SEG19	CATB SENSE14
51	51	PA20	20	LCDA	USART2 TXD	ABDACB DACN1	EIC EXTINT5	GLOC IN0	SCIF GCLK1	LCDCA SEG20	CATB SENSE15
55	55	PA21	21	LCDC	SPI MISO	USART1 CTS	EIC EXTINT6	GLOC IN1	TWIM2 TWD	LCDCA SEG34	CATB SENSE16
56	56	PA22	22	LCDC	SPI MOSI	USART2 CTS	EIC EXTINT7	GLOC IN2	TWIM2 TWCK	LCDCA SEG35	CATB SENSE17
59	59	PA23	23	LCDC	SPI SCK	TWIMS0 TWD	EIC EXTINT8	GLOC IN3	SCIF GCLK IN0	LCDCA SEG38	CATB DIS
60	60	PA24	24	LCDC	SPI NPCS0	TWIMS0 TWCK		GLOC OUT0	SCIF GCLK IN1	LCDCA SEG39	CATB SENSE18
62	62	PA25	25	VDDIO	USBC DM	USART2 RXD					CATB SENSE19
63	63	PA26	26	VDDIO	USBC DP	USART2 TXD					CATB SENSE20

Table 4-2. Interrupt Request Signal Map (Sheet 3 of 3)

Line	Module	Signal
48	External Interrupt Controller	EIC 4
49	External Interrupt Controller	EIC 5
50	External Interrupt Controller	EIC 6
51	External Interrupt Controller	EIC 7
52	External Interrupt Controller	EIC 8
53	Inter-IC Sound (I2S) Controller	IISC
54	Serial Peripheral Interface	SPI
55	Timer/Counter	TC00
56	Timer/Counter	TC01
57	Timer/Counter	TC02
58	Timer/Counter	TC10
59	Timer/Counter	TC11
60	Timer/Counter	TC12
61	Two-wire Master Interface	TWIM0
62	Two-wire Slave Interface	TWIS0
63	Two-wire Master Interface	TWIM1
64	Two-wire Slave Interface	TWIS1
65	Universal Synchronous Asynchronous Receiver Transmitter	USART0
66	Universal Synchronous Asynchronous Receiver Transmitter	USART1
67	Universal Synchronous Asynchronous Receiver Transmitter	USART2
68	Universal Synchronous Asynchronous Receiver Transmitter	USART3
69	ADC controller interface	ADCIFE
70	DAC Controller	DACC
71	Analog Comparator Interface	ACIFC
72	Audio Bitstream DAC	ABDACB
73	True Random Number Generator	TRNG
74	Parallel Capture	PARC
75	Capacitive Touch Module B	CATB
77	Two-wire Master Interface	TWIM2
78	Two-wire Master Interface	TWIM3
79	LCD Controller A	LCDCA

6.2 Power Supplies

The ATSAM4L8/L4/L2 has several types of power supply pins:

- VDDIO: Powers I/O lines, the general purpose oscillator (OSC), the 80MHz integrated RC oscillator (RC80M) . Voltage is 1.68V to 3.6V.
- VLCDIN: (ATSAM4LC only) Powers the LCD voltage pump. Voltage is 1.68V to 3.6V.
- VDDIN: Powers the internal voltage regulator. Voltage is 1.68V to 3.6V.
- VDDANA: Powers the ADC, the DAC, the Analog Comparators, the 32kHz oscillator (OSC32K), the 32kHz integrated RC oscillator (RC32K)and the Brown-out detectors (BOD18 and BOD33). Voltage is 1.68V to 3.6V nominal.
- VDDCORE: Powers the core, memories, peripherals, the PLL, the DFLL, the 4MHz integrated RC oscillator (RCFAST) and the 115kHz integrated RC oscillator (RCSYS).
  - VDDOUT is the output voltage of the regulator and must be connected with or without an inductor to VDDCORE.

The ground pins GND are common to VDDCORE, VDDIO, and VDDIN. The ground pin for VDDANA is GNDANA.

For decoupling recommendations for the different power supplies, refer to the schematic document.

6.2.1 Voltage Regulator

An embedded voltage regulator supplies all the digital logic in the Core and the Backup power domains.

The regulator has two functionnal mode depending of BUCK/LDOn (PA02) pin value. When this pin is low, the regulator is in linear mode and VDDOUT must be connected to VDDCORE externally. When this pin is high, it behaves as a switching regulator and an inductor must be placed between VDDOUT and VDDCORE. The value of this pin is sampled during the power-up phase when the Power On Reset 33 reaches V_{POT+} (Section 9.9 ”Analog Characteristics” on page 129)

Its output voltages in the Core domain (V_{CORE}) and in the Backup domain (V_{BKUP}) are always equal except in Backup mode where the Core domain is not powered (V_{CORE}=0). The Backup domain is always powered. The voltage regulator features three different modes:

- Normal mode: the regulator is configured as linear or switching regulator. It can support all different Run and Sleep modes.
- Low Power (LP) mode: the regulator consumes little static current. It can be used in Wait modes.
- Ultra Low Power (ULP) mode: the regulator consumes very little static current . It is dedicated to Retention and Backup modes. In Backup mode, the regulator only supplies the backup domain.

At power-up or after a reset, the ATSAM4L8/L4/L2 is in the RUN0 mode. Only the necessary clocks are enabled allowing software execution. The Power Manager (PM) can be used to adjust the clock frequencies and to enable and disable the peripheral clocks.

When the CPU is entering a Power Save Mode, the CPU stops executing code. The user can choose between four Power Save Modes to optimize power consumption:

- SLEEP mode: the Cortex-M4 core is stopped, optionally some clocks are stopped, peripherals are kept running if enabled by the user.
- WAIT mode: all clock sources are stopped, the core and all the peripherals are stopped except the modules running with the 32kHz clock if enabled. This is the lowest power configuration where SleepWalking is supported.
- RETENTION mode: similar to the WAIT mode in terms of clock activity. This is the lowest power configuration where the logic is retained.
- BACKUP mode: the Core domain is powered off, the Backup domain is kept powered.

A wake up source exits the system to the RUN mode from which the Power Save Mode was entered.

A reset source always exits the system from the Power Save Mode to the RUN0 mode.

The configuration of the I/O lines are maintained in all Power Save Modes. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677.

7.1.1 SLEEP mode

The SLEEP mode allows power optimization with the fastest wake up time.

The CPU is stopped. To further reduce power consumption, the user can switch off modules-clocks and synchronous clock sources through the BPM.PMCON.SLEEP field (See Table 7-1). The required modules will be halted regardless of the bit settings of the mask registers in the Power Manager (PM.AHBMASK, PM.APBxMASK).

Table 7-1. SLEEP mode Configuration

BPM.PSAVE.SLEEP	CPU clock	AHB clocks	APB clocks GCLK	Clock sources: OSC, RCFAST, RC80M, PLL, DFLL	RCSYS	OSC32K RC32K(2)	Wake up Sources
0	Stop	Run	Run	Run	Run	Run	Any interrupt
1	Stop	Stop	Run	Run	Run	Run	Any interrupt(1)
2	Stop	Stop	Stop	Run	Run	Run	Any interrupt(1)
3	Stop	Stop	Stop	Stop	Run	Run	Any interrupt(1)

Notes: 1. from modules with clock running.
2. OSC32K and RC32K will only remain operational if pre-enabled.

7.1.1.1 Entering SLEEP mode

The SLEEP mode is entered by executing the WFI instruction.

Additionally, if the SLEEPONEXIT bit in the Cortex-M4 System Control Register (SCR) is set, the SLEEP mode will also be entered when the Cortex-M4 exits the lowest priority ISR. This

7.1.5 Power Save Mode Summary Table

The following table shows a summary of the main Power Save modes:

Table 7-2. Power Save mode Configuration Summary

Mode	Mode Entry	Wake up sources	Core domain	Backup domain
SLEEP	WFI SCR.SLEEPDEEP bit = 0 BPM.PMCON.BKUP bit = 0	Any interrupt	CPU clock OFF Other clocks OFF depending on the BPM.PMCON.SLEEP field see "SLEEP mode" on page 56	Clocks OFF depending on the BPM.PMCON.SLEEP field see "SLEEP mode" on page 56
WAIT	WFI SCR.SLEEPDEEP bit = 1 BPM.PMCON.RET bit = 0 BPM.PMCON.BKUP bit = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running
RETENTION	WFI SCR.SLEEPDEEP bit = 1 BPM.PMCON.RET bit = 1 BPM.PMCON.BKUP bit = 0	PM WAKE interrupt	All clocks are OFF Core domain is retained	All clocks are OFF except RC32K or OSC32K if running
BACKUP	WFI + SCR.SLEEPDEEP bit = 1 + BPM.PMCON.BKUP bit = 1	EIC interrupt BOD33, BOD18 interrupt and reset AST alarm, periodic, overflow WDT interrupt and reset external reset on RESET_N pin	OFF (not powered)	All clocks are OFF except RC32K or OSC32K if running

7.2 Power Scaling

The Power Scaling technique consists of adjusting the internal regulator output voltage (voltage scaling) to reduce the power consumption. According to the requirements in terms of performance, operating modes, and current consumption, the user can select the Power Scaling configuration that fits the best with its application.

The Power Scaling configuration field (PMCON.PS) is provided in the Backup Power Manager (BPM) module.

In RUN mode, the user can adjust on the fly the Power Scaling configuration

The Figure 7.1 summarizes the different combination of the Power Scaling configuration which can be applied according to the Power Save Mode.

Power scaling from a current power configuration to a new power configuration is done by halting the CPU execution

Power scaling occurs after a WFI instruction. The system is halted until the new power configuration is stabilized. After handling the PM interrupt, the system resumes from WFI.

To scale the power, the following sequence is required:

- Check the BPM.SR.PSOK bit to make sure the current power configuration is stabilized.

The FPB unit contains:

- Two literal comparators for matching against literal loads from Code space, and remapping to a corresponding area in System space.
- Six instruction comparators for matching against instruction fetches from Code space and remapping to a corresponding area in System space.
- Alternatively, comparators can also be configured to generate a Breakpoint instruction to the processor core on a match.

8.6.2 DWT (Data Watchpoint and Trace)

The DWT contains four comparators which can be configured to generate the following:

- PC sampling packets at set intervals
- PC or Data watchpoint packets
- Watchpoint event to halt core

The DWT contains counters for the items that follow:

- Clock cycle (CYCCNT)
- Folded instructions
- Load Store Unit (LSU) operations
- Sleep Cycles
- CPI (all instruction cycles except for the first cycle)
- Interrupt overhead

8.6.3 ITM (Instrumentation Trace Macrocell)

The ITM is an application driven trace source that supports printf style debugging to trace Operating System (OS) and application events, and emits diagnostic system information. The ITM emits trace information as packets which can be generated by three different sources with several priority levels:

- **Software trace**: This can be done thanks to the printf style debugging. For more information, refer to Section "How to Configure the ITM:".
- **Hardware trace**: The ITM emits packets generated by the DWT.
- **Time stamping**: Timestamps are emitted relative to packets. The ITM contains a 21-bit counter to generate the timestamp.

How to Configure the ITM:

The following example describes how to output trace data in asynchronous trace mode.

- Configure the TPIU for asynchronous trace mode (refer to Section "5.4.3. How to Configure the TPIU")
- Enable the write accesses into the ITM registers by writing "0xC5ACCE55" into the Lock Access Register (Address: 0xE0000FB0)
- Write 0x00010015 into the Trace Control Register:
  - Enable ITM
  - Enable Synchronization packets
  - Enable SWO behavior

8.7.5 Product Dependencies

8.7.5.1 I/O Lines

The TCK pin is dedicated to the EDP. The other debug port pins default after reset to their GPIO functionality and are automatically reassigned to the JTAG functionalities on detection of a debugger. In serial wire mode, TDI and TDO can be used as GPIO functions. Note that in serial wire mode TDO can be used as a single pin trace output.

8.7.5.2 Power Management

When a debugger is present, the connection is kept alive allowing debug operations. As a side effect, the power is never turned off. The hot plugging functionality is always available except when the system is in BACKUP Power Save Mode.

8.7.5.3 Clocks

The SWJ-DP uses the external TCK pin as its clock source. This clock must be provided by the external JTAG master device.

Some of the JTAG Instructions are used to access an Access Port (SMAP or AHB-AP). These instructions require the CPU clock to be running.

If the CPU clock is not present because the CPU is in a Power Save Mode where this clock is not provided, the Power Manager(PM) will automatically restore the CPU clock on detection of a debug access.

The RCSYS clock is used as CPU clock when the external reset is applied to ensure correct Access Port operations.

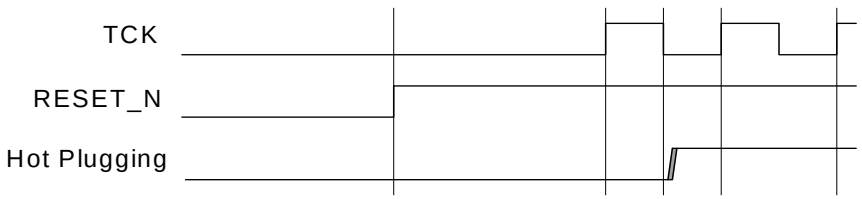
8.7.6 Module Initialization

This module is enabled as soon as a TCK falling edge is detected when RESET_N is not asserted (refer to Section 8.7.7 below). Moreover, the module is synchronously reseted as long as the TAP machine is in the TEST_LOGIC_RESET (TLR) state. It is advised asserting TMS at least 5 TCK clock periods after the debugger has been detected to ensure the module is in the TLR state prior to any operation. This module also has the ability to maintain the Cortex-M4 under reset (refer to the Section 8.7.8 ”SMAP Core Reset Request Source” on page 70).

8.7.7 Debugger Hot Plugging

The TCK pin is dedicated to the EDP. After reset has been released, the EDP detects that a debugger has been attached when a TCK falling edge arises.

Figure 8-4. Debugger Hot Plugging Detection Timings Diagram



8.7.10 SW-DP and JTAG-DP Selection Mechanism

After reset, the SWJ-DP is in JTAG mode but it can be switched to the Serial Wire mode. Debug port selection mechanism is done by sending specific **SWDIOTMS** sequence. The JTAG-DP is selected by default after reset.

- Switch from JTAG-DP to SW-DP. The sequence is:
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
  - Send the 16-bit sequence on **SWDIOTMS** = 0111100111100111 (0x79E7 MSB first)
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
- Switch from SWD to JTAG. The sequence is:
  - Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1
  - Send the 16-bit sequence on **SWDIOTMS** = 0011110011100111 (0x3CE7 MSB first)

Send more than 50 **SWCLKTCK** cycles with **SWDIOTMS** = 1

Note that the BSCAN-TAP is not available when the debug port is switched to Serial Mode. Boundary scan instructions are not available.

8.7.11 JTAG-DP and BSCAN-TAP Selection Mechanism

After the DP has been enabled, the BSCAN-TAP and the JTAG-DP run simultaneously has long as the SWJ-DP remains in JTAG mode. Each TAP captures simultaneously the JTAG instructions that are shifted. If an instruction is recognized by the BSCAN-TAP, then the BSCAN-TAP TDO is selected instead of the SWJ-DP TDO. TDO selection changes dynamically depending on the current instruction held in the BSCAN-TAP instruction register.

8.7.14.4 CLAMP

This instruction selects the Bypass register as Data Register. The device output pins are driven from the boundary-scan chain.

Starting in Run-Test/Idle, the CLAMP instruction is accessed the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. In Update-IR: The data from the boundary-scan chain is applied to the output pins.
5. Return to Run-Test/Idle.
6. Select the DR Scan path.
7. In Capture-DR: A logic ‘0’ is loaded into the Bypass Register.
8. In Shift-DR: Data is scanned from TDI to TDO through the Bypass register.
9. Return to Run-Test/Idle.

Table 8-8. CLAMP Details

Instructions	Details
IR input value	**0101** (0x5)
IR output value	p00s
DR Size	1
DR input value	x
DR output value	x

8.9.11.6 Data Register

Name: DATA

Access Type: Read/Write

Offset: 0x14

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
DATA							

23	22	21	20	19	18	17	16
DATA							

15	14	13	12	11	10	9	8
DATA							

7	6	5	4	3	2	1	0
DATA							

- **DATA: Generic data register**

8.11.8 Chip erase typical procedure

The chip erase operation is triggered by writing a one in the CE bit in the Control Register (CR.CE). This clears first all volatile memories in the system and second the whole flash array. Note that the User page is not erased in this process. To ensure that the chip erase operation is completed, check the DONE bit in the Status Register (SR.DONE). Also note that the chip erase operation depends on clocks and power management features that can be altered by the CPU. It is important to ensure that it is stopped. The recommended sequence is shown below:

1. At power up, RESET_N is driven low by a debugger. The on-chip regulator holds the system in a POR state until the input supply is above the POR threshold. The system continues to be held in this static state until the internally regulated supplies have reached a safe operating.
2. PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock, and any Bus Clocks that do not have clock gate control). Internal resets are maintained due to the external reset.
   – The debug port and access ports receives a clock and leave the reset state
3. The debugger maintains a low level on TCK and release RESET_N.
   – The SMAP asserts the core_hold_reset signal
4. The Cortex-M4 core remains in reset state, meanwhile the rest of the system is released.
5. The Chip erase operation can be performed by issuing the SMAP Chip Erase command. In this case:
   – volatile memories are cleared first
   – followed by the clearing of the flash array
   – followed by the clearing of the protected state
6. After operation is completed, the chip must be restarted by either controling RESET_N or switching power off/on. Make sure that the TCK pin is high when releasing RESET_N not to halt the core.

8.11.9 Setting the protected state

This is done by issuing a specific flash controller command, for more information, refer to the Flash Controller chapter and to section 8.11.7Flash Programming typical procedure97. The protected state is defined by a highly secure Flash builtin mechanism. Note that for this programmation to propagate, it is required to reset the chip.

Table 9-20. High Drive TWI Pin Characteristics in GPIO configuration (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-up resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	
V_{OL}	Output low-level voltage					0.4	
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			3.4	mA
			2.7V<V_{VDD}<3.6V			6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			5.2	mA
			2.7V<V_{VDD}<3.6V			8	
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			3.4	mA
			2.7V<V_{VDD}<3.6V			6	
		ODCR0=1	1.68V<V_{VDD}<2.7V			5.2	mA
			2.7V<V_{VDD}<3.6V			8	
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		18		ns
		OSRR0=1			110		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		10		ns
		OSRR0=1			50		
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, Cload = 25pF		19		ns
		OSRR0=1			140		
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, Cload = 25pF		12		ns
		OSRR0=1			63		

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization
3. These values are based on characterization. These values are not covered by test limits in production

Table 9-21. Common High Drive TWI Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LEAK}	Input leakage current (1)	Pull-up resistors disabled		0.01	2	µA
C_{IN}	Input capacitance(1)			10		pF

1. These values are based on simulation. These values are not covered by test limits in production or characterization

9.7.2 32kHz Crystal Oscillator (OSC32K) Characteristics

Figure 9-3 and the equation above also applies to the 32kHz oscillator connection. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can then be found in the crystal datasheet.

Table 9-24. Digital Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$f_{CPXIN32}$	XIN32 clock frequency (1)				6	MHz
	XIN32 clock duty cycle(1)		40		60	%
$t_{STARTUP}$	Startup time			N/A		cycles

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-25. 32 kHz Crystal Oscillator Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{OUT}	Crystal oscillator frequency				32 768		Hz
$t_{STARTUP}$	Startup time (1)	R_m = 100kΩ, C_L = 12.5pF			30000(2)		cycles
C_L	Crystal load capacitance(1)			6		12.5	pF
C_{SHUNT}	Crystal shunt capacitance(1)			0.8		1.7	
C_{XIN}	Parasitic capacitor load (3)	TQFP100 package			3.4		
C_{XOUT}	Parasitic capacitor load(3)				2.72		
I_{OSC32K}	Current consumption(1)				350		nA
ESR_{XTAL}	Crystal equivalent series resistance(1) f=32.768kHz OSCCTRL32.MODE=1 Safety Factor = 3	OSCCTRL32.SELCURR=0	C_L=6pF			28	kΩ
		OSCCTRL32.SELCURR=4				72	
		OSCCTRL32.SELCURR=8				114	
		OSCCTRL32.SELCURR=15				313	
		OSCCTRL32.SELCURR=0	C_L=9pF			14	kΩ
		OSCCTRL32.SELCURR=4				36	
		OSCCTRL32.SELCURR=8				100	
		OSCCTRL32.SELCURR=15				170	
	Crystal equivalent series resistance(3) f=32.768kHz OSCCTRL32.MODE=1 Safety Factor = 3	OSCCTRL32.SELCURR=4	C_L=12.5pF			15.2	kΩ
		OSCCTRL32.SELCURR=6				61.8	
		OSCCTRL32.SELCURR=8				101.8	
		OSCCTRL32.SELCURR=10				138.5	
		OSCCTRL32.SELCURR=15				228.5	

1. These values are based on simulation. These values are not covered by test limits in production or characterization.
2. Nominal crystal cycles.
3. These values are based on characterization. These values are not covered by test limits in production.

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

The values in Table 9-43 describe the values of the BOD33.LEVEL in the flash User Page fuses.

Table 9-43. BOD33.LEVEL Values

BOD33.LEVEL Value	Min	Typ	Max	Units
16		2.08		V
20		2.18		
24		2.33		
28		2.48		
32		2.62		
36		2.77		
40		2.92		
44		3.06		
48		3.21		

Table 9-44. BOD33 Characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Step size, between adjacent values in BSCIF.BOD33LEVEL(1)			34.4		mV
V_{HYST}	Hysteresis(1)		45		170	
t_{DET}	Detection time(1)	Time with VDDIN < V_{TH} necessary to generate a reset signal				µs
I_{BOD33}	Current consumption(1)	Normal mode			36	µA
$t_{STARTUP}$	Startup time(1)	Normal mode			6	µs

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

Maximum SPI Frequency, Master Output

The maximum SPI master output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn}, \frac{f_{CLKSPI} \times 2}{9})$$

Where $SPIn$ is the MOSI delay, USPI2 or USPI5 depending on CPOL and NCPHA. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Master Input

The maximum SPI master input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{1}{SPIn + t_{VALID}}, \frac{f_{CLKSPI} \times 2}{9})$$

Where $SPIn$ is the MISO setup and hold time, USPI0 + USPI1 or USPI3 + USPI4 depending on CPOL and NCPHA. T_{VALID} is the SPI slave response time. refer to the SPI slave datasheet for $T_{VALID} \cdot f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

9.10.2.2 Slave mode

Figure 9-9. USART in SPI Slave Mode with (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

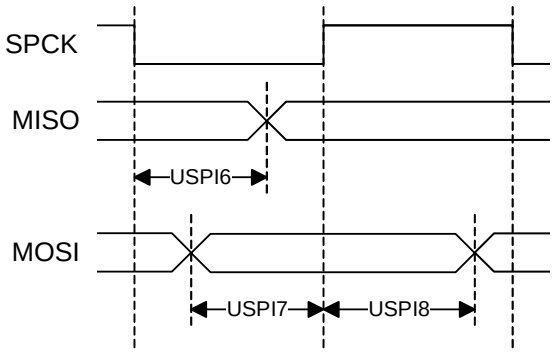


Table 9-61. USART3 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		593.9	ns
USPI7	MOSI setup time before SPCK rises		45.93 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		47.03 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			593.38	
USPI10	MOSI setup time before SPCK falls		45.93 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		47.03 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		237.5		
USPI13	NSS hold time after SPCK falls		-1.81		
USPI14	NSS setup time before SPCK falls		237.5		
USPI15	NSS hold time after SPCK rises		-1.81		

Notes: 1. These values are based on simulation. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left(\left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor + \frac{1}{2}\right) \times t_{CLKUSART}$

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, USPI7 + USPI8 or USPI10 + USPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

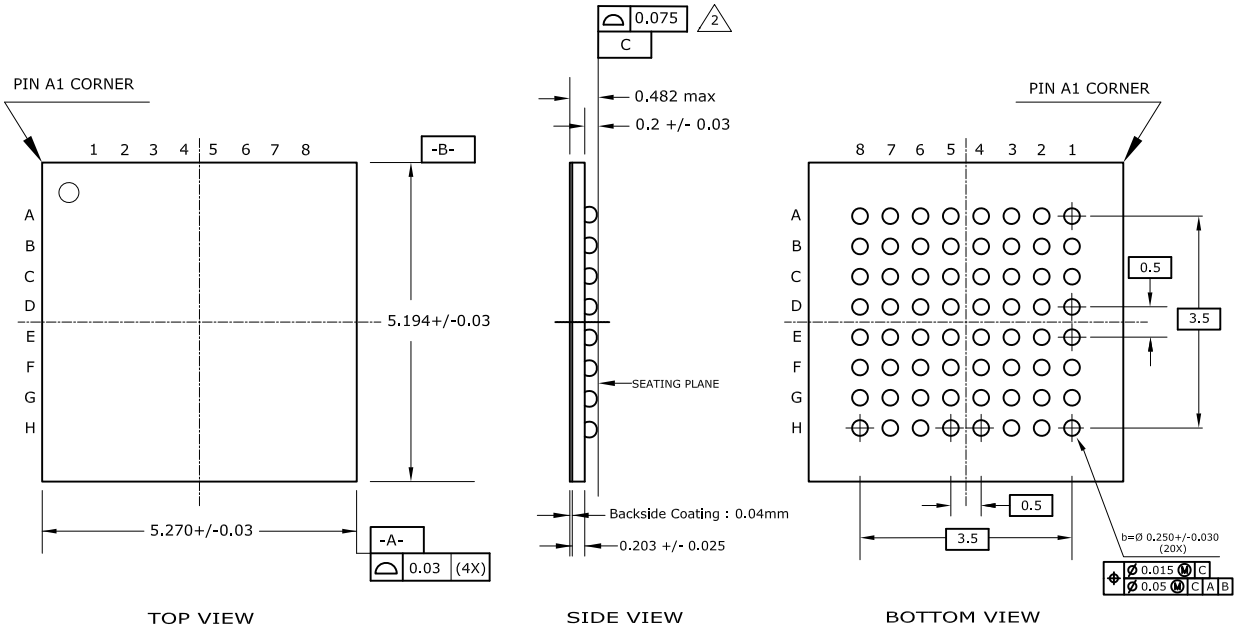
Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

Where $SPIn$ is the MISO delay, USPI6 or USPI9 depending on CPOL and NCPHA. T_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for T_{SETUP} . f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

Figure 10-5. WLCSP64 SAM4LC8 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.75	1.75
A2	GNDANA	1.75	1.25
A3	ADVREFP	1.75	0.75
A4	VDDANA	1.75	0.25
A5	PA09	1.75	-0.25
A6	CAPL	1.75	-0.75
A7	CAPH	1.75	-1.25
A8	PA12	1.75	-1.75
B1	PB03	1.25	1.75
B2	XIN32	1.25	1.25
B3	XOUT32	1.25	0.75
B4	PA08	1.25	0.25
B5	PB06	1.25	-0.25
B6	PA10	1.25	-0.75
B7	PA11	1.25	-1.25
B8	VLCD	1.25	-1.75
C1	VDDIN	0.75	1.75
C2	PB01	0.75	1.25
C3	PA05	0.75	0.75
C4	PA06	0.75	0.25
C5	PA07	0.75	-0.25
C6	PB07	0.75	-0.75

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	0.75	-1.25
C8	BIAS1	0.75	-1.75
D1	VDDOUT	0.25	1.75
D2	PB00	0.25	1.25
D3	PA04	0.25	0.75
D4	PB05	0.25	0.25
D5	PB12	0.25	-0.25
D6	PB08	0.25	-0.75
D7	PA14	0.25	-1.25
D8	BIAS2	0.25	-1.75
E1	GNDIN	-0.25	1.75
E2	PA03	-0.25	1.25
E3	PB02	-0.25	0.75
E4	RESET_N	-0.25	0.25
E5	PB13	-0.25	-0.25
E6	PB09	-0.25	-0.75
E7	PA15	-0.25	-1.25
E8	GNDIO0	-0.25	-1.75
F1	VDDCORE	-0.75	1.75
F2	TCK	-0.75	1.25
F3	PA02	-0.75	0.75
F4	PB14	-0.75	0.25

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.75	-0.25
F6	PB10	-0.75	-0.75
F7	PA16	-0.75	-1.25
F8	VLCDIN	-0.75	-1.75
G1	GNDIO1	-1.25	1.75
G2	PA26	-1.25	1.25
G3	PA24	-1.25	0.75
G4	PA00	-1.25	0.25
G5	PA01	-1.25	-0.25
G6	PA19	-1.25	-0.75
G7	PA18	-1.25	-1.25
G8	PA17	-1.25	-1.75
H1	VDDIO1	-1.75	1.75
H2	PA25	-1.75	1.25
H3	PA23	-1.75	0.75
H4	PB15	-1.75	0.25
H5	PA21	-1.75	-0.25
H6	VDDIO0	-1.75	-0.75
H7	PA20	-1.75	-1.25
H8	PB11	-1.75	-1.75

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-14. Device and Package Maximum Weight

14.8	mg

Table 10-15. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-16. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

Table 11-3. ATSAM4LC2 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LC2CA-AU	128	32	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LC2CA-AUR				Reel		
ATSAM4LC2CA-CFU			VFBGA100	Tray		
ATSAM4LC2CA-CFUR				Reel		
ATSAM4LC2BA-AU			TQFP64	Tray		
ATSAM4LC2BA-AUR				Reel		
ATSAM4LC2BA-MU			QFN64	Tray		
ATSAM4LC2BA-MUR				Reel		
ATSAM4LC2BA-UUR			WLCSP64	Reel		
ATSAM4LC2AA-AU			TQFP48	Tray		
ATSAM4LC2AA-AUR				Reel		
ATSAM4LC2AA-MU			QFN48	Tray		
ATSAM4LC2AA-MUR				Reel		

Table 11-4. ATSAM4LS8 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LS8CA-AU	512	64	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS8CA-AUR				Reel		
ATSAM4LS8CA-CFU			VFBGA100	Tray		
ATSAM4LS8CA-CFUR				Reel		
ATSAM4LS8BA-AU			TQFP64	Tray		
ATSAM4LS8BA-AUR				Reel		
ATSAM4LS8BA-MU			QFN64	Tray		
ATSAM4LS8BA-MUR				Reel		
ATSAM4LS8BA-UUR			WLCSP64	Reel		
ATSAM4LS8AA-MU			QFN48	Tray		
ATSAM4LS8AA-MUR				Reel		