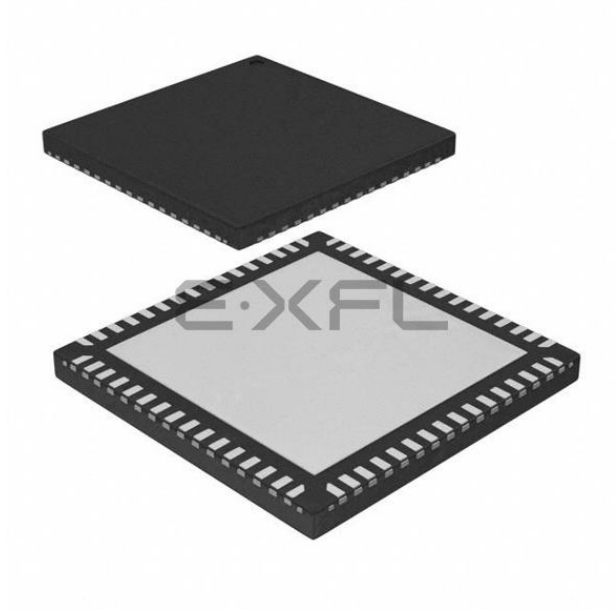

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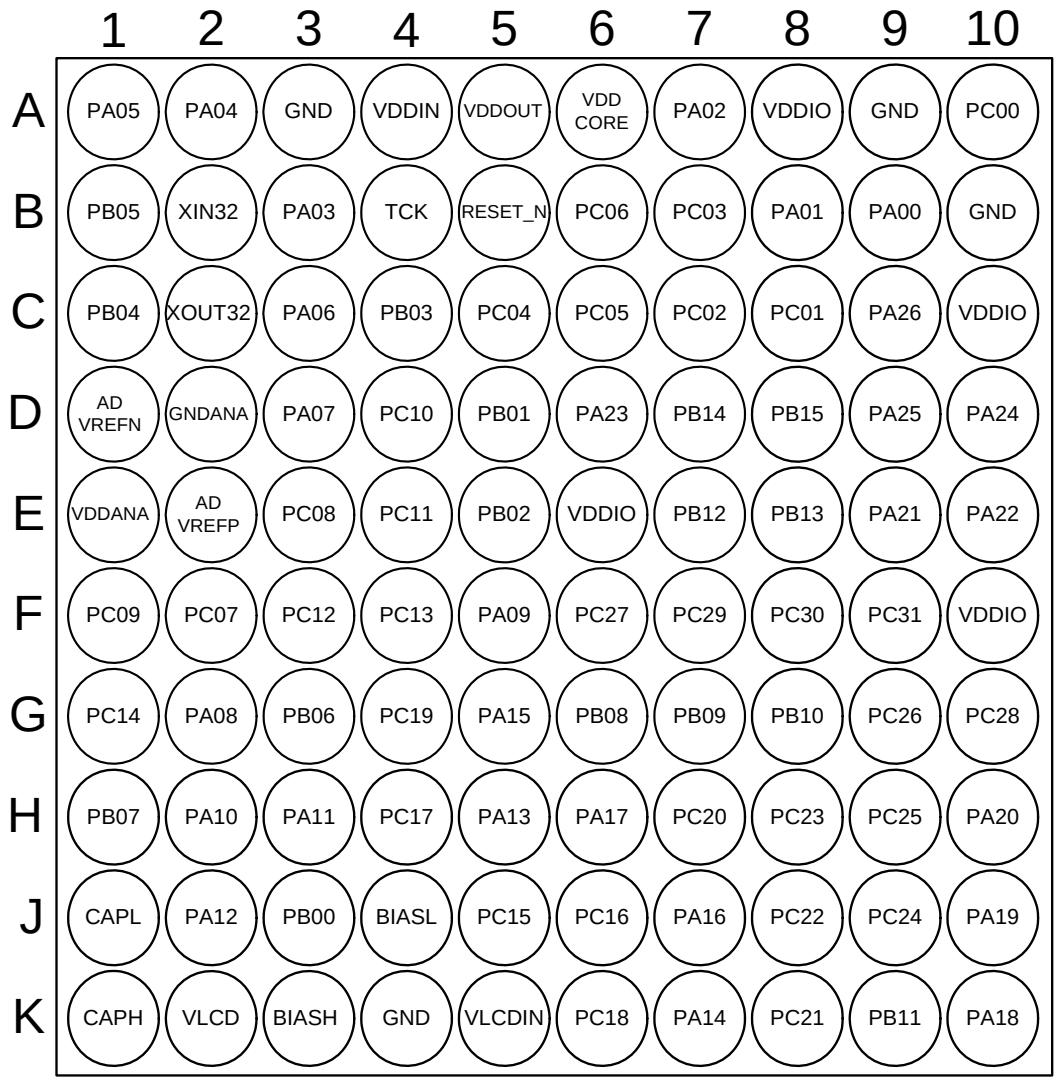
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	48
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 7x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls8ba-mu

Figure 3-2. ATSAM4LC VFBGA100 Pinout



3.2 Peripheral Multiplexing on I/O lines

3.2.1 Multiplexed Signals

Each GPIO line can be assigned to one of the peripheral functions. The following tables (Section 3-1 ”100-pin GPIO Controller Function Multiplexing” on page 19 to Section 3-4 ”48-pin GPIO Controller Function Multiplexing” on page 28) describes the peripheral signals multiplexed to the GPIO lines.

Peripheral functions that are not relevant in some parts of the family are grey-shaded.

For description of differents Supply voltage source, refer to the Section 6. ”Power and Startup Considerations” on page 46.

Table 3-1. 100-pin GPIO Controller Function Multiplexing (Sheet 1 of 4)

ATSAM4LC		ATSAM4LS		Pin	GPIO	Supply	GPIO Functions						
QFN	VFBGA	QFN	VFBGA				A	B	C	D	E	F	G
5	B9	5	B9	PA00	0	VDDIO							
6	B8	6	B8	PA01	1	VDDIO							
12	A7	12	A7	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
19	B3	19	B3	PA03	3	VDDIN		SPI MISO					
24	A2	24	A2	PA04	4	VDDANA	ADCIFE AD0	USART0 CLK	EIC EXTINT2	GLOC IN1			CATB SENSE0
25	A1	25	A1	PA05	5	VDDANA	ADCIFE AD1	USART0 RXD	EIC EXTINT3	GLOC IN2	ADCIFE TRIGGER		CATB SENSE1
30	C3	30	C3	PA06	6	VDDANA	DACC VOUT	USART0 RTS	EIC EXTINT1	GLOC IN0	ACIFC ACAN0		CATB SENSE2
31	D3	31	D3	PA07	7	VDDANA	ADCIFE AD2	USART0 TXD	EIC EXTINT4	GLOC IN3	ACIFC ACAP0		CATB SENSE3
44	G2	44	G2	PA08	8	LCDA	USART0 RTS	TC0 A0	PEVC PAD EVT0	GLOC OUT0		LCDCA SEG23	CATB SENSE4
47	F5	47	F5	PA09	9	LCDA	USART0 CTS	TC0 B0	PEVC PAD EVT1	PARC PCDATA0		LCDCA COM3	CATB SENSE5
48	H2	48	H2	PA10	10	LCDA	USART0 CLK	TC0 A1	PEVC PAD EVT2	PARC PCDATA1		LCDCA COM2	CATB SENSE6
49	H3	49	H3	PA11	11	LCDA	USART0 RXD	TC0 B1	PEVC PAD EVT3	PARC PCDATA2		LCDCA COM1	CATB SENSE7
50	J2	50	J2	PA12	12	LCDA	USART0 TXD	TC0 A2		PARC PCDATA3		LCDCA COM0	CATB DIS
63	H5	63	H5	PA13	13	LCDA	USART1 RTS	TC0 B2	SPI NPCS1	PARC PCDATA4		LCDCA SEG5	CATB SENSE8
64	K7	64	K7	PA14	14	LCDA	USART1 CLK	TC0 CLK0	SPI NPCS2	PARC PCDATA5		LCDCA SEG6	CATB SENSE9
65	G5	65	G5	PA15	15	LCDA	USART1 RXD	TC0 CLK1	SPI NPCS3	PARC PCDATA6		LCDCA SEG7	CATB SENSE10

Table 3-8. Signal Descriptions List (Sheet 4 of 4)

Signal Name	Function	Type	Active Level	Comments
PA31 - PA00	Parallel I/O Controller I/O Port A	I/O		
PB15 - PB00	Parallel I/O Controller I/O Port B	I/O		
PC31 - PC00	Parallel I/O Controller I/O Port C	I/O		

Note: 1. See "Power and Startup Considerations" section.

3.4 I/O Line Considerations

3.4.1 SW/JTAG Pins

The JTAG pins switch to the JTAG functions if a rising edge is detected on TCK low after the RESET_N pin has been released. The TMS, and TDI pins have pull-up resistors when used as JTAG pins. The TCK pin always has pull-up enabled during reset. The JTAG pins can be used as GPIO pins and multiplexed with peripherals when the JTAG is disabled. Refer to Section 3.2.3 "JTAG Port Connections" on page 29 for the JTAG port connections.

For more details, refer to Section 1.1 "Enhanced Debug Port (EDP)" on page 3.

3.4.2 RESET_N Pin

The RESET_N pin is a schmitt input and integrates a permanent pull-up resistor to VDDIN. As the product integrates a power-on reset detector, the RESET_N pin can be left unconnected in case no reset from the system needs to be applied to the product.

3.4.3 TWI Pins

When these pins are used for TWI, the pins are open-drain outputs with slew-rate limitation and-inputs with inputs with spike-filtering. When used as GPIO-pins or used for other peripherals, the pins have the same characteristics as GPIO pins.

3.4.4 GPIO Pins

All the I/O lines integrate a pull-up/pull-down resistor and slew rate controller. Programming these features is performed independently for each I/O line through the GPIO Controllers. After reset, I/O lines default as inputs with pull-up and pull-down resistors disabled and slew rate enabled.

3.4.5 High-drive Pins

The six pins PA02, PB00, PB01, PC04, PC05 and PC06 have high-drive output capabilities. Refer to Section 9.6.2 "High-drive I/O Pin : PA02, PC04, PC05, PC06" on page 115 for electrical characteristics.

3.4.6 USB Pins

When these pins are used for USB, the pins are behaving according to the USB specification. When used as GPIO pins or used for other peripherals, the pins have the same behavior as other normal I/O pins, but the characteristics are different. Refer to Section 9.6.3 "USB I/O Pin : PA25, PA26" on page 116 for electrical characteristics.

These pins are compliant to USB standard only when VDDIO power supply is 3.3V nominal.

3.4.7 ADC Input Pins

These pins are regular I/O pins powered from the VDDANA.

6.2 Power Supplies

The ATSAM4L8/L4/L2 has several types of power supply pins:

- VDDIO: Powers I/O lines, the general purpose oscillator (OSC), the 80MHz integrated RC oscillator (RC80M) . Voltage is 1.68V to 3.6V.
- VLCDIN: (ATSAM4LC only) Powers the LCD voltage pump. Voltage is 1.68V to 3.6V.
- VDDIN: Powers the internal voltage regulator. Voltage is 1.68V to 3.6V.
- VDDANA: Powers the ADC, the DAC, the Analog Comparators, the 32kHz oscillator (OSC32K), the 32kHz integrated RC oscillator (RC32K)and the Brown-out detectors (BOD18 and BOD33). Voltage is 1.68V to 3.6V nominal.
- VDDCORE: Powers the core, memories, peripherals, the PLL, the DFLL, the 4MHz integrated RC oscillator (RCFAST) and the 115kHz integrated RC oscillator (RCSYS).
  - VDDOUT is the output voltage of the regulator and must be connected with or without an inductor to VDDCORE.

The ground pins GND are common to VDDCORE, VDDIO, and VDDIN. The ground pin for VDDANA is GNDANA.

For decoupling recommendations for the different power supplies, refer to the schematic document.

6.2.1 Voltage Regulator

An embedded voltage regulator supplies all the digital logic in the Core and the Backup power domains.

The regulator has two functionnal mode depending of BUCK/LDOn (PA02) pin value. When this pin is low, the regulator is in linear mode and VDDOUT must be connected to VDDCORE externally. When this pin is high, it behaves as a switching regulator and an inductor must be placed between VDDOUT and VDDCORE. The value of this pin is sampled during the power-up phase when the Power On Reset 33 reaches V_{POT+} (Section 9.9 ”Analog Characteristics” on page 129)

Its output voltages in the Core domain (V_{CORE}) and in the Backup domain (V_{BKUP}) are always equal except in Backup mode where the Core domain is not powered (V_{CORE}=0). The Backup domain is always powered. The voltage regulator features three different modes:

- Normal mode: the regulator is configured as linear or switching regulator. It can support all different Run and Sleep modes.
- Low Power (LP) mode: the regulator consumes little static current. It can be used in Wait modes.
- Ultra Low Power (ULP) mode: the regulator consumes very little static current . It is dedicated to Retention and Backup modes. In Backup mode, the regulator only supplies the backup domain.

At power-up or after a reset, the ATSAM4L8/L4/L2 is in the RUN0 mode. Only the necessary clocks are enabled allowing software execution. The Power Manager (PM) can be used to adjust the clock frequencies and to enable and disable the peripheral clocks.

When the CPU is entering a Power Save Mode, the CPU stops executing code. The user can choose between four Power Save Modes to optimize power consumption:

- SLEEP mode: the Cortex-M4 core is stopped, optionally some clocks are stopped, peripherals are kept running if enabled by the user.
- WAIT mode: all clock sources are stopped, the core and all the peripherals are stopped except the modules running with the 32kHz clock if enabled. This is the lowest power configuration where SleepWalking is supported.
- RETENTION mode: similar to the WAIT mode in terms of clock activity. This is the lowest power configuration where the logic is retained.
- BACKUP mode: the Core domain is powered off, the Backup domain is kept powered.

A wake up source exits the system to the RUN mode from which the Power Save Mode was entered.

A reset source always exits the system from the Power Save Mode to the RUN0 mode.

The configuration of the I/O lines are maintained in all Power Save Modes. Refer to Section 9. ”Backup Power Manager (BPM)” on page 677.

7.1.1 SLEEP mode

The SLEEP mode allows power optimization with the fastest wake up time.

The CPU is stopped. To further reduce power consumption, the user can switch off modules-clocks and synchronous clock sources through the BPM.PMCON.SLEEP field (See Table 7-1). The required modules will be halted regardless of the bit settings of the mask registers in the Power Manager (PM.AHBMASK, PM.APBxMASK).

Table 7-1. SLEEP mode Configuration

BPM.PSAVE.SLEEP	CPU clock	AHB clocks	APB clocks GCLK	Clock sources: OSC, RCFAST, RC80M, PLL, DFLL	RCSYS	OSC32K RC32K(2)	Wake up Sources
0	Stop	Run	Run	Run	Run	Run	Any interrupt
1	Stop	Stop	Run	Run	Run	Run	Any interrupt(1)
2	Stop	Stop	Stop	Run	Run	Run	Any interrupt(1)
3	Stop	Stop	Stop	Stop	Run	Run	Any interrupt(1)

Notes: 1. from modules with clock running.
2. OSC32K and RC32K will only remain operational if pre-enabled.

7.1.1.1 Entering SLEEP mode

The SLEEP mode is entered by executing the WFI instruction.

Additionally, if the SLEEPONEXIT bit in the Cortex-M4 System Control Register (SCR) is set, the SLEEP mode will also be entered when the Cortex-M4 exits the lowest priority ISR. This

7.1.4 Wakeup Time

7.1.4.1 Wakeup Time From SLEEP Mode

The latency depends on the clock sources wake up time. If the clock sources are not stopped, there is no latency to wake the clocks up.

7.1.4.2 Wakeup Time From WAIT or RETENTION Mode

The wake up latency consists of:

- the switching time from the low power configuration to the RUN mode power configuration. By default, the switching time is completed when all the voltage regulation system is ready. To speed-up the startup time, the user can set the Fast Wakeup bit in BPM.PMCON register.
- the wake up time of the RC oscillator used to start the system up. By default, the RCSYS oscillator is used to startup the system. The user can use another clock source (RCFAST for example) to speed up the startup time by configuring the PM.FASTWKUP register. Refer to Section 9. ”Power Manager (PM)” on page 677.
- the Flash memory wake up time.

To have the shortest wakeup time, the user should:

- set the BPM.PMCON.FASTWKUP bit.

- configure the PM.FASTSLEEP.FASTRCOSC field to use the RCFAST main clock.

- enter the WAIT or RETENTION mode

Upon a wakeup, this is required to keep the main clock connected to RCFAST until the voltage regulation system is fully ready (when BPM.ISR.PSOK bit is one). During this wakeup period, the FLASHCALW module is automatically configured to operate in “1 wait state mode”.

7.1.4.3 Wake time from BACKUP mode

It is equal to the Core domain logic reset latency (similar to the reset latency caused by an external reset in RESET_N pin) added to the time required for the voltage regulation system to be stabilized.

8.9.9 Unlimited Flash User Page Read Access

The SMAP can access the User page even if the protected state is set. Prior to operate such an access, the user should check that the module is not busy by checking that SR.STATE is equal to zerp. Once the offset of the word to access inside the page is written in ADDR.ADDR, the read operation can be initiated by writing a one in CR.FSPR. The SR.STATE field will indicate the FSPR state. Addresses written to ADDR.ADDR must be world aligned. Failing to do so will result in unpredictable behavior. The result can be read in the DATA register as soon as SR.DONE rises. The ADDR field is used as an offset in the page, bits outside a page boundary will be silently discarded. The ADDR register is automatically incremented at the end of the read operation making possible to dump consecutive words without writing the next offset into ADDR.ADDR.

8.9.10 32-bit Cyclic Redundancy Check (CRC)

The SMAP unit provides support for calculating a Cyclic Redundancy Check (CRC) value for a memory area. The algorithm used is the industry standard CRC32 algorithm using the generator polynomial 0xEDB88320.

8.9.10.1 Starting CRC Calculation

To calculate CRC for a memory range, the start address must be written into the ADDR register, and the size of the memory range into the LENGTH register. Both the start address and the length must be word aligned.

The initial value used for the CRC calculation must be written to the DATA register. This value will usually be 0xFFFFFFFF, but can be e.g. the result of a previous CRC calculation if generating a common CRC of separate memory blocks.

Once completed, the calculated CRC value can be read out of the DATA register. The read value must be inverted to match standard CRC32 implementations, or kept non-inverted if used as starting point for subsequent CRC calculations.

If the device is in protected state, it is only possible to calculate the CRC of the whole flash array. In most cases this area will be the entire onboard nonvolatile memory. The ADDR, LENGTH, and DATA registers will be forced to predefined values once the CRC operation is started, and user-written values are ignored. This allows the user to verify the contents of a protected device.

The actual test is started by writing a one in CR.CRC. A running CRC operation can be cancelled by disabling the module (write a one in CR.DIS). This has the effect of resetting the module. The module has to be restarted by issuing an enable command (write a one in CR.EN).

8.9.10.2 Interpreting the Results

The user should monitor the SR register (Refer to Section 8.9.11.2 ”Status Register” on page 83). When the operation is completed SR.DONE is set. Then the SR.BERR and SR.FAIL must be read to ensure that no bus error nor functional error occured.

8.9.11.3 Status Clear Register

Name: SCR

Access Type: Write-Only

Offset: 0x08

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	LCK	FAIL	BERR	HCR	DONE

Writing a zero to a bit in this register has no effect.
Writing a one to a bit clears the corresponding SR bit

Note: *Writing a one to bit HCR while the chip is in protected state has no effect*

Table 9-3. Supply Rise Rates and Order [1]

VDDIO, VDDIN and VDDANA must be connected together and as a consequence, rise synchronously

Symbol	Parameter	Rise Rate			
		Min	Max	Unit	Comment
V_{VDDIO}	DC supply peripheral I/Os	0.0001	2.5	V/µs	
V_{VDDIN}	DC supply peripheral I/Os and internal regulator	0.0001	2.5	V/µs	
V_{VDDANA}	Analog supply voltage	0.0001	2.5	V/µs	

1. These values are based on characterization. These values are not covered by test limits in production.

9.5 Power Consumption

9.5.1 Power Scaling 0 and 2

The values in Table 9-6 are measured values of power consumption under the following conditions, except where noted:

- Operating conditions for power scaling mode 0 and 2
  - V_{VDDIN} = 3.3V
  - Power Scaling mode 0 is used for CPU frequencies under 36MHz
  - Power Scaling mode 2 is used for CPU frequencies above 36MHz
- Wake up time from low power modes is measured from the edge of the wakeup signal to the first instruction fetched in flash.
- Oscillators
  - OSC0 (crystal oscillator) stopped
  - OSC32K (32kHz crystal oscillator) running with external 32kHz crystal
  - DFLL using OSC32K as reference and running at 48MHz
- Clocks
  - DFLL used as main clock source
  - CPU, AHB clocks undivided
  - APBC and APBD clocks divided by 4
  - APBA and APBB bridges off
  - The following peripheral clocks running
    - PM, SCIF, AST, FLASHCALW, APBC and APBD bridges
  - All other peripheral clocks stopped
- I/Os are inactive with internal pull-up
- CPU is running on flash with 1 wait state
- Low power cache enabled
- BOD18 and BOD33 disabled

Table 9-6. ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	296	326	µA/MHz
		85°C		300	332	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	320	377	
		85°C		326	380	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	177	198	
		85°C		179	200	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	186	232	
		85°C		195	239	

Table 9-7. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
SLEEP0	Switching mode	25°C	9 * Main clock cycles	3817	4033	µA
		85°C		4050	4507	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	2341	2477	
		85°C		2525	2832	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	1758	1862	
		85°C		1925	1971	
SLEEP3	Linear mode	25°C		51	60	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	6.7		
	OSC32K and AST stopped Fast wake-up enable			5.5		
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.9		
	AST and OSC32K stopped			3.0		
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

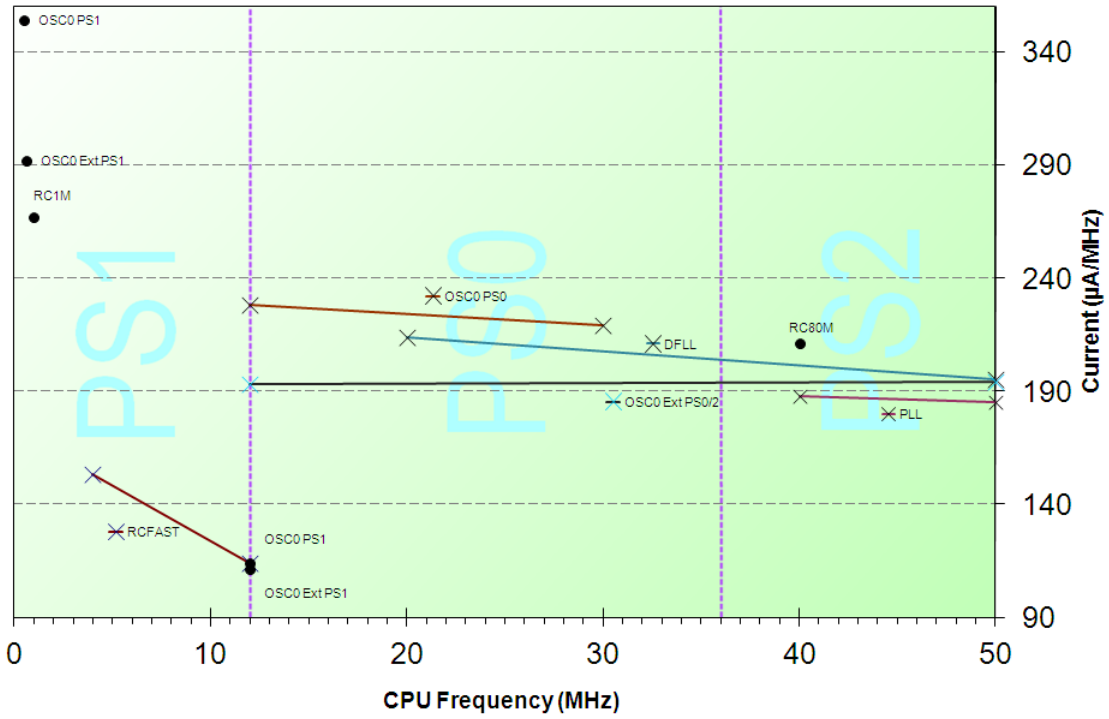
1. These values are based on characterization. These values are not covered by test limits in production.

9.5.2 Power Scaling 1

The values in Table 34-7 are measured values of power consumption under the following conditions, except where noted:

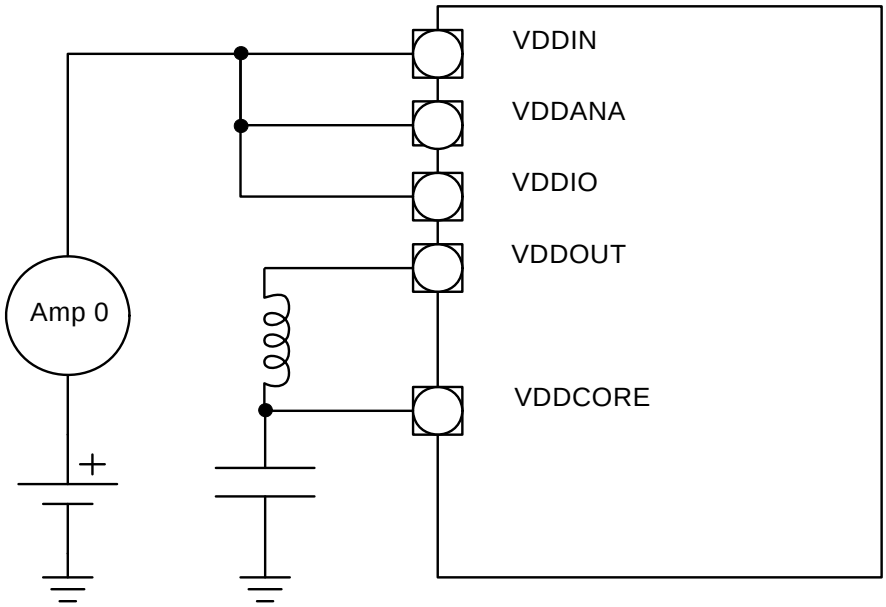
- Operating conditions for power scaling mode 1
  - V_{VDDIN} = 3.3V
- Wake up time from low power modes is measured from the edge of the wakeup signal to the first instruction fetched in flash.
- Oscillators
  - OSC0 (crystal oscillator) and OSC32K (32kHz crystal oscillator) stopped
  - RCFAST Running at 12MHz
- Clocks
  - RCFAST used as main clock source
  - CPU, AHB clocks undivided
  - APBC and APBD clocks divided by 4
  - APBA and APBB bridges off
  - The following peripheral clocks running
    - PM, SCIF, AST, FLASHCALW, APBC and APBD bridges

Figure 9-1. Typical Power Consumption running Coremark (from above table)



Note: For variable frequency oscillators, linear interpolation between high and low settings

Figure 9-2. Measurement Schematic, Switching Mode



9.6 I/O Pin Characteristics

9.6.1 Normal I/O Pin

Table 9-13. Normal I/O Pin Characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
R_{PULLUP}	Pull-up resistance (2)				40		kΩ
$R_{PULLDOWN}$	Pull-down resistance(2)				40		kΩ
V_{IL}	Input low-level voltage			-0.3		0.2 * V_{VDD}	V
V_{IH}	Input high-level voltage			0.8 * V_{VDD}		V_{VDD} + 0.3	V
V_{OL}	Output low-level voltage					0.4	V
V_{OH}	Output high-level voltage			V_{VDD} - 0.4			V
I_{OL}	Output low-level current (3)	ODCR0=0	1.68V<V_{VDD}<2.7V			0.8	mA
			2.7V<V_{VDD}<3.6V			1.6	mA
		ODCR0=1	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	mA
I_{OH}	Output high-level current(3)	ODCR0=0	1.68V<V_{VDD}<2.7V			0.8	mA
			2.7V<V_{VDD}<3.6V			1.6	mA
		ODCR0=1	1.68V<V_{VDD}<2.7V			1.6	mA
			2.7V<V_{VDD}<3.6V			3.2	mA
t_{RISE}	Rise time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, load = 25pF			35	ns
		OSRR0=1				45	ns
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, load = 25pF			19	ns
		OSRR0=1				23	ns
t_{FALL}	Fall time(2)	OSRR0=0	ODCR0=0 1.68V<V_{VDD}<2.7V, load = 25pF			36	ns
		OSRR0=1				47	ns
		OSRR0=0	ODCR0=0 2.7V<V_{VDD}<3.6V, load = 25pF			20	ns
		OSRR0=1				24	ns
F_{PINMAX}	Output frequency(2)	OSRR0=0	ODCR0=0, V_{VDD}>2.7V load = 25pF			17	MHz
		OSRR0=1				15	MHz
		OSRR0=0	ODCR0=1, V_{VDD}>2.7V load = 25pF			27	MHz
		OSRR0=1				23	MHz
I_{LEAK}	Input leakage current(3)		Pull-up resistors disabled		0.01	1	µA
C_{IN}	Input capacitance(2)				5		pF

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details
2. These values are based on simulation. These values are not covered by test limits in production or characterization

9.7 Oscillator Characteristics

9.7.1 Oscillator 0 (OSC0) Characteristics

9.7.1.1 Digital Clock Characteristics

The following table describes the characteristics for the oscillator when a digital clock is applied on XIN.

Table 9-22. Digital Clock Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{CPXIN}	XIN clock frequency (1)				50	MHz
t_{CPXIN}	XIN clock duty cycle(1)		40		60	%
$t_{STARTUP}$	Startup time			N/A		cycles

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.7.1.2 Crystal Oscillator Characteristics

The following table describes the characteristics for the oscillator when a crystal is connected between XIN and XOUT as shown in Figure 9-3. The user must choose a crystal oscillator where the crystal load capacitance C_L is within the range given in the table. The exact value of C_L can be found in the crystal datasheet. The capacitance of the external capacitors (C_{LEXT}) can then be computed as follows:

$$C_{LEXT} = 2(C_L - C_{STRAY} - C_{SHUNT})$$

where C_{STRAY} is the capacitance of the pins and PCB, C_{SHUNT} is the shunt capacitance of the crystal.

Table 9-23. Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Crystal oscillator frequency (1)		0.6		30	MHz
ESR	Crystal Equivalent Series Resistance (2)	f = 0.455MHz, C_{LEXT} = 100pF SCIF.OSCCTRL.GAIN = 0			17000	Ω
		f = 2MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 0			2000	
		f = 4MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 1			1500	
		f = 8MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 2			300	
		f = 16MHz, C_{LEXT} = 20pF SCIF.OSCCTRL.GAIN = 3			350	
		f = 30MHz, C_{LEXT} = 18pF SCIF.OSCCTRL.GAIN = 4			45	

9.7.7 1MHz RC Oscillator (RC1M) Characteristics

Table 9-30. RC1M Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)		0.91	1	1.12	MHz
I_{RC1M}	Current consumption (2)			35		µA
Duty	Duty cycle(1)		48.6	49.9	54.4	%

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

9.7.8 4/8/12MHz RC Oscillator (RCFAST) Characteristics

Table 9-31. RCFAST Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OUT}	Output frequency (1)	Calibrated, FRANGE=0	4	4.3	4.6	MHz
		Calibrated, FRANGE=1	7.8	8.2	8.5	
		Calibrated, FRANGE=2	11.3	12	12.3	
I_{RCFAST}	Current consumption (2)	Calibrated, FRANGE=0		90	110	µA
		Calibrated, FRANGE=1		130	150	
		Calibrated, FRANGE=2		180	205	
Duty	Duty cycle(1)	Calibrated, FRANGE=0	48.8	49.6	50.1	%
		Calibrated, FRANGE=1	47.8	49.2	50.1	
		Calibrated, FRANGE=2	46.7	48.8	50.0	
$t_{STARTUP}$	Startup time(1)	Calibrated, FRANGE=2	0.1	0.31	0.71	µs

1. These values are based on characterization. These values are not covered by test limits in production.
2. These values are based on simulation. These values are not covered by test limits in production or characterization.

Table 9-39. VREG Electrical Characteristics in Switching mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	DC output current(1)	$V_{VDDCORE}$ > 1.65V			55	mA
	Output DC load regulation(1) Transient load regulation	I_{OUT} = 0 to 50mA, V_{VDDIN} = 3V	-136	-101	-82	mV
	Output DC regulation(1)	I_{OUT} = 50 mA, V_{VDDIN} = 2V to 3.6V	-20	38	99	mV
I_Q	Quescient current(1)	V_{VDDIN} = 2V, I_{OUT} = 0 mA	97	186	546	µA
		V_{VDDIN} > 2.2V, I_{OUT} = 0 mA	97	111	147	
P_{EFF}	Power efficiency(1)	I_{OUT} = 5mA, 50mA Reference power not included	82.7	88.3	95	%

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-40. Decoupling Requirements in Switching Mode

Symbol	Parameter	Technology	Typ	Units
C_{IN1}	Input regulator capacitor 1		33	nF
C_{IN2}	Input regulator capacitor 2		100	
C_{IN3}	Input regulator capacitor 3		10	µF
C_{OUT1}	Output regulator capacitor 1	X7R MLCC	100	nF
C_{OUT2}	Output regulator capacitor 2	X7R MLCC (ex : GRM31CR71A475)	4.7	µF
L_{EXT}	External inductance	(ex: Murata LQH3NPN220MJ0)	22	µH
R_{DCLEXT}	Serial resistance of L_{EXT}		0.7	Ω
$ISAT_{LEXT}$	Saturation current of L_{EXT}		300	mA

Note: 1. Refer to Section 6. on page 46.

The maximum SPI master output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(f_{PINMAX}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI delay, SPI2 or SPI5 depending on CPOL and NCPHA. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

Maximum SPI Frequency, Master Input

The maximum SPI master input frequency is given by the following formula:

$$f_{SPCKMAX} = \frac{1}{SPIn + t_{VALID}}$$

Where $SPIn$ is the MISO setup and hold time, SPI0 + SPI1 or SPI3 + SPI4 depending on CPOL and NCPHA. t_{VALID} is the SPI slave response time. refer to the SPI slave datasheet for t_{VALID} .

9.10.3.2 Slave mode

Figure 9-14. SPI Slave Mode with (CPOL= 0 and NCPHA= 1) or (CPOL= 1 and NCPHA= 0)

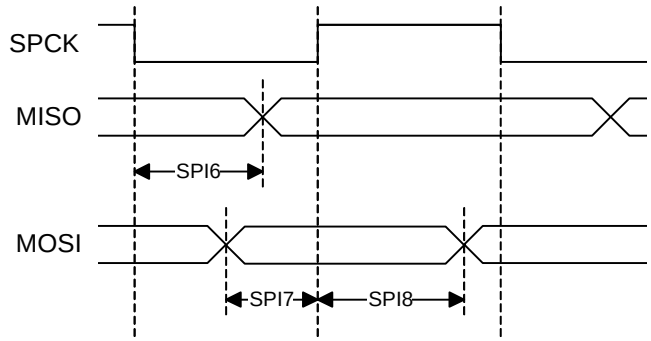
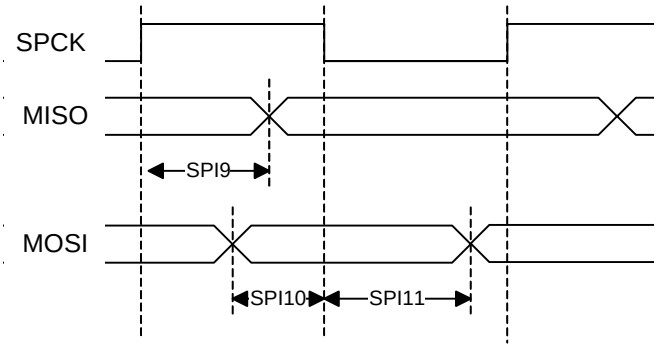


Figure 9-15. SPI Slave Mode with (CPOL= NCPHA= 0) or (CPOL= NCPHA= 1)



Where $SPIn$ is the MISO delay, SPI6 or SPI9 depending on CPOL and NCPHA. t_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for t_{SETUP} . f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

9.10.4 TWIM/TWIS Timing

Figure 9-64 shows the TWI-bus timing requirements and the compliance of the device with them. Some of these requirements (t_r and t_f) are met by the device without requiring user intervention. Compliance with the other requirements (t_{HD-STA}, t_{SU-STA}, t_{SU-STO}, t_{HD-DAT}, $t_{SU-DAT-TWI}$, $t_{LOW-TWI}$, t_{HIGH}, and f_{TWCK}) requires user intervention through appropriate programming of the relevant TWIM and TWIS user interface registers. refer to the TWIM and TWIS sections for more information.

Table 9-64. TWI-Bus Timing Requirements

Symbol	Parameter	Mode	Minimum		Maximum		Unit
			Requirement	Device	Requirement	Device	
t_r	TWCK and TWD rise time	Standard(1)	-		1000		ns
		Fast(1)	$20 + 0.1C_b$		300		
t_f	TWCK and TWD fall time	Standard	-		300		ns
		Fast	$20 + 0.1C_b$		300		
t_{HD-STA}	(Repeated) START hold time	Standard	4	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STA}	(Repeated) START set-up time	Standard	4.7	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STO}	STOP set-up time	Standard	4.0	$4t_{clkpb}$	-		µs
		Fast	0.6				
t_{HD-DAT}	Data hold time	Standard	0.3(2)	$2t_{clkpb}$	3.45()	$15t_{prescaled} + t_{clkpb}$	µs
		Fast			0.9()		
$t_{SU-DAT-TWI}$	Data set-up time	Standard	250	$2t_{clkpb}$	-		ns
		Fast	100				
t_{SU-DAT}		-	-	t_{clkpb}	-		-
$t_{LOW-TWI}$	TWCK LOW period	Standard	4.7	$4t_{clkpb}$	-		µs
		Fast	1.3				
t_{LOW}		-	-	t_{clkpb}	-		-
t_{HIGH}	TWCK HIGH period	Standard	4.0	$8t_{clkpb}$	-		µs
		Fast	0.6				
f_{TWCK}	TWCK frequency	Standard	-		100	$\frac{1}{12t_{clkpb}}$	kHz
		Fast			400		

Notes: 1. Standard mode: $f_{TWCK} \leq 100$ kHz ; fast mode: $f_{TWCK} > 100$ kHz .

12.1.7 FLASHCALW

Corrupted data in flash may happen after flash page write operations.
After a flash page write operation, reading (data read or code fetch) in flash may fail. This may lead to an expecption or to others errors derived from this corrupted read access.
Fix/Workaround
Before any flash page write operation, each 64-bit doublewords write in the page buffer must preceded by a 64-bit doublewords write in the page buffer with 0xFFFFFFFF_FFFFFFFF content at any address in the page. Note that special care is required when loading page buffer, refer to Section 2.5.9 ”Page Buffer Operations” on page 11.