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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls8ca-au

2.2 Configuration Summary

Table 2-1. Sub Series Summary

Feature	ATSAM4LC	ATSAM4LS
SEGMENT LCD	Yes	No
AESA	Yes	No
USB	Device + Host	Device Only

Table 2-2. ATSAM4LC Configuration Summary

Feature	ATSAM4LC8/4/2C	ATSAM4LC8/4/2B	ATSAM4LC8/4/2A
Number of Pins	100	64	48
Max Frequency	48MHz		
Flash	512/256/128KB		
SRAM	64/32/32KB		
SEGMENT LCD	4x40	4x23	4x13
GPIO	75	43	27
High-drive pins	6	3	1
External Interrupts	8 + 1 NMI		
TWI	2 Masters + 2 Masters/Slaves		1 Master + 1 Master/Slave
USART	4		3 in LC sub series 4 in LS sub series
PICOUART	1		0
Peripheral DMA Channels	16		
AESA	1		
Peripheral Event System	1		
SPI	1		
Asynchronous Timers	1		
Timer/Counter Channels	6	3	
Parallel Capture Inputs	8		
Frequency Meter	1		
Watchdog Timer	1		
Power Manager	1		
Glue Logic LUT	2		1

3.2 Peripheral Multiplexing on I/O lines

3.2.1 Multiplexed Signals

Each GPIO line can be assigned to one of the peripheral functions. The following tables (Section 3-1 ”100-pin GPIO Controller Function Multiplexing” on page 19 to Section 3-4 ”48-pin GPIO Controller Function Multiplexing” on page 28) describes the peripheral signals multiplexed to the GPIO lines.

Peripheral functions that are not relevant in some parts of the family are grey-shaded.

For description of differents Supply voltage source, refer to the Section 6. ”Power and Startup Considerations” on page 46.

Table 3-1. 100-pin GPIO Controller Function Multiplexing (Sheet 1 of 4)

ATSAM4LC		ATSAM4LS		Pin	GPIO	Supply	GPIO Functions						
QFN	VFBGA	QFN	VFBGA				A	B	C	D	E	F	G
5	B9	5	B9	PA00	0	VDDIO							
6	B8	6	B8	PA01	1	VDDIO							
12	A7	12	A7	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
19	B3	19	B3	PA03	3	VDDIN		SPI MISO					
24	A2	24	A2	PA04	4	VDDANA	ADCIFE AD0	USART0 CLK	EIC EXTINT2	GLOC IN1			CATB SENSE0
25	A1	25	A1	PA05	5	VDDANA	ADCIFE AD1	USART0 RXD	EIC EXTINT3	GLOC IN2	ADCIFE TRIGGER		CATB SENSE1
30	C3	30	C3	PA06	6	VDDANA	DACC VOUT	USART0 RTS	EIC EXTINT1	GLOC IN0	ACIFC ACAN0		CATB SENSE2
31	D3	31	D3	PA07	7	VDDANA	ADCIFE AD2	USART0 TXD	EIC EXTINT4	GLOC IN3	ACIFC ACAP0		CATB SENSE3
44	G2	44	G2	PA08	8	LCDA	USART0 RTS	TC0 A0	PEVC PAD EVT0	GLOC OUT0		LCDCA SEG23	CATB SENSE4
47	F5	47	F5	PA09	9	LCDA	USART0 CTS	TC0 B0	PEVC PAD EVT1	PARC PCDATA0		LCDCA COM3	CATB SENSE5
48	H2	48	H2	PA10	10	LCDA	USART0 CLK	TC0 A1	PEVC PAD EVT2	PARC PCDATA1		LCDCA COM2	CATB SENSE6
49	H3	49	H3	PA11	11	LCDA	USART0 RXD	TC0 B1	PEVC PAD EVT3	PARC PCDATA2		LCDCA COM1	CATB SENSE7
50	J2	50	J2	PA12	12	LCDA	USART0 TXD	TC0 A2		PARC PCDATA3		LCDCA COM0	CATB DIS
63	H5	63	H5	PA13	13	LCDA	USART1 RTS	TC0 B2	SPI NPCS1	PARC PCDATA4		LCDCA SEG5	CATB SENSE8
64	K7	64	K7	PA14	14	LCDA	USART1 CLK	TC0 CLK0	SPI NPCS2	PARC PCDATA5		LCDCA SEG6	CATB SENSE9
65	G5	65	G5	PA15	15	LCDA	USART1 RXD	TC0 CLK1	SPI NPCS3	PARC PCDATA6		LCDCA SEG7	CATB SENSE10

Table 3-8. Signal Descriptions List (Sheet 2 of 4)

Signal Name	Function	Type	Active Level	Comments
Inter-IC Sound (I2S) Controller - IISC				
IMCK	I2S Master Clock	Output		
ISCK	I2S Serial Clock	I/O		
ISDI	I2S Serial Data In	Input		
ISDO	I2S Serial Data Out	Output		
IWS	I2S Word Select	I/O		
LCD Controller - LCDCA				
BIASL	Bias voltage (1/3 VLCD)	Analog		
BIASH	Bias voltage (2/3 VLCD)	Analog		
CAPH	High voltage end of flying capacitor	Analog		
CAPL	Low voltage end of flying capacitor	Analog		
COM3 - COM0	Common terminals	Analog		
SEG39 - SEG0	Segment terminals	Analog		
VLCD	Bias voltage	Analog		
Parallel Capture - PARC				
PCCK	Clock	Input		
PCDATA7 - PCDATA0	Data lines	Input		
PCEN1	Data enable 1	Input		
PCEN2	Data enable 2	Input		
Peripheral Event Controller - PEVC				
PAD_EVT3 - PAD_EVT0	Event Inputs	Input		
Power Manager - PM				
RESET_N	Reset	Input	Low	
System Control Interface - SCIF				
GCLK3 - GCLK0	Generic Clock Outputs	Output		
GCLK_IN1 - GCLK_IN0	Generic Clock Inputs	Input		
XIN0	Crystal 0 Input	Analog/ Digital		
XOUT0	Crystal 0 Output	Analog		
Serial Peripheral Interface - SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
NPCS3 - NPCS0	SPI Peripheral Chip Selects	I/O	Low	
SCK	Clock	I/O		
Timer/Counter - TC0, TC1				

Table 3-8. Signal Descriptions List (Sheet 3 of 4)

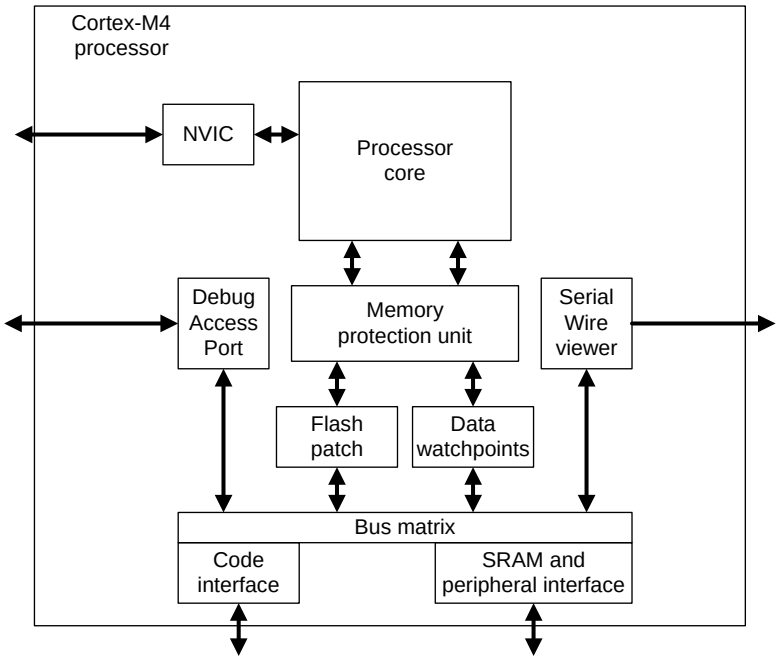
Signal Name	Function	Type	Active Level	Comments
A0	Channel 0 Line A	I/O		
A1	Channel 1 Line A	I/O		
A2	Channel 2 Line A	I/O		
B0	Channel 0 Line B	I/O		
B1	Channel 1 Line B	I/O		
B2	Channel 2 Line B	I/O		
CLK0	Channel 0 External Clock Input	Input		
CLK1	Channel 1 External Clock Input	Input		
CLK2	Channel 2 External Clock Input	Input		
Two-wire Interface - TWIMS0, TWIMS1, TWIM2, TWIM3				
TWCK	Two-wire Serial Clock	I/O		
TWD	Two-wire Serial Data	I/O		
Universal Synchronous Asynchronous Receiver Transmitter - USART0, USART1, USART2, USART3				
CLK	Clock	I/O		
CTS	Clear To Send	Input	Low	
RTS	Request To Send	Output	Low	
RXD	Receive Data	Input		
TXD	Transmit Data	Output		
USB 2.0 Interface - USBC				
DM	USB Full Speed Interface Data -	I/O		
DP	USB Full Speed Interface Data +	I/O		
Power				
GND	Ground	Ground		
GNDANA	Analog Ground	Ground		
VDDANA	Analog Power Supply	Power Input		1.68V to 3.6V
VDDCORE	Core Power Supply	Power Input		1.68V to 1.98V
VDDIN	Voltage Regulator Input	Power Input		1.68V to 3.6V
VDDIO	I/O Pads Power Supply	Power Input		1.68V to 3.6V. VDDIO must always be equal to or lower than VDDIN.
VDDOUT	Voltage Regulator Output	Power Output		1.08V to 1.98V
General Purpose I/O				

4. Cortex-M4 processor and core peripherals

4.1 Cortex-M4

The Cortex-M4 processor is a high performance 32-bit processor designed for the microcontroller market. It offers significant benefits to developers, including:

- **outstanding processing performance combined with fast interrupt handling**
- **enhanced system debug with extensive breakpoint and trace capabilities**
- **efficient processor core, system and memories**
- **ultra-low power consumption with integrated sleep modes**
- **platform security robustness, with integrated memory protection unit (MPU).**



The Cortex-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, saturating arithmetic and dedicated hardware division.

To facilitate the design of cost-sensitive devices, the Cortex-M4 processor implements tightly-coupled system components that reduce processor area while significantly improving interrupt handling and system debug capabilities. The Cortex-M4 processor implements a version of the Thumb® instruction set based on Thumb-2 technology, ensuring high code density and reduced program memory requirements. The Cortex-M4 instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers.

The Cortex-M4 processor closely integrates a configurable Nested Vectored Interrupt Controller (NVIC), to deliver industry-leading interrupt performance. The NVIC includes a *non-maskable interrupt* (NMI), and provides up to 80 interrupt priority levels. The tight integration of the proces-

sor core and NVIC provides fast execution of interrupt service routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to suspend load-multiple and store-multiple operations. Interrupt handlers do not require wrapping in assembler code, removing any code overhead from the ISRs. A tail-chain optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes, that include a deep sleep function enabling the entire device to be rapidly powered down while still retaining program state.

4.2 System level interface

The Cortex-M4 processor provides multiple interfaces using AMBA® technology to provide high speed, low latency memory accesses. It supports unaligned data accesses and implements atomic bit manipulation that enables faster peripheral controls, system spinlocks and thread-safe Boolean data handling.

The Cortex-M4 processor has an *memory protection unit* (MPU) that provides fine grain memory control, enabling applications to utilize multiple privilege levels, separating and protecting code, data and stack on a task-by-task basis. Such requirements are becoming critical in many embedded applications such as automotive.

4.3 Integrated configurable debug

The Cortex-M4 processor implements a complete hardware debug solution. This provides high system visibility of the processor and memory through either a traditional JTAG port or a 2-pin *Serial Wire Debug* (SWD) port that is ideal for microcontrollers and other small package devices.

For system trace the processor integrates an *Instrumentation Trace Macrocell* (ITM) alongside data watchpoints and a profiling unit. To enable simple and cost-effective profiling of the system events these generate, a *Serial Wire Viewer* (SWV) can export a stream of software-generated messages, data trace, and profiling information through a single pin.

The *Flash Patch and Breakpoint Unit* (FPB) provides 8 hardware breakpoint comparators that debuggers can use. The comparators in the FPB also provide remap functions of up to 8 words in the program code in the CODE memory region. This enables applications stored on a non-erasable, ROM-based microcontroller to be patched if a small programmable memory, for example flash, is available in the device. During initialization, the application in ROM detects, from the programmable memory, whether a patch is required. If a patch is required, the application programs the FPB to remap a number of addresses. When those addresses are accessed, the accesses are redirected to a remap table specified in the FPB configuration, which means the program in the non-modifiable ROM can be patched.

A specific Peripheral Debug (PDBG) register is implemented in the Private Peripheral Bus address map. This register allows the user to configure the behavior of some modules in debug mode.

4.4 Cortex-M4 processor features and benefits summary

- **tight integration of system peripherals reduces area and development costs**
- **Thumb instruction set combines high code density with 32-bit performance**
- **code-patch ability for ROM system updates**
- **power control optimization of system components**
- **integrated sleep modes for low power consumption**
- **fast code execution permits slower processor clock or increases sleep mode time**
- **hardware division and fast digital-signal-processing orientated multiply accumulate**
- **saturating arithmetic for signal processing**
- **deterministic, high-performance interrupt handling for time-critical applications**
- ***memory protection unit* (MPU) for safety-critical applications**
- **extensive debug and trace capabilities:**
  - **Serial Wire Debug and Serial Wire Trace reduce the number of pins required for debugging, tracing, and code profiling.**

4.5 Cortex-M4 core peripherals

These are:

Nested Vectored Interrupt Controller

The NVIC is an embedded interrupt controller that supports low latency interrupt processing.

System control block

The *System control block* (SCB) is the programmers model interface to the processor. It provides system implementation information and system control, including configuration, control, and reporting of system exceptions.

System timer

The system timer, SysTick, is a 24-bit count-down timer. Use this as a Real Time Operating System (RTOS) tick timer or as a simple counter.

Memory protection unit

The *Memory protection unit* (MPU) improves system reliability by defining the memory attributes for different memory regions. It provides up to eight different regions, and an optional predefined background region.

The complete Cortex-M4 User Guide can be found on the ARM web site:

http://infocenter.arm.com/help/topic/com.arm.doc.dui0553a/DUI0553A_cortex_m4_dgug.pdf

4.6 Cortex-M4 implementations options

This table provides the specific configuration options implemented in the SAM4L series

Option	Implementation
Inclusion of MPU	yes
Inclusion of FPU	No
Number of interrupts	80
Number of priority bits	4
Inclusion of the WIC	No
Embedded Trace Macrocell	No
Sleep mode instruction	Only WFI supported
Endianness	Little Endian
Bit-banding	No
SysTick timer	Yes
Register reset values	No

Table 4-1. Cortex-M4 implementation options

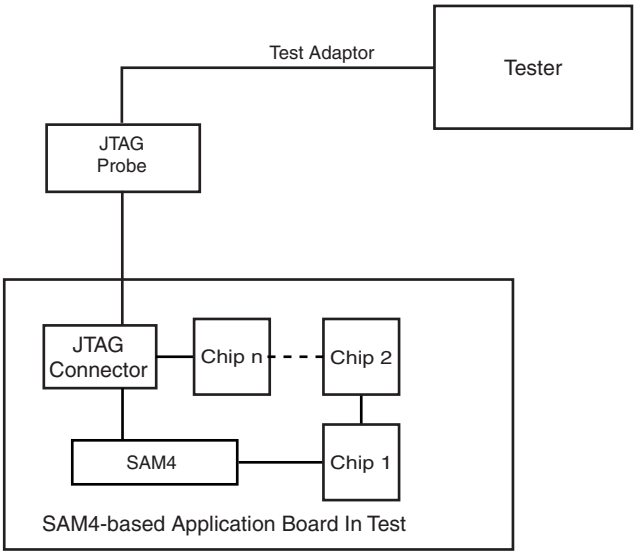
4.7 Cortex-M4 Interrupts map

The table below shows how the interrupt request signals are connected to the NVIC.

Table 4-2. Interrupt Request Signal Map (Sheet 1 of 3)

Line	Module	Signal
0	Flash Controller	HFLASHC
1	Peripheral DMA Controller	PDCA 0
2	Peripheral DMA Controller	PDCA 1
3	Peripheral DMA Controller	PDCA 2
4	Peripheral DMA Controller	PDCA 3
5	Peripheral DMA Controller	PDCA 4
6	Peripheral DMA Controller	PDCA 5
7	Peripheral DMA Controller	PDCA 6
8	Peripheral DMA Controller	PDCA 7
9	Peripheral DMA Controller	PDCA 8
10	Peripheral DMA Controller	PDCA 9
11	Peripheral DMA Controller	PDCA 10

Figure 8-9. Application Test Environment Example



8.11.3 How to initialize test and debug features

To enable the JTAG pins a falling edge event must be detected on the TCK pin at any time after the RESET_N pin is released.

Certain operations requires that the system is prevented from running code after reset is released. This is done by holding low the TCK pin after the RESET_N is released. This makes the SMAP assert the core_hold_reset signal that hold the Cortex-M4 core under reset.

To make the CPU run again, clear the CHR bit in the Status Register (SR.CHR) to de-assert the core_hold_reset signal. Independent of the initial state of the TAP Controller, the Test-Logic-Reset state can always be entered by holding TMS high for 5 TCK clock periods. This sequence should always be applied at the start of a JTAG session and after enabling the JTAG pins to bring the TAP Controller into a defined state before applying JTAG commands. Applying a 0 on TMS for 1 TCK period brings the TAP Controller to the Run-Test/Idle state, which is the starting point for JTAG operations.

8.11.4 How to disable test and debug features

To disable the JTAG pins the TCK pin must be held high while RESET_N pin is released.

8.11.5 Typical JTAG sequence

Assuming Run-Test/Idle is the present state, a typical scenario for using the JTAG interface is:

8.11.5.1 Scanning in JTAG instruction

At the TMS input, apply the sequence 1, 1, 0, 0 at the rising edges of TCK to enter the Shift Instruction Register - Shift-IR state. While in this state, shift the 4 bits of the JTAG instructions into the JTAG instruction register from the TDI input at the rising edge of TCK. The TMS input must be held low during input of the 4 LSBs in order to remain in the Shift-IR state. The JTAG Instruction selects a particular Data Register as path between TDI and TDO and controls the circuitry surrounding the selected Data Register.

Table 9-5. Maximum Clock Frequencies in Power Scaling Mode 1 and RUN Mode

Symbol	Parameter	Description	Max	Units
f_{CPU}	CPU clock frequency		12	MHz
f_{PBA}	PBA clock frequency		12	
f_{PBB}	PBB clock frequency		12	
f_{PBC}	PBC clock frequency		12	
f_{PBD}	PBD clock frequency		12	
f_{GCLK0}	GCLK0 clock frequency	DFLLIF main reference, GCLK0 pin	16.6	
f_{GCLK1}	GCLK1 clock frequency	DFLLIF dithering and SSGreference, GCLK1 pin	16.6	
f_{GCLK2}	GCLK2 clock frequency	AST, GCLK2 pin	6.6	
f_{GCLK3}	GCLK3 clock frequency	CATB, GCLK3 pin	17.3	
f_{GCLK4}	GCLK4 clock frequency	FLO and AESA	16.6	
f_{GCLK5}	GCLK5 clock frequency	GLOC, TC0 and RC32KIFB_REF	26.6	
f_{GCLK6}	GCLK6 clock frequency	ABDACB and IISC	16.6	
f_{GCLK7}	GCLK7 clock frequency	USBC	16.6	
f_{GCLK8}	GCLK8 clock frequency	TC1 and PEVC[0]	16.6	
f_{GCLK9}	GCLK9 clock frequency	PLL0 and PEVC[1]	16.6	
f_{GCLK10}	GCLK10 clock frequency	ADCIFE	16.6	
f_{GCLK11}	GCLK11 clock frequency	Master generic clock. Can be used as source for other generic clocks	51.2	
f_{OSC0}	OSC0 output frequency	Oscillator 0 in crystal mode	16	
		Oscillator 0 in digital clock mode	16	
f_{PLL}	PLL output frequency	Phase Locked Loop	N/A	
f_{DFLL}	DFLL output frequency	Digital Frequency Locked Loop	N/A	
f_{RC80M}	RC80M output frequency	Internal 80MHz RC Oscillator	N/A	

Table 9-6. ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
SLEEP0	Switching mode	25°C	9 * Main clock cycles	3817	4033	µA
		85°C		3934	4174	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	2341	2477	
		85°C		2437	2585	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	1758	1862	
		85°C		1847	1971	
SLEEP3	Linear mode	25°C		51	60	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	5.9	8.7	
	OSC32K and AST stopped Fast wake-up enable			4.7	7.6	
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.1	5.1	
	AST and OSC32K stopped			2.2	4.2	
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-7. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	319	343	µA/MHz
		85°C		326	350	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	343	387	
		85°C		351	416	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	181	198	
		85°C		186	203	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	192	232	
		85°C		202	239	

Table 9-9. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 1

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	222	240	µA/MHz
		85°C		233	276	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	233	276	
		85°C		230	270	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	100	112	
		85°C		100	119	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	104	128	
		85°C		107	138	
SLEEP0	Switching mode	25°C	9 * Main clock cycles	527	627	µA
		85°C		579	739	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	369	445	
		85°C		404	564	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	305	381	
		85°C		334	442	
SLEEP3	Linear mode	25°C		46	55	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	5.5		
	OSC32K and AST stopped Fast wake-up enable			4.3		
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.4		
	AST and OSC32K stopped			2.3		
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-10. Typical Power Consumption running CoreMark on CPU clock sources (1)

Clock Source	Conditions	Regulator	Frequency (MHz)	Typ	Unit

Table 9-10. Typical Power Consumption running CoreMark on CPU clock sources [1]

RCSYS (MCSEL = 0)	Power scaling mode 1	Switching Mode	0.115	978	µA/MHz
OSC0 (MCSEL = 1)	Power scaling mode 1		0.5	354	
			12	114	
	Power scaling mode 0		12	228	
			30	219	
OSC0 (MCSEL = 1) External Clock (MODE=0)	Power scaling mode 1		0.6	292	
			12	111	
	Power scaling mode 0		12	193	
	Power scaling mode 2		50	194	
PLL (MCSEL = 2)	Power scaling mode 2 Input Freq = 4MHz from OSC0		40	188	
			50	185	
DFLL (MCSEL = 3)	Power scaling mode 0 Input Freq = 32kHz from OSC32K		20	214	
	Power scaling mode 2 Input Freq = 32kHz from OSC32K		50	195	
RC1M (MCSEL = 4)	Power scaling mode 1		1	267	
RCFAST (MCSEL = 5)	Power scaling mode 1 RCFAST frequency is configurable from 4 to 12MHz		4	153	
			12	114	
RC80M (MCSEL = 6)	Power scaling mode 2 f_{CPU} = RC80M / 2 = 40MHz		40	211	

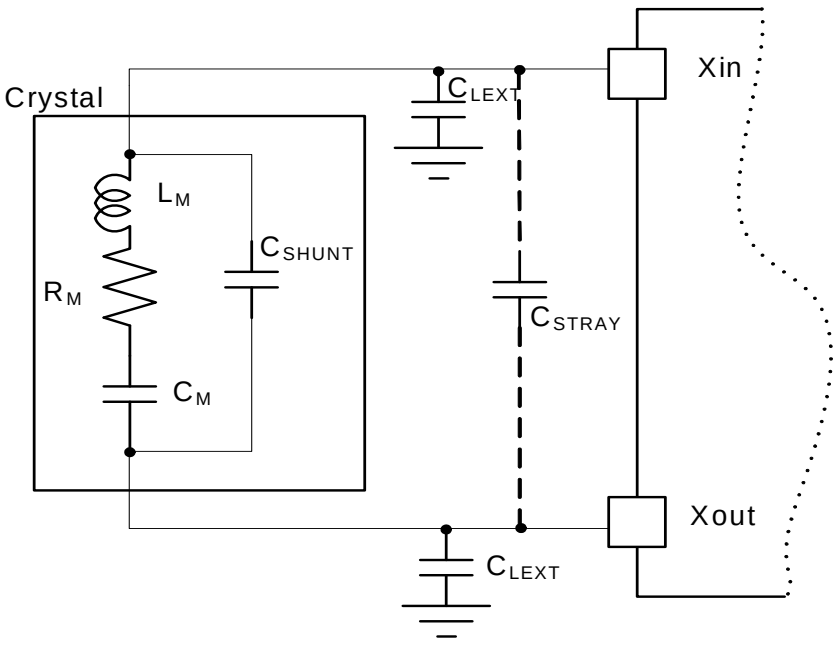
1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-23. Crystal Oscillator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_L	Crystal load capacitance[1]		6		18	pF
C_{SHUNT}	Crystal shunt capacitance[1]				7	
C_{XIN}	Parasitic capacitor load[2]	TQFP100 package		4.91		
C_{XOUT}	Parasitic capacitor load[2]			3.22		
$t_{STARTUP}$	Startup time[1]	SCIF.OSCCTRL.GAIN = 2		30000[3]		cycles
I_{OSC}	Current consumption[1]	Active mode, f = 0.6MHz, SCIF.OSCCTRL.GAIN = 0		30		µA
		Active mode, f = 4MHz, SCIF.OSCCTRL.GAIN = 1		130		
		Active mode, f = 8MHz, SCIF.OSCCTRL.GAIN = 2		260		
		Active mode, f = 16MHz, SCIF.OSCCTRL.GAIN = 3		590		
		Active mode, f = 30MHz, SCIF.OSCCTRL.GAIN = 4		960		

1. These values are based on simulation. These values are not covered by test limits in production or characterization.
2. These values are based on characterization. These values are not covered by test limits in production.
3. Nominal crystal cycles.

Figure 9-3. Oscillator Connection



9.9 Analog Characteristics

9.9.1 Voltage Regulator Characteristics

Table 9-36. VREG Electrical Characteristics in Linear and Switching Modes

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OUT}	DC output current (1) Power scaling mode 0 & 2	Low power mode (WAIT)	2000	3600	5600	µA
		Ultra Low power mode (RETENTION)	100	180	300	
	DC output current(1) Power scaling mode 1	Low power mode (WAIT)	4000	7000	10000	
		Ultra Low power mode (RETENTION)	200	350	600	
$V_{VDDCORE}$	DC output voltage	All modes			1.9	V

1. These values are based on simulation. These values are not covered by test limits in production.

Table 9-37. VREG Electrical Characteristics in Linear mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VDDIN}	Input voltage range	I_{OUT}=10mA	1.68		3.6	V
		I_{OUT}=50mA	1.8		3.6	
$V_{VDDCORE}$	DC output voltage (1) Power scaling mode 0 & 2	I_{OUT} = 0 mA	1.777	1.814	1.854	
		I_{OUT} = 50 mA	1.75	1.79	1.83	
I_{OUT}	DC output current(1)	$V_{VDDCORE}$ > 1.65V			100	mA
	Output DC load regulation(1) Transient load regulation	I_{OUT} = 0 to 80mA, V_{VDDIN} = 3V	-34	-27	-19	mV
	Output DC regulation(1)	I_{OUT} = 80 mA, V_{VDDIN} = 2V to 3.6V	10	28	48	mV
I_Q	Quescient current(1)	I_{OUT} = 0 mA RUN and SLEEPx modes	88	107	128	µA

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-38. External components requirements in Linear Mode

Symbol	Parameter	Technology	Typ	Units
C_{IN1}	Input regulator capacitor 1		33	nF
C_{IN2}	Input regulator capacitor 2		100	
C_{IN3}	Input regulator capacitor 3		10	µF
C_{OUT1}	Output regulator capacitor 1		100	nF
C_{OUT2}	Output regulator capacitor 2	Tantalum or MLCC 0.5<ESR<10Ω	4.7	µF

Table 9-39. VREG Electrical Characteristics in Switching mode

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VDDIN}	Input voltage range	$V_{VDDCORE}$ = 1.65V, I_{OUT}=50mA	2.0		3.6	V
$V_{VDDCORE}$	DC output voltage (1) Power scaling mode 0 & 2	I_{OUT} = 0 mA	1.75	1.82	1.87	
		I_{OUT} = 50 mA	1.66	1.71	1.79	

Table 9-61. USART3 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		593.9	ns
USPI7	MOSI setup time before SPCK rises		45.93 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		47.03 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			593.38	
USPI10	MOSI setup time before SPCK falls		45.93 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		47.03 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		237.5		
USPI13	NSS hold time after SPCK falls		-1.81		
USPI14	NSS setup time before SPCK falls		237.5		
USPI15	NSS hold time after SPCK rises		-1.81		

Notes: 1. These values are based on simulation. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left(\left\lfloor \frac{t_{SPCK}}{2 \times t_{CLKUSART}} \right\rfloor + \frac{1}{2}\right) \times t_{CLKUSART}$

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, \frac{1}{SPIn})$$

Where $SPIn$ is the MOSI setup and hold time, USPI7 + USPI8 or USPI10 + USPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = MIN(\frac{f_{CLKSPI} \times 2}{9}, f_{PINMAX}, \frac{1}{SPIn + t_{SETUP}})$$

Where $SPIn$ is the MISO delay, USPI6 or USPI9 depending on CPOL and NCPHA. T_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for T_{SETUP} . f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

Where $SPIn$ is the MISO delay, SPI6 or SPI9 depending on CPOL and NCPHA. t_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for t_{SETUP} . f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

9.10.4 TWIM/TWIS Timing

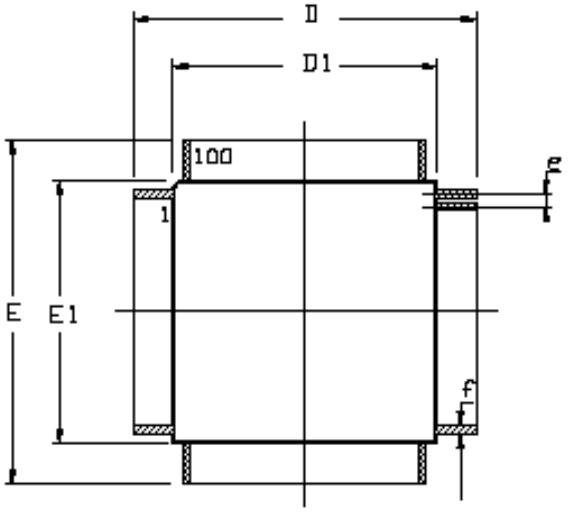
Figure 9-64 shows the TWI-bus timing requirements and the compliance of the device with them. Some of these requirements (t_r and t_f) are met by the device without requiring user intervention. Compliance with the other requirements (t_{HD-STA}, t_{SU-STA}, t_{SU-STO}, t_{HD-DAT}, $t_{SU-DAT-TWI}$, $t_{LOW-TWI}$, t_{HIGH}, and f_{TWCK}) requires user intervention through appropriate programming of the relevant TWIM and TWIS user interface registers. refer to the TWIM and TWIS sections for more information.

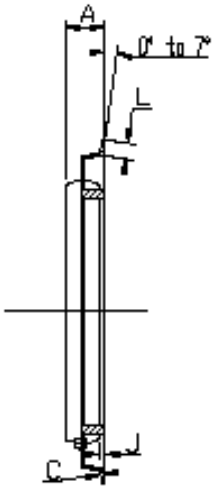
Table 9-64. TWI-Bus Timing Requirements

Symbol	Parameter	Mode	Minimum		Maximum		Unit
			Requirement	Device	Requirement	Device	
t_r	TWCK and TWD rise time	Standard(1)	-		1000		ns
		Fast(1)	$20 + 0.1C_b$		300		
t_f	TWCK and TWD fall time	Standard	-		300		ns
		Fast	$20 + 0.1C_b$		300		
t_{HD-STA}	(Repeated) START hold time	Standard	4	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STA}	(Repeated) START set-up time	Standard	4.7	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STO}	STOP set-up time	Standard	4.0	$4t_{clkpb}$	-		µs
		Fast	0.6				
t_{HD-DAT}	Data hold time	Standard	0.3(2)	$2t_{clkpb}$	3.45()	$15t_{prescaled} + t_{clkpb}$	µs
		Fast			0.9()		
$t_{SU-DAT-TWI}$	Data set-up time	Standard	250	$2t_{clkpb}$	-		ns
		Fast	100				
t_{SU-DAT}		-	-	t_{clkpb}	-		-
$t_{LOW-TWI}$	TWCK LOW period	Standard	4.7	$4t_{clkpb}$	-		µs
		Fast	1.3				
t_{LOW}		-	-	t_{clkpb}	-		-
t_{HIGH}	TWCK HIGH period	Standard	4.0	$8t_{clkpb}$	-		µs
		Fast	0.6				
f_{TWCK}	TWCK frequency	Standard	-		100	$\frac{1}{12t_{clkpb}}$	kHz
		Fast			400		

Notes: 1. Standard mode: $f_{TWCK} \leq 100$ kHz ; fast mode: $f_{TWCK} > 100$ kHz .

Figure 10-2. TQFP-100 Package Drawing





COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

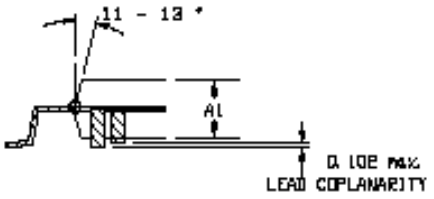


Table 10-5. Device and Package Maximum Weight

500	mg

Table 10-6. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-7. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Table 11-3. ATSAM4LC2 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LC2CA-AU	128	32	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LC2CA-AUR				Reel		
ATSAM4LC2CA-CFU			VFBGA100	Tray		
ATSAM4LC2CA-CFUR				Reel		
ATSAM4LC2BA-AU			TQFP64	Tray		
ATSAM4LC2BA-AUR				Reel		
ATSAM4LC2BA-MU			QFN64	Tray		
ATSAM4LC2BA-MUR				Reel		
ATSAM4LC2BA-UUR			WLCSP64	Reel		
ATSAM4LC2AA-AU			TQFP48	Tray		
ATSAM4LC2AA-AUR				Reel		
ATSAM4LC2AA-MU			QFN48	Tray		
ATSAM4LC2AA-MUR				Reel		

Table 11-4. ATSAM4LS8 Sub Serie Ordering Information

Ordering Code	Flash (Kbytes)	RAM (Kbytes)	Package	Conditioning	Package Type	Temperature Operating Range
ATSAM4LS8CA-AU	512	64	TQFP100	Tray	Green	Industrial -40°C to 85°C
ATSAM4LS8CA-AUR				Reel		
ATSAM4LS8CA-CFU			VFBGA100	Tray		
ATSAM4LS8CA-CFUR				Reel		
ATSAM4LS8BA-AU			TQFP64	Tray		
ATSAM4LS8BA-AUR				Reel		
ATSAM4LS8BA-MU			QFN64	Tray		
ATSAM4LS8BA-MUR				Reel		
ATSAM4LS8BA-UUR			WLCSP64	Reel		
ATSAM4LS8AA-MU			QFN48	Tray		
ATSAM4LS8AA-MUR				Reel		

13. Datasheet Revision History

Note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

13.1 Rev. A – 09/12

1. Initial revision.

13.2 Rev. B – 10/12

1. Fixed ordering code
2. Changed BOD18CTRL and BOD33CTRL ACTION field from “Reserved” to ‘No action”

13.3 Rev. C – 02/13

1. Fixed ball pitch for VFBGA100 package
2. Added VFBGA100 and WLCSP64 pinouts
3. Added Power Scaling Mode 2 for high frequency support
4. Minor update on several modules chapters
5. Major update on Electrical characteristics
6. Updated errata
7. Fixed GPIO multiplexing pin numbers

13.4 Rev. D – 03/13

1. Removed WLCSP package information
2. Added errata text for detecting whether a part supports PS2 mode or not
3. Removed temperature sensor feature (not supported by production flow)
4. Fixed MUX selection on Positive ADC input channel table
5. Added information about TWI instances capabilities
6. Added some details on errata Corrupted data in flash may happen after flash page write operations.171