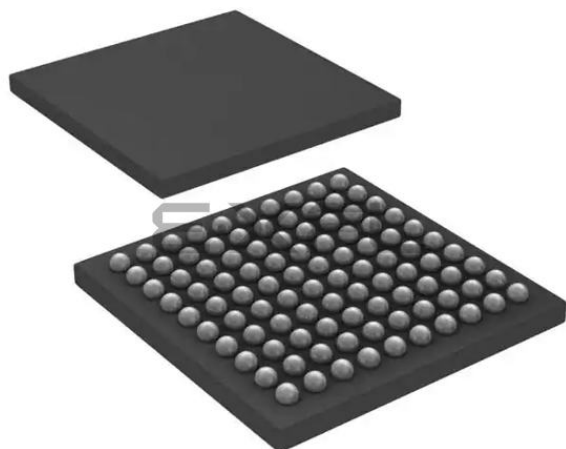




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls8ca-cfu

Table 2-3. ATSAM4LS Configuration Summary

Feature	ATSAM4LS8/4/2C	ATSAM4LS8/4/2B	ATSAM4LS8/4/2A
Timer/Counter Channels	6	3	
Parallel Capture Inputs	8		
Frequency Meter	1		
Watchdog Timer	1		
Power Manager	1		
Glue Logic LUT	2		1
Oscillators	Digital Frequency Locked Loop 20-150MHz (DFLL) Phase Locked Loop 48-240MHz (PLL) Crystal Oscillator 0.6-30MHz (OSC0) Crystal Oscillator 32kHz (OSC32K) RC Oscillator 80MHz (RC80M) RC Oscillator 4,8,12MHz (RCFAST) RC Oscillator 115kHz (RCSYS) RC Oscillator 32kHz (RC32K)		
ADC	15-channel	7-channel	3-channel
DAC	1-channel		
Analog Comparators	4	2	1
CATB Sensors	32	32	26
USB	1		
Audio Bitstream DAC	1		
IIS Controller	1		
Packages	TQFP/VFBGA	TQFP/QFN/ WLCSP	TQFP/QFN

Figure 3-3. ATSAM4LC WLCSP64 Pinout

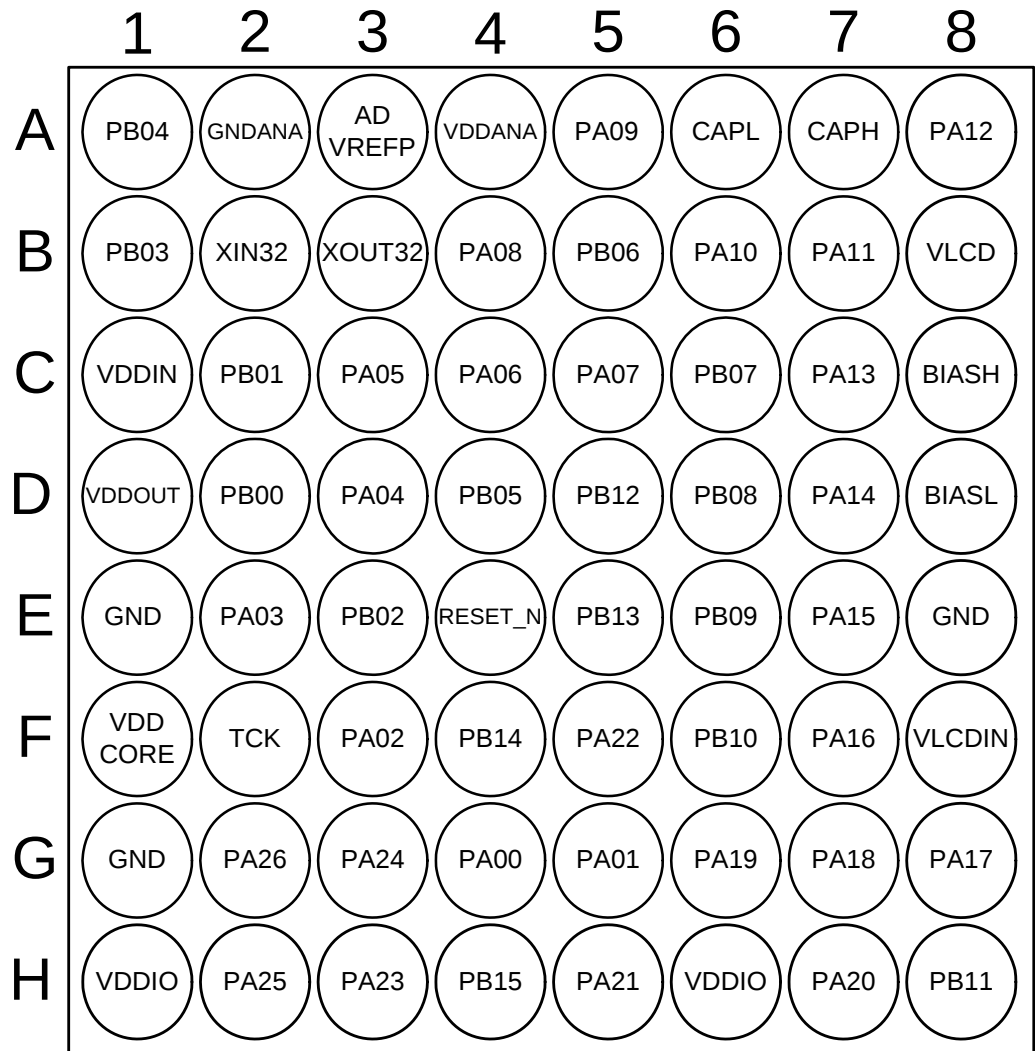


Table 3-3. 64-pin GPIO Controller Function Multiplexing for WLCSP package (Sheet 2 of 3)

ATSAM4L8	ATSAM4L4	Pin	GPIO	Supply	GPIO Functions						
WLCSP	WLCSP				A	B	C	D	E	F	G
H3	H3	PA23	23	LCDC	SPI SCK	TWIMS0 TWD	EIC EXTINT8	GLOC IN3	SCIF GCLK IN0	LCDCA SEG38	CATB DIS
G3	G3	PA24	24	LCDC	SPI NPCS0	TWIMS0 TWCK		GLOC OUT0	SCIF GCLK IN1	LCDCA SEG39	CATB SENSE18
H2	H2	PA25	25	VDDIO	USBC DM	USART2 RXD					CATB SENSE19
G2	G2	PA26	26	VDDIO	USBC DP	USART2 TXD					CATB SENSE20
	A7	PA27	27	LCDA	SPI MISO	IISC ISCK	ABDACB DAC0	GLOC IN4	USART3 RTS		CATB SENSE0
	A6	PA28	28	LCDA	SPI MOSI	IISC ISDI	ABDACB DACN0	GLOC IN5	USART3 CTS		CATB SENSE1
	B8	PA29	29	LCDA	SPI SCK	IISC IWS	ABDACB DAC1	GLOC IN6	USART3 CLK		CATB SENSE2
	E8	PA30	30	LCDA	SPI NPCS0	IISC ISDO	ABDACB DACN1	GLOC IN7	USART3 RXD		CATB SENSE3
	F8	PA31	31	LCDA	SPI NPCS1	IISC IMCK	ABDACB CLK	GLOC OUT1	USART3 TXD		CATB DIS
D2	D2	PB00	32	VDDIN	TWIMS1 TWD	USART0 RXD					CATB SENSE21
C2	C2	PB01	33	VDDIN	TWIMS1 TWCK	USART0 TXD	EIC EXTINT0				CATB SENSE22
E3	E3	PB02	34	VDDANA	ADCIFE AD3	USART1 RTS	ABDACB DAC0	IISC ISCK	ACIFC ACBN0		CATB SENSE23
B1	B1	PB03	35	VDDANA	ADCIFE AD4	USART1 CLK	ABDACB DACN0	IISC ISDI	ACIFC ACBP0		CATB DIS
A1	A1	PB04	36	VDDANA	ADCIFE AD5	USART1 RXD	ABDACB DAC1	IISC ISDO	DACC EXT TRIG0		CATB SENSE24
D4	D4	PB05	37	VDDANA	ADCIFE AD6	USART1 TXD	ABDACB DACN1	IISC IMCK			CATB SENSE25
B5	B5	PB06	38	LCDA	USART3 RTS		GLOC IN4	IISC IWS		LCDCA SEG22	CATB SENSE26
C6	C6	PB07	39	LCDA	USART3 CTS		GLOC IN5	TC0 A0		LCDCA SEG21	CATB SENSE27
D6	D6	PB08	40	LCDA	USART3 CLK		GLOC IN6	TC0 B0		LCDCA SEG14	CATB SENSE28
E6	E6	PB09	41	LCDA	USART3 RXD	PEVC PAD EVT2	GLOC IN7	TC0 A1		LCDCA SEG15	CATB SENSE29
F6	F6	PB10	42	LCDA	USART3 TXD	PEVC PAD EVT3	GLOC OUT1	TC0 B1	SCIF GCLK0	LCDCA SEG16	CATB SENSE30
H8	H8	PB11	43	LCDA	USART0 CTS	SPI NPCS2		TC0 A2	SCIF GCLK1	LCDCA SEG17	CATB SENSE31
D5	D5	PB12	44	LCDC	USART0 RTS	SPI NPCS3	PEVC PAD EVT0	TC0 B2	SCIF GCLK2	LCDCA SEG32	CATB DIS

Table 3-3. 64-pin GPIO Controller Function Multiplexing for WLCSP package (Sheet 3 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
WLCSP	WLCSP				A	B	C	D	E	F	G
E5	E5	PB13	45	LCDC	USART0 CLK	SPI NPCS1	PEVC PAD EVT1	TC0 CLK0	SCIF GCLK3	LCDCA SEG33	CATB SENSE0
F4	F4	PB14	46	LCDC	USART0 RXD	SPI MISO	TWIM3 TWD	TC0 CLK1	SCIF GCLK IN0	LCDCA SEG36	CATB SENSE1
H4	H4	PB15	47	LCDC	USART0 TXD	SPI MOSI	TWIM3 TWCK	TC0 CLK2	SCIF GCLK IN1	LCDCA SEG37	CATB SENSE2

Memory	Start Address	Size
		ATSAM4Lx8
AESA	0x400B0000	256 bytes
Peripheral Bridge C	0x400E0000	64Kbytes
Peripheral Bridge D	0x400F0000	64Kbytes

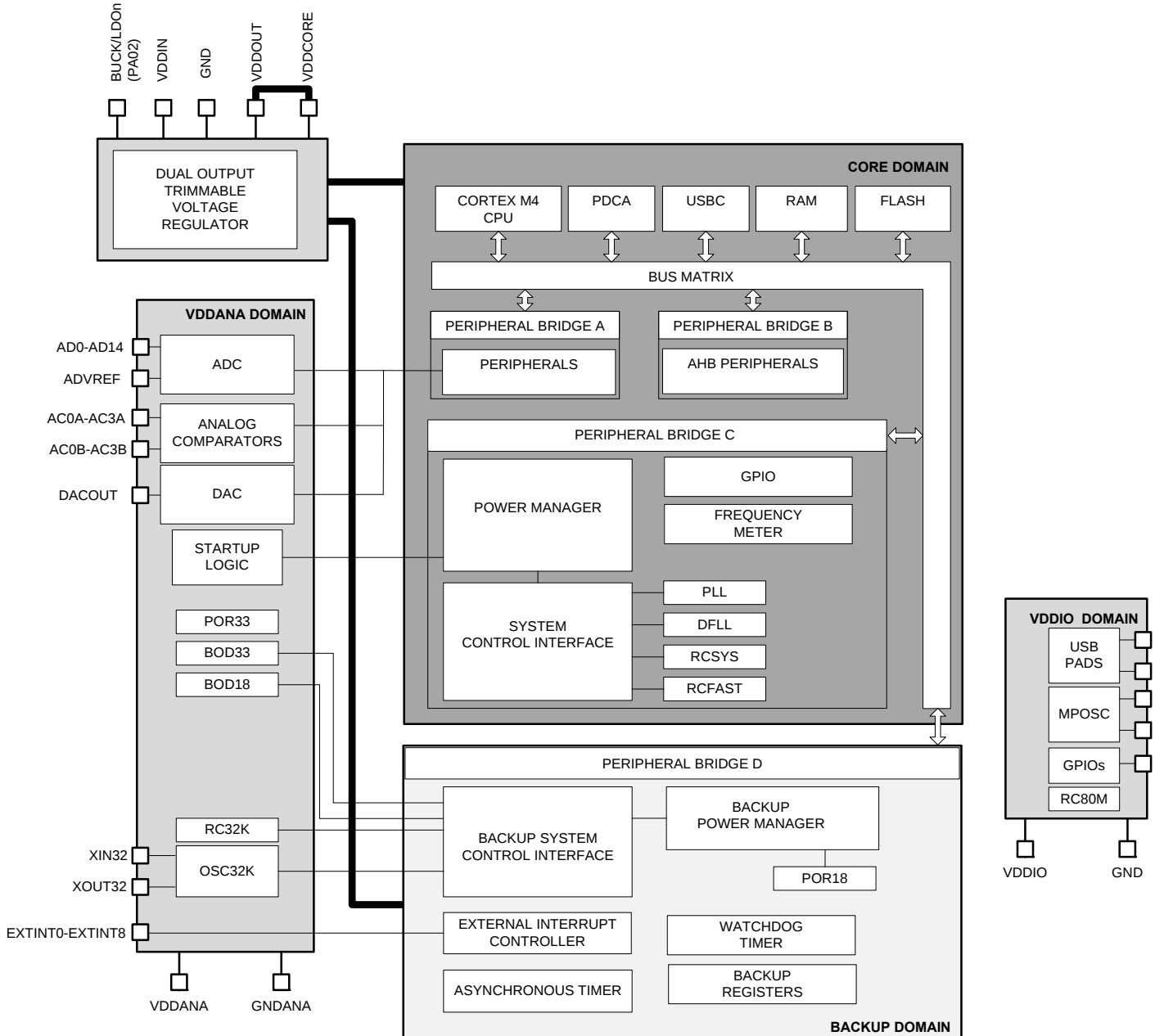
Table 5-2. Flash Memory Parameters

Device	Flash Size (<i>FLASH_PW</i>)	Number of Pages (<i>FLASH_P</i>)	Page Size (<i>FLASH_W</i>)
ATSAM4Lx8	512Kbytes	1024	512 bytes
ATSAM4Lx4	256Kbytes	512	512 bytes
ATSAM4Lx2	128Kbytes	256	512 bytes

6. Power and Startup Considerations

6.1 Power Domain Overview

Figure 6-1. ATSAM4LS Power Domain Diagram

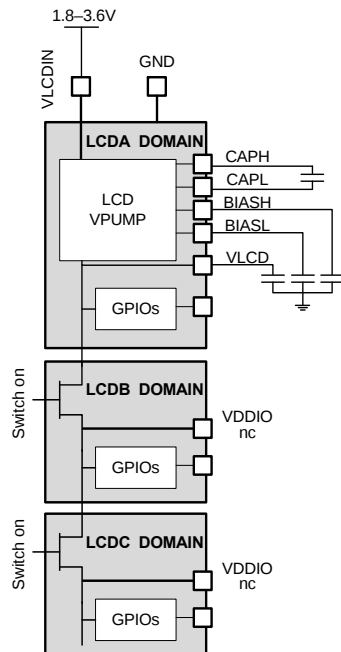


connected to an external voltage source (1.8-3.6V). LCDB cluster is not available in 64 and 48 pin packages

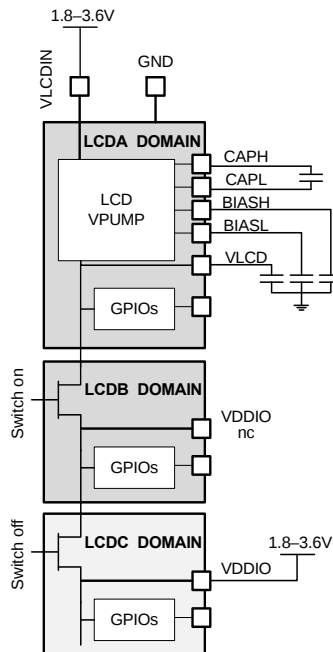
Table 6-1. LCD powering when using the internal voltage pump

Package	Segments in use	VDDIO LCDB	VDDIO LCDC
100-pin packages	[1,24]	1.8-3.6V	1.8-3.6V
	[1, 32]	nc	1.8-3.6V
	[1, 40]	nc	nc
64-pin packages	[1,15]	-	1.8-3.6V
	[1, 23]	-	nc
48-pin packages	[1,9]	-	1.8-3.6V
	[1,13]	-	nc

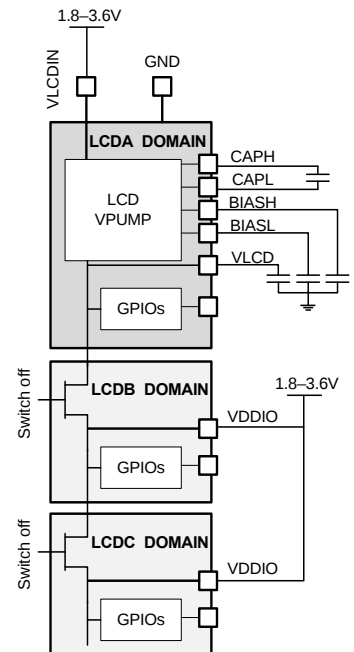
Up to 4x40 segments
No GPIO in LCD clusters



Up to 4x32 segments
Up to 8 GPIOs in LCDC clusters



Up to 4x24 segments
Up to 16 GPIOs in LCDB & LCDC clusters



mechanism can be useful for applications that only require the processor to run when an interrupt occurs.

Before entering the SLEEP mode, the user must configure:

- the SLEEP mode configuration field (BPM.PMCON.SLEEP), Refer to [Table 7-1](#).
- the SCR.SLEEPDEEP bit to 0. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- the BPM.PMCON.RET bit to 0.
- the BPM.PMCON.BKUP bit to 0.

7.1.1.2 Exiting SLEEP mode

The NVIC wakes the system up when it detects any non-masked interrupt with sufficient priority to cause exception entry. The system goes back to the RUN mode from which the SLEEP mode was entered. The CPU and affected modules are restarted. Note that even if an interrupt is enabled in SLEEP mode, it will not trigger if the source module is not clocked.

7.1.2 WAIT Mode and RETENTION Mode

The WAIT and RETENTION modes allow achieving very low power consumption while maintaining the Core domain powered-on. Internal SRAM and registers contents of the Core domain are preserved.

In these modes, all clocks are stopped except the 32kHz clocks (OSC32K, RC32K) which are kept running if enabled.

In RETENTION mode, the SleepWalking feature is not supported and must not be used.

7.1.2.1 Entering WAIT or RETENTION Mode

The WAIT or RETENTION modes are entered by executing the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 0.
- set the BPM.PMCON.RET bit to RETENTION or WAIT mode.

SLEEPONEXIT feature is also available. See ["Entering SLEEP mode" on page 56](#).

7.1.2.2 Exiting WAIT or RETENTION Mode

In WAIT or RETENTION modes, synchronous clocks are stopped preventing interrupt sources from triggering. To wakeup the system, asynchronous wake up sources (AST, EIC, USBC ...) should be enabled in the peripheral (refer to the documentation of the peripheral). The PM.AWEN (Asynchronous Wake Up Enable) register should also be enabled for all peripheral except for EIC and AST.

When the enabled asynchronous wake up event occurs and the system is waken-up, it will generate either:

- an interrupt on the PM WAKE interrupt line if enabled (Refer to [Section 9. "Power Manager \(PM\)" on page 677](#)). In that case, the PM.WCAUSE register indicates the wakeup source.
- or an interrupt directly from the peripheral if enabled (Refer to the section of the peripheral).

When waking up, the system goes back to the RUN mode from which the WAIT or RETENTION mode was entered.

7.1.3 BACKUP Mode

The BACKUP mode allows achieving the lowest power consumption possible in a system which is performing periodic wake-ups to perform tasks but not requiring fast startup time.

The Core domain is powered-off. The internal SRAM and register contents of the Core domain are lost. The Backup domain is kept powered-on. The 32kHz clock (RC32K or OSC32K) is kept running if enabled to feed modules that require clocking.

In BACKUP mode, the configuration of the I/O lines is preserved. Refer to [Section 9. "Backup Power Manager \(BPM\)" on page 677](#) to have more details.

7.1.3.1 Entering BACKUP Mode

The Backup mode is entered by using the WFI instruction with the following settings:

- set the SCR.SLEEPDEEP bit to 1. (See the Power Management section in the ARM Cortex-M4 Processor chapter).
- set the BPM.PSAVE.BKUP bit to 1.

7.1.3.2 Exiting BACKUP Mode

Exit from BACKUP mode happens if a reset occurs or if an enabled wake up event occurs.

The reset sources are:

- BOD33 reset
- BOD18 reset
- WDT reset
- External reset in RESET_N pin

The wake up sources are:

- EIC lines (level transition only)
- BOD33 interrupt
- BOD18 interrupt
- AST alarm, periodic, overflow
- WDT interrupt

The RC32K or OSC32K should be used as clock source for modules if required. The PMCON.CK32S is used to select one of these two 32kHz clock sources.

Exiting the BACKUP mode is triggered by:

- a reset source: an internal reset sequence is performed according to the reset source. Once VDDCORE is stable and has the correct value according to RUN0 mode, the internal reset is released and program execution starts. The corresponding reset source is flagged in the Reset Cause register (RCAUSE) of the PM.
- a wake up source: the Backup domain is not reset. An internal reset is generated to the Core domain, and the system switches back to the previous RUN mode. Once VDDCORE is stable and has the correct value, the internal reset in the Core domain is released and program execution starts. The BKUP bit is set in the Reset Cause register (RCAUSE) of the PM. It allows the user to discriminate between the reset cause and a wake up cause from the BACKUP mode. The wake up cause can be found in the Backup Wake up Cause register (BPM.BKUPWCAUSE).

8.7.14.4 CLAMP

This instruction selects the Bypass register as Data Register. The device output pins are driven from the boundary-scan chain.

Starting in Run-Test/Idle, the CLAMP instruction is accessed the following way:

1. Select the IR Scan path.
2. In Capture-IR: The IR output value is latched into the shift register.
3. In Shift-IR: The instruction register is shifted by the TCK input.
4. In Update-IR: The data from the boundary-scan chain is applied to the output pins.
5. Return to Run-Test/Idle.
6. Select the DR Scan path.
7. In Capture-DR: A logic '0' is loaded into the Bypass Register.
8. In Shift-DR: Data is scanned from TDI to TDO through the Bypass register.
9. Return to Run-Test/Idle.

Table 8-8. CLAMP Details

Instructions	Details
IR input value	0101 (0x5)
IR output value	p00s
DR Size	1
DR input value	x
DR output value	x

8.9.11.5 Length Register

Name: LENGTH
Access Type: Read/Write
Offset: 0x10
Reset Value: 0x00000000

31	30	29	28	27	26	25	24
LENGTH							
23	22	21	20	19	18	17	16
LENGTH							
15	14	13	12	11	10	9	8
LENGTH							
7	6	5	4	3	2	1	0
LENGTH						-	-

- **LENGTH:** Length Value, Bits 1-0 are always zero

9. Electrical Characteristics

9.1 Absolute Maximum Ratings*

Table 9-1. Absolute Maximum Ratings

Operating temperature	-40°C to +85°C
Storage temperature	-60°C to +150°C
Voltage on input pins with respect to ground	-0.3V to $V_{VDD}^{(1)}+0.3V$
Total DC output current on all I/O pins VDDIO	120 mA
Total DC output current on all I/O pins VDDIN	100 mA
Total DC output current on all I/O pins VDDANA	50 mA
Maximum operating voltage VDDIO, VDDIN	3.6V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO} , depending on the supply for the pin. Refer to [Section 3-5 on page 13](#) for details

9.2 Operating Conditions

All the electrical characteristics are applicable to the following conditions unless otherwise specified :

- operating voltage range 1,68V to 3,6V for VDDIN, VDDIO & VDDANA
- Power Scaling 0 and 2 modes
- operating temperature range: $T_A = -40^{\circ}\text{C}$ to 85°C and for a junction temperature up to $T_J = 100^{\circ}\text{C}$.

Typical values are base on $T_A = 25^{\circ}\text{C}$ and $V_{VDDIN}, V_{VDDIO}, V_{VDDANA} = 3,3V$ unless otherwise specified

9.3 Supply Characteristics

Table 9-2. Supply Characteristics

Symbol	Conditions	Voltage		
		Min	Max	Unit
V_{VDDIO} , V_{VDDIN} , V_{VDDANA}	PS1 (FCPU $\leq$ 12MHz) Linear mode	1.68	3.6	V
	PS0 & PS2 (FCPU $>$ 12MHz) Linear mode	1.8		
	Switching mode	2.0 ⁽¹⁾		

1. Below 2.3V, linear mode is more power efficient than switching mode.

Refer to [Section 6. "Power and Startup Considerations" on page 46](#) for details about Power Supply

- All other peripheral clocks stopped
- I/Os are inactive with internal pull-up
- CPU is running on flash with 1 wait state
- Low power cache enabled
- BOD18 and BOD33 disabled

Table 9-8. ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 1

Mode	Conditions	T _A	Typical Wakeup Time	Typ	Max ⁽¹⁾	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	205	224	μA/MHz
		85°C		212	231	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	213	244	
		85°C		230	270	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	95	112	
		85°C		100	119	
SLEEP0	Switching mode	25°C	9 * Main clock cycles	527	627	μA
		85°C		579	739	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	369	445	
		85°C		404	564	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	305	381	
		85°C		334	442	
SLEEP3	Linear mode	25°C		46	55	
WAIT	OSC32K and AST running Fast wake-up enable		1.5μs	4.7	7.5	
	OSC32K and AST stopped Fast wake-up enable			3.5	6.3	
RETENTION	OSC32K running AST running at 1kHz		1.5μs	2.6	4.8	
	AST and OSC32K stopped			1.5	4	
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

- Operating conditions, internal core supply (Figure 9-2)
 - $V_{DDIN} = 3.3V$
 - $V_{DDCORE} = 1.2V$, supplied by the internal regulator in switching mode
- $T_A = 25^{\circ}C$
- Oscillators
 - OSC0 (crystal oscillator) stopped
 - OSC32K (32KHz crystal oscillator) running with external 32KHz crystal
 - RCFAST running @ 12MHz
- Clocks
 - RCFAST used as main clock source
 - CPU, AHB, and PB clocks undivided
- I/Os are inactive with internal pull-up
- Flash enabled in normal mode
- CPU in SLEEP0 mode
- BOD18 and BOD33 disabled

Consumption active is the added current consumption when the module clock is turned on

Table 9-46. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDDANA	Supply voltage ⁽¹⁾		1.6		3.6	V
	Reference range ⁽²⁾	Differential mode	1.0		VDDANA -0.6	V
		Unipolar and Window modes	1.0		1.0	
		Using divide by two function (differential)	2.0		VDDANA	
	Absolute min, max input voltage ⁽²⁾		-0.1		VDDANA +0.1	V
	Start up time ⁽²⁾	ADC with reference already enabled		12	24	Cycles
		No gain compensation Reference buffer			5	μs
		Gain compensation Reference buffer			60	Cycles
R _{SAMPLE}	Input channel source resistance ⁽²⁾				0.5	kΩ
C _{SAMPLE}	Sampling capacitance ⁽²⁾		2.9	3.6	4.3	pF
	Reference input source resistance ⁽²⁾	Gain compensation			2	kΩ
		No gain compensation			1	MΩ
	ADC reference settling time ⁽²⁾	After changing reference/mode ⁽³⁾		5	60	Cycles

1. These values are based on characterization. These values are not covered by test limits in production
2. These values are based on simulation. These values are not covered by test limits in production
3. Requires refresh/flush otherwise conversion time (latency) + 1

Table 9-47. Differential mode, gain=1

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Accuracy without compensation ⁽¹⁾			7		ENOB
	Accuracy after compensation ⁽¹⁾	(INL, gain and offset)			11	ENOB
INL	Integral Non Linearity ⁽²⁾	After calibration, Gain compensation		1.2	1.7	LSBs
DNL	Differential Non Linearity ⁽²⁾	After calibration		0.7	1.0	LSBs
	Gain error ⁽²⁾	External reference	-5.0	-1.0	5.0	mV
		VDDANA/1.6	-40		40	
		VDDANA/2.0	-40		40	
		Bandgap After calibration	-30		30	
	Gain error drift vs voltage ⁽¹⁾	External reference	-2		2	mV/V
	Gain error drift vs temperature ⁽¹⁾	After calibration + bandgap drift If using onchip bandgap			0.08	mV/°K
	Offset error ⁽²⁾	External reference	-5.0		5.0	mV
		VDDANA/1.6	-10		10	
		VDDANA/2.0	-10		10	
		Bandgap After calibration	-10		10	
	Offset error drift vs voltage ⁽¹⁾		-4		4	mV/V

Table 9-50. Analog Comparator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Hysteresis ⁽¹⁾	$V_{ACREFN} = 0.1V$ to $VDDIO - 0.1V$, hysteresis = 1 ⁽²⁾ Fast mode	10		55	mV
		$V_{ACREFN} = 0.1V$ to $VDDIO - 0.1V$, hysteresis = 1 ⁽²⁾ Low power mode	10		68	mV
		$V_{ACREFN} = 0.1V$ to $VDDIO - 0.1V$, hysteresis = 2 ⁽²⁾ Fast mode	26		83	mV
		$V_{ACREFN} = 0.1V$ to $VDDIO - 0.1V$, hysteresis = 2 ⁽²⁾ Low power mode	19		91	mV
		$V_{ACREFN} = 0.1V$ to $VDDIO - 0.1V$, hysteresis = 3 ⁽²⁾ Fast mode	43		106	mV
		$V_{ACREFN} = 0.1V$ to $VDDIO - 0.1V$, hysteresis = 3 ⁽²⁾ Low power mode	32		136	mV
	Propagation delay ⁽¹⁾	Changes for $V_{ACM} = VDDIO/2$ 100mV Overdrive Fast mode			67	ns
		Changes for $V_{ACM} = VDDIO/2$ 100mV Overdrive Low power mode			315	ns
$t_{STARTUP}$	Startup time ⁽¹⁾	Enable to ready delay Fast mode			1.19	μs
		Enable to ready delay Low power mode			3.61	μs
I_{AC}	Channel current consumption ⁽³⁾	Low power mode, no hysteresis		4.9	8.7	μA
		Fast mode, no hysteresis		63	127	

1. These values are based on characterization. These values are not covered by test limits in production
2. HYSTAC.CONFN.HYS field, refer to the Analog Comparator Interface chapter
3. These values are based on simulation. These values are not covered by test limits in production or characterization

9.9.7 Liquid Crystal Display Controller characteristics

Table 9-51. Liquid Crystal Display Controller characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SEG	Segment Terminal Pins				40	
COM	Common Terminal Pins				4	
f_{Frame}	LCD Frame Frequency	F_{CLKLCD}	31.25		512	Hz
C_{Flying}	Flying Capacitor			100		nF
V_{LCD}	LCD Regulated Voltages ⁽¹⁾ CFG.FCST=0	$C_{Flying} = 100nF$ 100nF on V_{LCD} , BIAS2 and BIAS1 pins		3		V
BIAS2				$2 \cdot V_{LCD}/3$		
BIAS1				$V_{LCD}/3$		

1. These values are based on simulation. These values are not covered by test limits in production or characterization

9.9.7.1 Liquid Crystal Controller supply current

The values in [Table 9-52](#) are measured values of power consumption under the following conditions, except where noted:

- T=25°C, WAIT mode, Low power waveform, Frame Rate = 32Hz from OSC32K
- Configuration: 4COMx40SEG, 1/4 Duty, 1/3 Bias, No animation
- All segments on, Load = 160 x 22pF between each COM and each SEG.
- LCDCA current based on $I_{LCD} = I_{WAIT}(Lcd\ On) - I_{WAIT}(Lcd\ Off)$

Table 9-52. Liquid Crystal Display Controller supply current

Symbol	Conditions	Min	Typ	Max	Units
I_{LCD}	Internal voltage generation CFG.FCST=0	$V_{VDDIN} = 3.6V$	8.85		μA
		$V_{VDDIN} = 1.8V$	6.16		
	External bias $V_{LCD}=3.0V$	$V_{VDDIN} = 3.3V$	0.98		
		$V_{VDDIN} = 1.8V$	1.17		

Maximum SPI Frequency, Master Output

The maximum SPI master output frequency is given by the following formula:

$$f_{SPCKMAX} = \text{MIN}(f_{PINMAX}, \frac{1}{SPI_{in}}, \frac{f_{CLKSPI} \times 2}{9})$$

Where SPI_{in} is the MOSI delay, USPI2 or USPI5 depending on CPOL and NCPHA. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Master Input

The maximum SPI master input frequency is given by the following formula:

$$f_{SPCKMAX} = \text{MIN}(\frac{1}{SPI_{in} + t_{VALID}}, \frac{f_{CLKSPI} \times 2}{9})$$

Where SPI_{in} is the MISO setup and hold time, USPI0 + USPI1 or USPI3 + USPI4 depending on CPOL and NCPHA. t_{VALID} is the SPI slave response time. refer to the SPI slave datasheet for $t_{VALID} \cdot f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

9.10.2.2 Slave mode

Figure 9-9. USART in SPI Slave Mode with (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

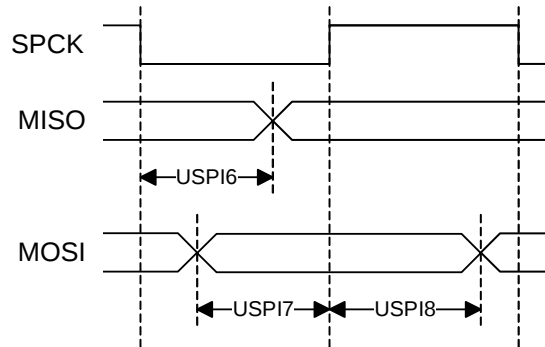


Table 9-61. USART3 in SPI mode Timing, Slave Mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V _{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		593.9	ns
USPI7	MOSI setup time before SPCK rises		$45.93 + t_{SAMPLE}^{(2)} + t_{CLK_USART}$		
USPI8	MOSI hold time after SPCK rises		$47.03 - (t_{SAMPLE}^{(2)} + t_{CLK_USART})$		
USPI9	SPCK rising to MISO delay			593.38	
USPI10	MOSI setup time before SPCK falls		$45.93 + (t_{SAMPLE}^{(2)} + t_{CLK_USART})$		
USPI11	MOSI hold time after SPCK falls		$47.03 - (t_{SAMPLE}^{(2)} + t_{CLK_USART})$		
USPI12	NSS setup time before SPCK rises		237.5		
USPI13	NSS hold time after SPCK falls		-1.81		
USPI14	NSS setup time before SPCK falls		237.5		
USPI15	NSS hold time after SPCK rises		-1.81		

Notes: 1. These values are based on simulation. These values are not covered by test limits in production.

2. Where: $t_{SAMPLE} = t_{SPCK} - \left(\left\lfloor \frac{t_{SPCK}}{2 \times t_{CLK_USART}} \right\rfloor + \frac{1}{2} \right) \times t_{CLK_USART}$

Maximum SPI Frequency, Slave Input Mode

The maximum SPI slave input frequency is given by the following formula:

$$f_{SPCKMAX} = \min\left(\frac{f_{CLKSPI} \times 2}{9}, \frac{1}{SPI_{In}}\right)$$

Where SPI_{In} is the MOSI setup and hold time, USPI7 + USPI8 or USPI10 + USPI11 depending on CPOL and NCPHA. f_{CLKSPI} is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock.

Maximum SPI Frequency, Slave Output Mode

The maximum SPI slave output frequency is given by the following formula:

$$f_{SPCKMAX} = \min\left(\frac{f_{CLKSPI} \times 2}{9}, f_{PINMAX} \cdot \frac{1}{SPI_{In} + t_{SETUP}}\right)$$

Where SPI_{In} is the MISO delay, USPI6 or USPI9 depending on CPOL and NCPHA. T_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for $T_{SETUP} \cdot f_{CLKSPI}$ is the maximum frequency of the CLK_SPI. Refer to the SPI chapter for a description of this clock. f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

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