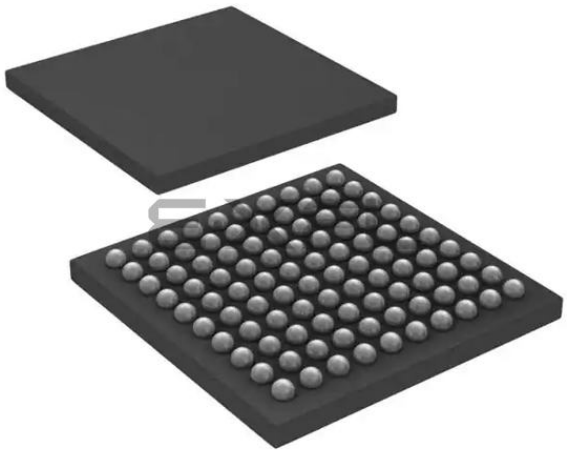

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	80
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.68V ~ 3.6V
Data Converters	A/D 15x12b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-VFBGA
Supplier Device Package	100-VFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsam4ls8ca-cfur

3.1.2 ATSAM4LSx Pinout

Figure 3-6. ATSAM4LS TQFP100 Pinout

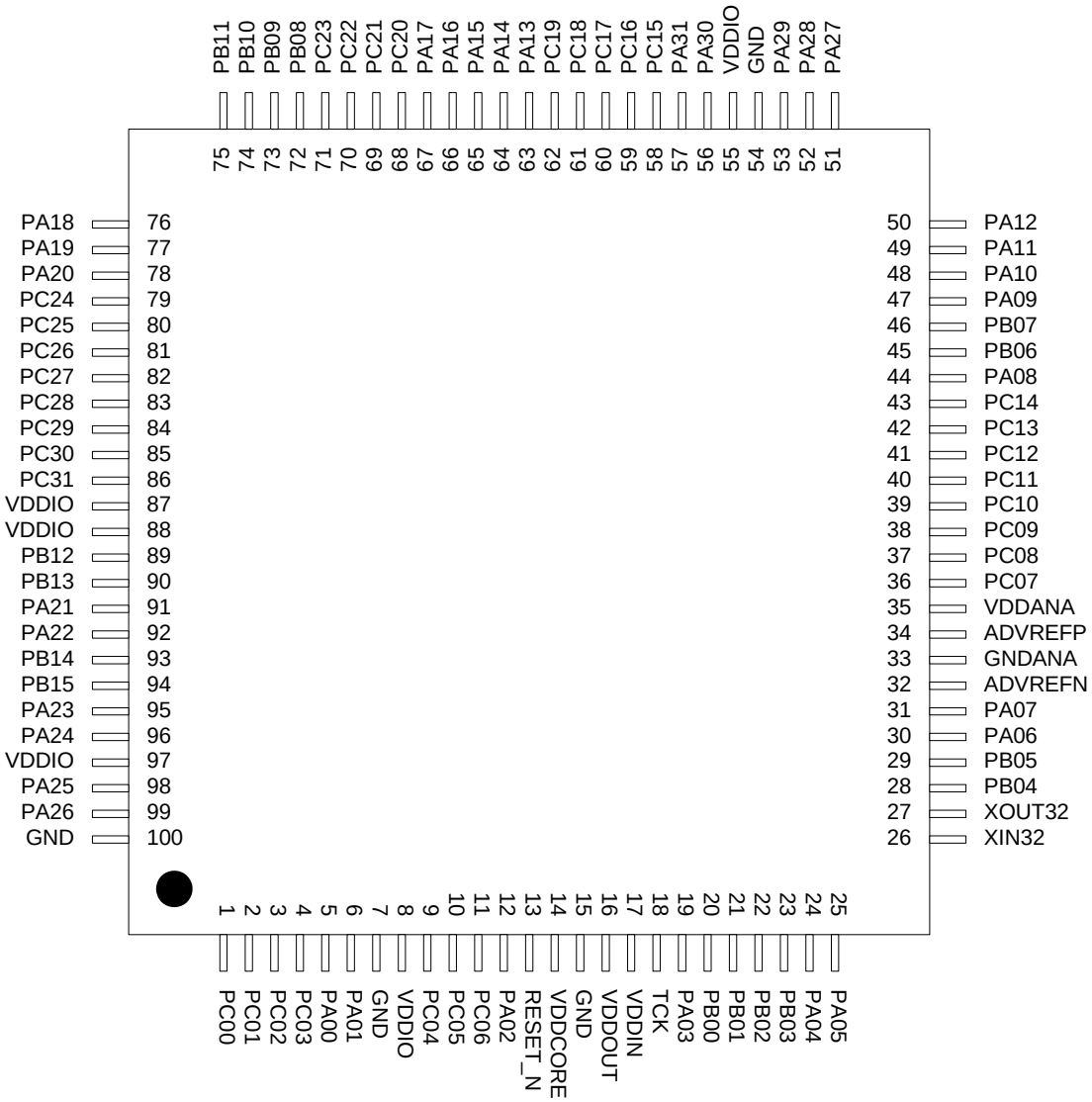


Figure 3-8. ATSAM4LS WLCSP64 Pinout

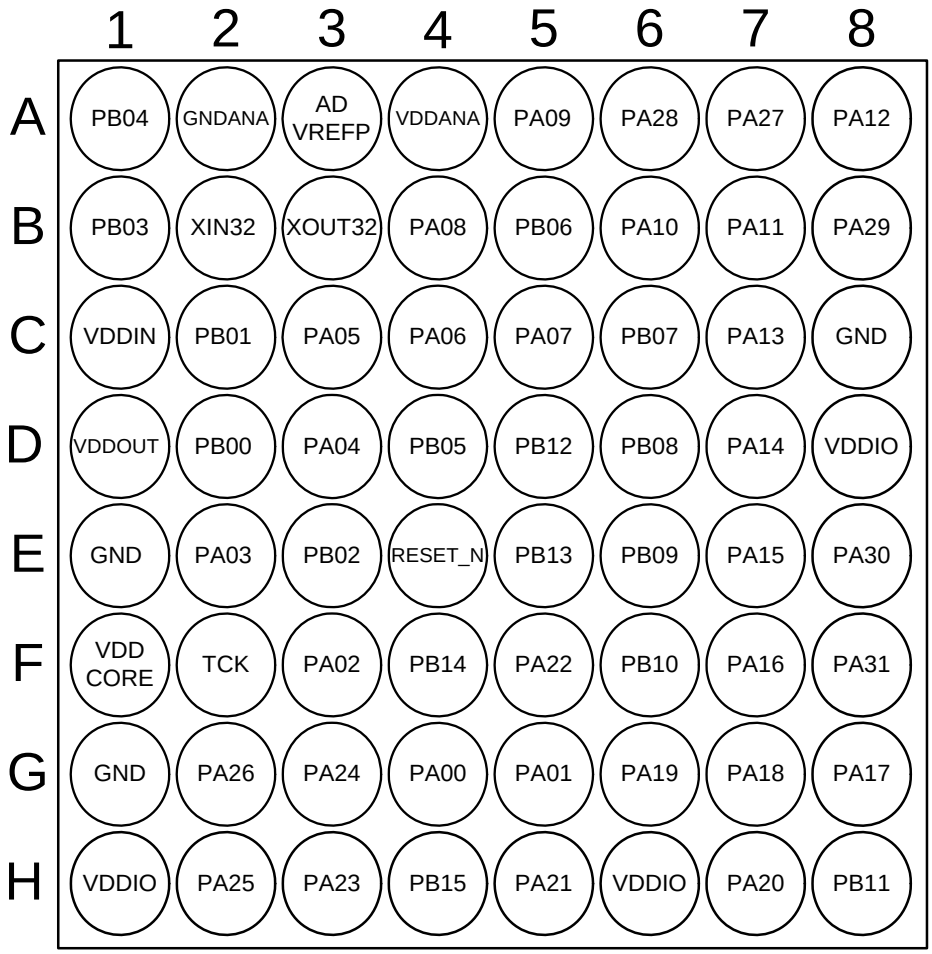


Table 3-3. 64-pin GPIO Controller Function Multiplexing for WLCSP package (Sheet 1 of 3)

ATSAM4LC	ATSAM4LS	Pin	GPIO	Supply	GPIO Functions						
WLCSP	WLCSP				A	B	C	D	E	F	G
G4	G4	PA00	0	VDDIO							
G5	G5	PA01	1	VDDIO							
F3	F3	PA02	2	VDDIN	SCIF GCLK0	SPI NPCS0					CATB DIS
E2	E2	PA03	3	VDDIN		SPI MISO					
D3	D3	PA04	4	VDDANA	ADCIFE AD0	USART0 CLK	EIC EXTINT2	GLOC IN1			CATB SENSE0
C3	C3	PA05	5	VDDANA	ADCIFE AD1	USART0 RXD	EIC EXTINT3	GLOC IN2	ADCIFE TRIGGER		CATB SENSE1
C4	C4	PA06	6	VDDANA	DACC VOUT	USART0 RTS	EIC EXTINT1	GLOC IN0	ACIFC ACAN0		CATB SENSE2
C5	C5	PA07	7	VDDANA	ADCIFE AD2	USART0 TXD	EIC EXTINT4	GLOC IN3	ACIFC ACAP0		CATB SENSE3
B4	B4	PA08	8	LCDA	USART0 RTS	TC0 A0	PEVC PAD EVT0	GLOC OUT0		LCDCA SEG23	CATB SENSE4
A5	A5	PA09	9	LCDA	USART0 CTS	TC0 B0	PEVC PAD EVT1	PARC PCDATA0		LCDCA COM3	CATB SENSE5
B6	B6	PA10	10	LCDA	USART0 CLK	TC0 A1	PEVC PAD EVT2	PARC PCDATA1		LCDCA COM2	CATB SENSE6
B7	B7	PA11	11	LCDA	USART0 RXD	TC0 B1	PEVC PAD EVT3	PARC PCDATA2		LCDCA COM1	CATB SENSE7
A8	A8	PA12	12	LCDA	USART0 TXD	TC0 A2		PARC PCDATA3		LCDCA COM0	CATB DIS
C7	C7	PA13	13	LCDA	USART1 RTS	TC0 B2	SPI NPCS1	PARC PCDATA4		LCDCA SEG5	CATB SENSE8
D7	D7	PA14	14	LCDA	USART1 CLK	TC0 CLK0	SPI NPCS2	PARC PCDATA5		LCDCA SEG6	CATB SENSE9
E7	E7	PA15	15	LCDA	USART1 RXD	TC0 CLK1	SPI NPCS3	PARC PCDATA6		LCDCA SEG7	CATB SENSE10
F7	F7	PA16	16	LCDA	USART1 TXD	TC0 CLK2	EIC EXTINT1	PARC PCDATA7		LCDCA SEG8	CATB SENSE11
G8	G8	PA17	17	LCDA	USART2 RTS	ABDACB DAC0	EIC EXTINT2	PARC PCCK		LCDCA SEG9	CATB SENSE12
G7	G7	PA18	18	LCDA	USART2 CLK	ABDACB DACN0	EIC EXTINT3	PARC PCEN1		LCDCA SEG18	CATB SENSE13
G6	G6	PA19	19	LCDA	USART2 RXD	ABDACB DAC1	EIC EXTINT4	PARC PCEN2	SCIF GCLK0	LCDCA SEG19	CATB SENSE14
H7	H7	PA20	20	LCDA	USART2 TXD	ABDACB DACN1	EIC EXTINT5	GLOC IN0	SCIF GCLK1	LCDCA SEG20	CATB SENSE15
H5	H5	PA21	21	LCDC	SPI MISO	USART1 CTS	EIC EXTINT6	GLOC IN1	TWIM2 TWD	LCDCA SEG34	CATB SENSE16
F5	F5	PA22	22	LCDC	SPI MOSI	USART2 CTS	EIC EXTINT7	GLOC IN2	TWIM2 TWCK	LCDCA SEG35	CATB SENSE17

3.2.4 ITM Trace Connections

If the ITM trace is enabled, the ITM will take control over the pin PA23, irrespectively of the I/O Controller configuration. The Serial Wire Trace signal is available on pin PA23

3.2.5 Oscillator Pinout

The oscillators are not mapped to the normal GPIO functions and their muxings are controlled by registers in the System Control Interface (SCIF) or Backup System Control Interface (BSCIF). Refer to the Section 15. ”System Control Interface (SCIF)” on page 308 and Section 15. ”Backup System Control Interface (BSCIF)” on page 308 for more information about this.

Table 3-7. Oscillator Pinout

48-pin Packages	64-pin QFN/QFP	64-pin WLCSP	100-pin Packages	100-ball VFBGA	Pin Name	Oscillator Pin
1	1	G4	5	B9	PA00	XIN0
13	17	B2	26	B2	XIN32	XIN32
2	2	G5	6	B8	PA01	XOUT0
14	18	B3	27	C2	XOUT32	XOUT32

7.1.4 Wakeup Time

7.1.4.1 Wakeup Time From SLEEP Mode

The latency depends on the clock sources wake up time. If the clock sources are not stopped, there is no latency to wake the clocks up.

7.1.4.2 Wakeup Time From WAIT or RETENTION Mode

The wake up latency consists of:

- the switching time from the low power configuration to the RUN mode power configuration. By default, the switching time is completed when all the voltage regulation system is ready. To speed-up the startup time, the user can set the Fast Wakeup bit in BPM.PMCON register.
- the wake up time of the RC oscillator used to start the system up. By default, the RCSYS oscillator is used to startup the system. The user can use another clock source (RCFAST for example) to speed up the startup time by configuring the PM.FASTWKUP register. Refer to Section 9. ”Power Manager (PM)” on page 677.
- the Flash memory wake up time.

To have the shortest wakeup time, the user should:

- set the BPM.PMCON.FASTWKUP bit.

- configure the PM.FASTSLEEP.FASTRCOSC field to use the RCFAST main clock.

- enter the WAIT or RETENTION mode

Upon a wakeup, this is required to keep the main clock connected to RCFAST until the voltage regulation system is fully ready (when BPM.ISR.PSOK bit is one). During this wakeup period, the FLASHCALW module is automatically configured to operate in “1 wait state mode”.

7.1.4.3 Wake time from BACKUP mode

It is equal to the Core domain logic reset latency (similar to the reset latency caused by an external reset in RESET_N pin) added to the time required for the voltage regulation system to be stabilized.

8.7.12 JTAG Instructions Summary

The implemented JTAG instructions are shown in the table below.

Table 8-2. Implemented JTAG instructions list

IR instruction value	Instruction	Description	availability when protected	Component
b0000	EXTEST	Select boundary-scan chain as data register for testing circuitry external to the device.	yes	BSCAN-TAP
b0001	SAMPLE_PRELOAD	Take a snapshot of external pin values without affecting system operation.	yes	
b0100	INTEST	Select boundary-scan chain for internal testing of the device.	yes	
b0101	CLAMP	Bypass device through Bypass register, while driving outputs from boundary-scan register.	yes	
b1000	ABORT	ARM JTAG-DP Instruction	yes	SWJ-DP (in JTAG mode)
b1010	DPACC	ARM JTAG-DP Instruction	yes	
b1011	APACC	ARM JTAG-DP Instruction	yes	
b1100	-	Reserved	yes	
b1101	-	Reserved	yes	
b1110	IDCODE	ARM JTAG-DP Instruction	yes	
b1111	BYPASS	Bypass this device through the bypass register.	yes	

8.9.9 Unlimited Flash User Page Read Access

The SMAP can access the User page even if the protected state is set. Prior to operate such an access, the user should check that the module is not busy by checking that SR.STATE is equal to zerp. Once the offset of the word to access inside the page is written in ADDR.ADDR, the read operation can be initiated by writing a one in CR.FSPR. The SR.STATE field will indicate the FSPR state. Addresses written to ADDR.ADDR must be world aligned. Failing to do so will result in unpredictable behavior. The result can be read in the DATA register as soon as SR.DONE rises. The ADDR field is used as an offset in the page, bits outside a page boundary will be silently discarded. The ADDR register is automatically incremented at the end of the read operation making possible to dump consecutive words without writing the next offset into ADDR.ADDR.

8.9.10 32-bit Cyclic Redundancy Check (CRC)

The SMAP unit provides support for calculating a Cyclic Redundancy Check (CRC) value for a memory area. The algorithm used is the industry standard CRC32 algorithm using the generator polynomial 0xEDB88320.

8.9.10.1 Starting CRC Calculation

To calculate CRC for a memory range, the start address must be written into the ADDR register, and the size of the memory range into the LENGTH register. Both the start address and the length must be word aligned.

The initial value used for the CRC calculation must be written to the DATA register. This value will usually be 0xFFFFFFFF, but can be e.g. the result of a previous CRC calculation if generating a common CRC of separate memory blocks.

Once completed, the calculated CRC value can be read out of the DATA register. The read value must be inverted to match standard CRC32 implementations, or kept non-inverted if used as starting point for subsequent CRC calculations.

If the device is in protected state, it is only possible to calculate the CRC of the whole flash array. In most cases this area will be the entire onboard nonvolatile memory. The ADDR, LENGTH, and DATA registers will be forced to predefined values once the CRC operation is started, and user-written values are ignored. This allows the user to verify the contents of a protected device.

The actual test is started by writing a one in CR.CRC. A running CRC operation can be cancelled by disabling the module (write a one in CR.DIS). This has the effect of resetting the module. The module has to be restarted by issuing an enable command (write a one in CR.EN).

8.9.10.2 Interpreting the Results

The user should monitor the SR register (Refer to Section 8.9.11.2 ”Status Register” on page 83). When the operation is completed SR.DONE is set. Then the SR.BERR and SR.FAIL must be read to ensure that no bus error nor functional error occured.

8.9.11.1 Control Register

Name: CR

Access Type: Write-Only

Offset: 0x00

Reset Value: 0x00000000

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	-

23	22	21	20	19	18	17	16
-	-	-	-	-	-	-	-

15	14	13	12	11	10	9	8
-	-	-	-	-	-	-	-

7	6	5	4	3	2	1	0
-	-	-	CE	FSPR	CRC	DIS	EN

Writing a zero to a bit in this register has no effect.

- **CE: Chip Erase**
  Writing a one to this bit triggers the FLASH Erase All (EA) operation which clears all volatile memories, the whole flash array, the general purpose fuses and the protected state. The Status register DONE field indicates the completion of the operation.
  Reading this bit always returns 0
- **FSPR: Flash User Page Read**
  Writing a one to this bit triggers a read operation in the User page. The word pointed by the ADDR register in the page is read and written to the DATA register. ADDR is post incremented allowing a burst of reads without modifying ADDR. SR.DONE must be read high prior to reading the DATA register.
  Reading this bit always returns 0
- **CRC: Cyclic Redundancy Code**
  Writing a one triggers a CRC calculation over a memory area defined by the ADDR and LENGTH registers. Reading this bit always returns 0
  Note: This feature is restricted while in protected state
- **DIS: Disable**
  Writing a one to this bit disables the module. Disabling the module resets the whole module immediately.
- **EN: Enable**
  Writing a one to this bit enables the module.

8.9.11.10 Identification Register

Name: IDR

Access Type: Read-Only

Offset: 0xFC

Reset Value: -

31	30	29	28	27	26	25	24
REVISION				CC			

23	22	21	20	19	18	17	16
IC							CLSS

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
APID				APIDV			

- **REVISION: Revision**
- **CC: JEP-106 Continuation Code**
  Atmel continuation code is 0x0
- **IC: JEP-106 Identity Code**
  Atmel identification code is 0x1F
- **CLSS: Class**
  0: This AP is not a Memory Access Port
  1: This AP is a Memory Access Port
- **APID: AP Identification**
- **APIDV: AP Identification Variant**

For more information about this register, refer to the ARM Debug Interface v5.1 Architecture Specification document.

9. Electrical Characteristics

9.1 Absolute Maximum Ratings*

Table 9-1. Absolute Maximum Ratings

Operating temperature ..... -40°C to +85°C
Storage temperature ..... -60°C to +150°C
Voltage on input pins with respect to ground .....-0.3V to V_{VDD} (1)+0.3V
Total DC output current on all I/O pins VDDIO ..... 120 mA
Total DC output current on all I/O pins VDDIN ..... 100 mA
Total DC output current on all I/O pins VDDANA..... 50 mA
Maximum operating voltage VDDIO, VDDIN 3.6V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. V_{VDD} corresponds to either V_{VDDIN} or V_{VDDIO}, depending on the supply for the pin. Refer to Section 3-5 on page 13 for details

9.2 Operating Conditions

All the electrical characteristics are applicable to the following conditions unless otherwise specified :

- operating voltage range 1,68V to 3,6V for VDDIN, VDDIO & VDDANA
- Power Scaling 0 and 2 modes
- operating temperature range: TA = -40°C to 85°C and for a junction temperature up to TJ = 100°C.

Typical values are base on TA = 25°c and VDDIN,VDDIO,VDDANA = 3,3V unless otherwise specified

9.3 Supply Characteristics

Table 9-2. Supply Characteristics

Symbol	Conditions	Voltage		
		Min	Max	Unit
V_{VDDIO}, V_{VDDIN}, V_{VDDANA}	PS1 (FCPU<=12MHz) Linear mode	1.68	3.6	V
	PS0 & PS2 (FCPU>12MHz) Linear mode	1.8		
	Switching mode	2.0 (1)		

1. Below 2.3V, linear mode is more power efficient than switching mode.

Refer to Section 6. ”Power and Startup Considerations” on page 46 for details about Power Supply

Table 9-6. ATSAM4L4/2 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
SLEEP0	Switching mode	25°C	9 * Main clock cycles	3817	4033	µA
		85°C		3934	4174	
SLEEP1	Switching mode	25°C	9 * Main clock cycles + 500ns	2341	2477	
		85°C		2437	2585	
SLEEP2	Switching mode	25°C	9 * Main clock cycles + 500ns	1758	1862	
		85°C		1847	1971	
SLEEP3	Linear mode	25°C		51	60	
WAIT	OSC32K and AST running Fast wake-up enable		1.5µs	5.9	8.7	
	OSC32K and AST stopped Fast wake-up enable			4.7	7.6	
RETENTION	OSC32K running AST running at 1kHz		1.5µs	3.1	5.1	
	AST and OSC32K stopped			2.2	4.2	
BACKUP	OSC32K running AST running at 1kHz			1.5	3.1	
	AST and OSC32K stopped			0.9	1.7	

1. These values are based on characterization. These values are not covered by test limits in production.

Table 9-7. ATSAM4L8 Current consumption and Wakeup time for power scaling mode 0 and 2

Mode	Conditions	T_A	Typical Wakeup Time	Typ	Max (1)	Unit
RUN	CPU running a Fibonacci algorithm Linear mode	25°C	N/A	319	343	µA/MHz
		85°C		326	350	
	CPU running a CoreMark algorithm Linear mode	25°C	N/A	343	387	
		85°C		351	416	
	CPU running a Fibonacci algorithm Switching mode	25°C	N/A	181	198	
		85°C		186	203	
	CPU running a CoreMark algorithm Switching mode	25°C	N/A	192	232	
		85°C		202	239	

9.10 Timing Characteristics

9.10.1 RESET_N Timing

Table 9-53. RESET_N Waveform Parameters [1]

Symbol	Parameter	Conditions	Min	Max	Units
t_{RESET}	RESET_N minimum pulse length		10		ns

1. These values are based on simulation. These values are not covered by test limits in production.

9.10.2 USART in SPI Mode Timing

9.10.2.1 Master mode

Figure 9-7. USART in SPI Master Mode with (CPOL= CPHA= 0) or (CPOL= CPHA= 1)

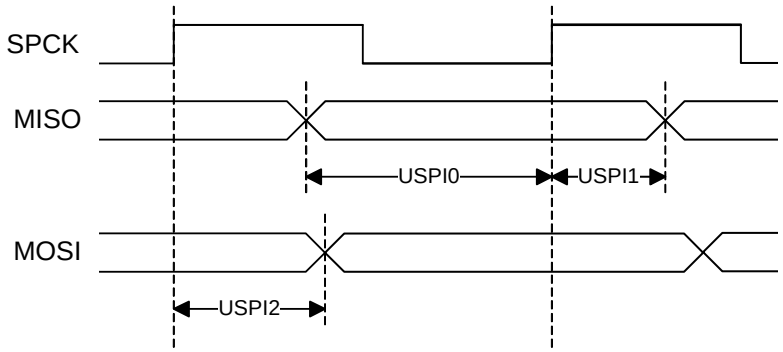


Figure 9-8. USART in SPI Master Mode with (CPOL= 0 and CPHA= 1) or (CPOL= 1 and CPHA= 0)

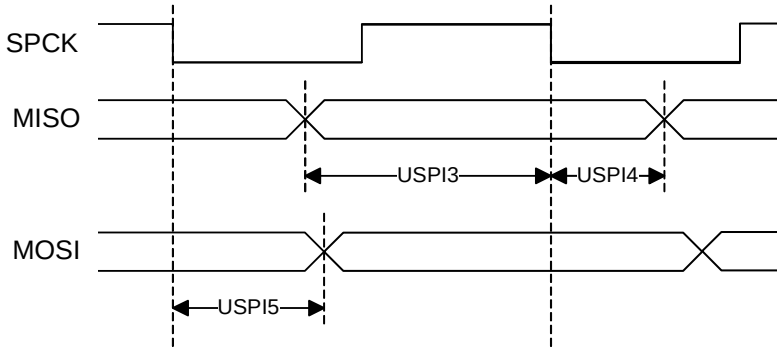


Table 9-59. USART1 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		373.58	ns
USPI7	MOSI setup time before SPCK rises		4.16 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		46.69 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			373.54	
USPI10	MOSI setup time before SPCK falls		4.16 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		46.69 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		200.43		
USPI13	NSS hold time after SPCK falls		-16.5		
USPI14	NSS setup time before SPCK falls		200.43		
USPI15	NSS hold time after SPCK rises		-16.5		

Table 9-60. USART2 in SPI mode Timing, Slave Mode[1]

Symbol	Parameter	Conditions	Min	Max	Units
USPI6	SPCK falling to MISO delay	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF		770.02	ns
USPI7	MOSI setup time before SPCK rises		136.56 + t_{SAMPLE}[2] + t_{CLK_USART}		
USPI8	MOSI hold time after SPCK rises		47.9 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI9	SPCK rising to MISO delay			570.19	
USPI10	MOSI setup time before SPCK falls		136.73 +(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI11	MOSI hold time after SPCK falls		47.9 -(t_{SAMPLE}[2] + t_{CLK_USART})		
USPI12	NSS setup time before SPCK rises		519.87		
USPI13	NSS hold time after SPCK falls		-1.83		
USPI14	NSS setup time before SPCK falls		519.87		
USPI15	NSS hold time after SPCK rises		-1.83		

Where $SPIn$ is the MISO delay, SPI6 or SPI9 depending on CPOL and NCPHA. t_{SETUP} is the SPI master setup time. refer to the SPI master datasheet for t_{SETUP} . f_{PINMAX} is the maximum frequency of the SPI pins. refer to the I/O Pin Characteristics section for the maximum frequency of the pins.

9.10.4 TWIM/TWIS Timing

Figure 9-64 shows the TWI-bus timing requirements and the compliance of the device with them. Some of these requirements (t_r and t_f) are met by the device without requiring user intervention. Compliance with the other requirements (t_{HD-STA}, t_{SU-STA}, t_{SU-STO}, t_{HD-DAT}, $t_{SU-DAT-TWI}$, $t_{LOW-TWI}$, t_{HIGH}, and f_{TWCK}) requires user intervention through appropriate programming of the relevant TWIM and TWIS user interface registers. refer to the TWIM and TWIS sections for more information.

Table 9-64. TWI-Bus Timing Requirements

Symbol	Parameter	Mode	Minimum		Maximum		Unit
			Requirement	Device	Requirement	Device	
t_r	TWCK and TWD rise time	Standard(1)	-		1000		ns
		Fast(1)	$20 + 0.1C_b$		300		
t_f	TWCK and TWD fall time	Standard	-		300		ns
		Fast	$20 + 0.1C_b$		300		
t_{HD-STA}	(Repeated) START hold time	Standard	4	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STA}	(Repeated) START set-up time	Standard	4.7	t_{clkpb}	-		µs
		Fast	0.6				
t_{SU-STO}	STOP set-up time	Standard	4.0	$4t_{clkpb}$	-		µs
		Fast	0.6				
t_{HD-DAT}	Data hold time	Standard	0.3(2)	$2t_{clkpb}$	3.45()	$15t_{prescaled} + t_{clkpb}$	µs
		Fast			0.9()		
$t_{SU-DAT-TWI}$	Data set-up time	Standard	250	$2t_{clkpb}$	-		ns
		Fast	100				
t_{SU-DAT}		-	-	t_{clkpb}	-		-
$t_{LOW-TWI}$	TWCK LOW period	Standard	4.7	$4t_{clkpb}$	-		µs
		Fast	1.3				
t_{LOW}		-	-	t_{clkpb}	-		-
t_{HIGH}	TWCK HIGH period	Standard	4.0	$8t_{clkpb}$	-		µs
		Fast	0.6				
f_{TWCK}	TWCK frequency	Standard	-		100	$\frac{1}{12t_{clkpb}}$	kHz
		Fast			400		

Notes: 1. Standard mode: $f_{TWCK} \leq 100$ kHz ; fast mode: $f_{TWCK} > 100$ kHz .

Table 9-65. JTAG Timings[1]

Symbol	Parameter	Conditions	Min	Max	Units
JTAG0	TCK Low Half-period	V_{VDDIO} from 3.0V to 3.6V, maximum external capacitor = 40pF	21.8		ns
JTAG1	TCK High Half-period		8.6		
JTAG2	TCK Period		30.3		
JTAG3	TDI, TMS Setup before TCK High		2.0		
JTAG4	TDI, TMS Hold after TCK High		2.3		
JTAG5	TDO Hold Time		9.5		
JTAG6	TCK Low to TDO Valid			21.8	
JTAG7	Boundary Scan Inputs Setup Time		0.6		
JTAG8	Boundary Scan Inputs Hold Time		6.9		
JTAG9	Boundary Scan Outputs Hold Time		9.3		
JTAG10	TCK to Boundary Scan Outputs Valid			32.2	

Note: 1. These values are based on simulation. These values are not covered by test limits in production.

9.10.6 SWD Timing

Figure 9-18. SWD Interface Signals

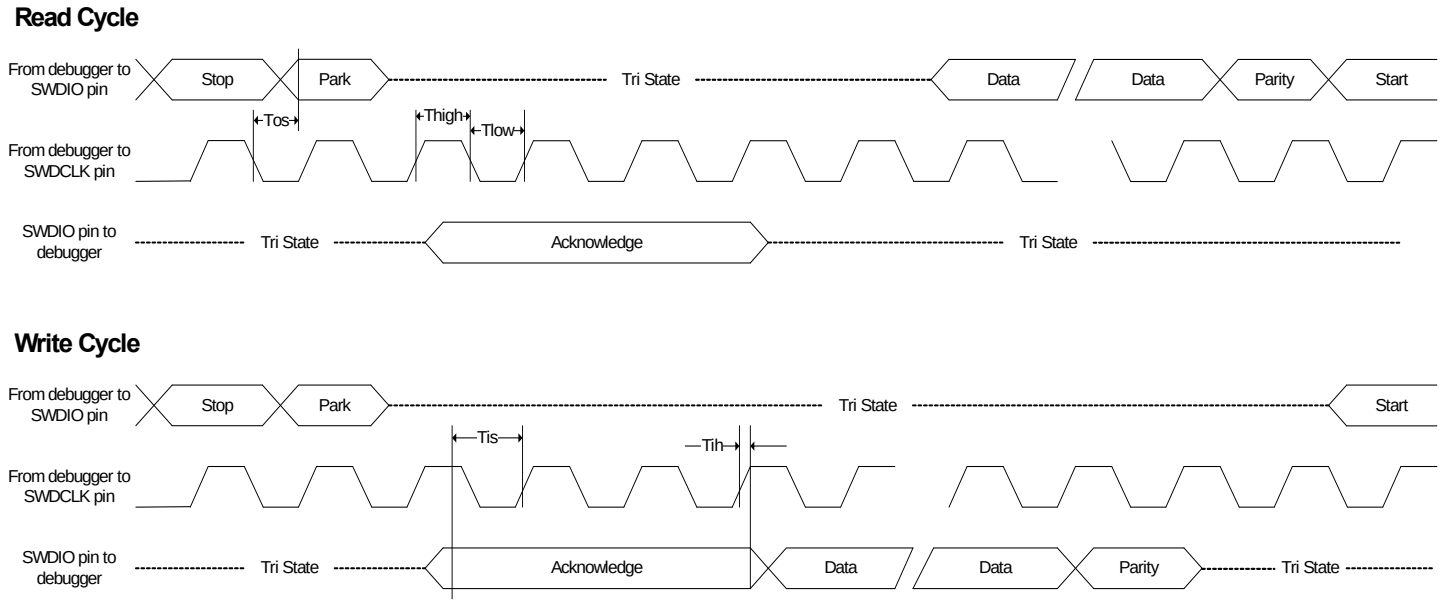


Table 9-66. SWD Timings[1]

Symbol	Parameter	Conditions	Min	Max	Units
Thigh	SWDCLK High period	V_{VDDIO} from 3.0 V to 3.6 V, maximum external capacitor = 40 pF	10	500 000	ns
Tlow	SWDCLK Low period		10	500 000	
Tos	SWDIO output skew to falling edge SWDCLK		-5	5	
Tis	Input Setup time required between SWDIO		4	-	
Tih	Input Hold time required between SWDIO and rising edge SWDCLK		1	-	

Note: 1. These values are based on simulation. These values are not covered by test limits in production or characterization.

10. Mechanical Characteristics

10.1 Thermal Considerations

10.1.1 Thermal Data

Table 10-1 summarizes the thermal resistance data depending on the package.

Table 10-1. Thermal Resistance Data

Symbol	Parameter	Condition	Package	Typ	Unit
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP100	48.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP100	13.3	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	VFBGA100	31.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		VFBGA100	6.9	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	WLCSP64	26.9	°C/W
θ_{JC}	Junction-to-case thermal resistance		WLCSP64	0.2	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP64	49.6	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP64	13.5	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN64	22.0	°C/W
θ_{JC}	Junction-to-case thermal resistance		QFN64	1.3	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	TQFP48	51.1	°C/W
θ_{JC}	Junction-to-case thermal resistance		TQFP48	13.7	
θ_{JA}	Junction-to-ambient thermal resistance	Still Air	QFN48	24.9	°C/W
θ_{JC}	Junction-to-case thermal resistance		QFN48	1.3	

10.1.2 Junction Temperature

The average chip-junction temperature, T_J, in °C can be obtained from the following:

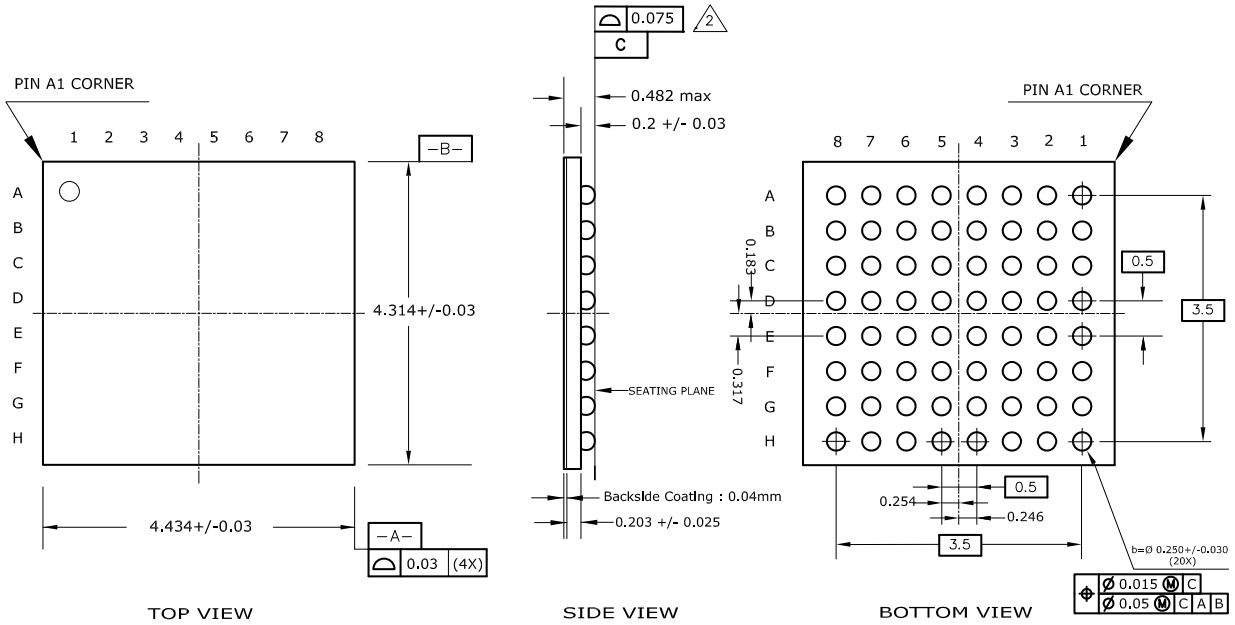
1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:

- θ_{JA} = package thermal resistance, Junction-to-ambient (°C/W), provided in Table 10-1.
- θ_{JC} = package thermal resistance, Junction-to-case thermal resistance (°C/W), provided in Table 10-1.
- $\theta_{HEAT\ SINK}$ = cooling device thermal resistance (°C/W), provided in the device datasheet.
- P_D = device power consumption (W) estimated from data provided in Section 9.5 on page 103.
- T_A = ambient temperature (°C).

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature T_J in °C.

Figure 10-4. WLCSP64 SAM4LS4/2 Package Drawing



COMMON DIMENSIONS
(Unit of Measure = mm)

BALL	SIGNAL	X COORD	Y COORD
A1	PB04	1.746	1.683
A2	GNDANA	1.246	1.683
A3	ADVREFP	0.746	1.683
A4	VDDANA	0.246	1.683
A5	PA09	-0.254	1.683
A6	PA28	-0.754	1.683
A7	PA27	-1.254	1.683
A8	PA12	-1.754	1.683
B1	PB03	1.746	1.183
B2	XIN32	1.246	1.183
B3	XOUT32	0.746	1.183
B4	PA08	0.246	1.183
B5	PB06	-0.254	1.183
B6	PA10	-0.754	1.183
B7	PA11	-1.254	1.183
B8	PA29	-1.754	1.183
C1	VDDIN	1.746	0.683
C2	PB01	1.246	0.683
C3	PA05	0.746	0.683
C4	PA06	0.246	0.683
C5	PA07	-0.254	0.683
C6	PB07	-0.754	0.683

BALL	SIGNAL	X COORD	Y COORD
C7	PA13	-1.254	0.683
C8	GNDIO0	-1.754	0.683
D1	VDDOUT	1.746	0.183
D2	PB00	1.246	0.183
D3	PA04	0.746	0.183
D4	PB05	0.246	0.183
D5	PB12	-0.254	0.183
D6	PB08	-0.754	0.183
D7	PA14	-1.254	0.183
D8	VLCDIN	-1.754	0.183
E1	GNDIN	1.746	-0.317
E2	PA03	1.246	-0.317
E3	PB02	0.746	-0.317
E4	RESET_N	0.246	-0.317
E5	PB13	-0.254	-0.317
E6	PB09	-0.754	-0.317
E7	PA15	-1.254	-0.317
E8	PA30	-1.754	-0.317
F1	VDDCORE	1.746	-0.817
F2	TCK	1.246	-0.817
F3	PA02	0.746	-0.817
F4	PB14	0.246	-0.817

BALL	SIGNAL	X COORD	Y COORD
F5	PA22	-0.254	-0.817
F6	PB10	-0.754	-0.817
F7	PA16	-1.254	-0.817
F8	PA31	-1.754	-0.817
G1	GNDIO1	1.746	-1.317
G2	PA26	1.246	-1.317
G3	PA24	0.746	-1.317
G4	PA00	0.246	-1.317
G5	PA01	-0.254	-1.317
G6	PA19	-0.754	-1.317
G7	PA18	-1.254	-1.317
G8	PA17	-1.754	-1.317
H1	VDDIO1	1.746	-1.817
H2	PA25	1.246	-1.817
H3	PA23	0.746	-1.817
H4	PB15	0.246	-1.817
H5	PA21	-0.254	-1.817
H6	VDDIO0	-0.754	-1.817
H7	PA20	-1.254	-1.817
H8	PB11	-1.754	-1.817

Notes : 1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.

2. Applied to whole wafer.

Table 10-11. Device and Package Maximum Weight

14.8	mg

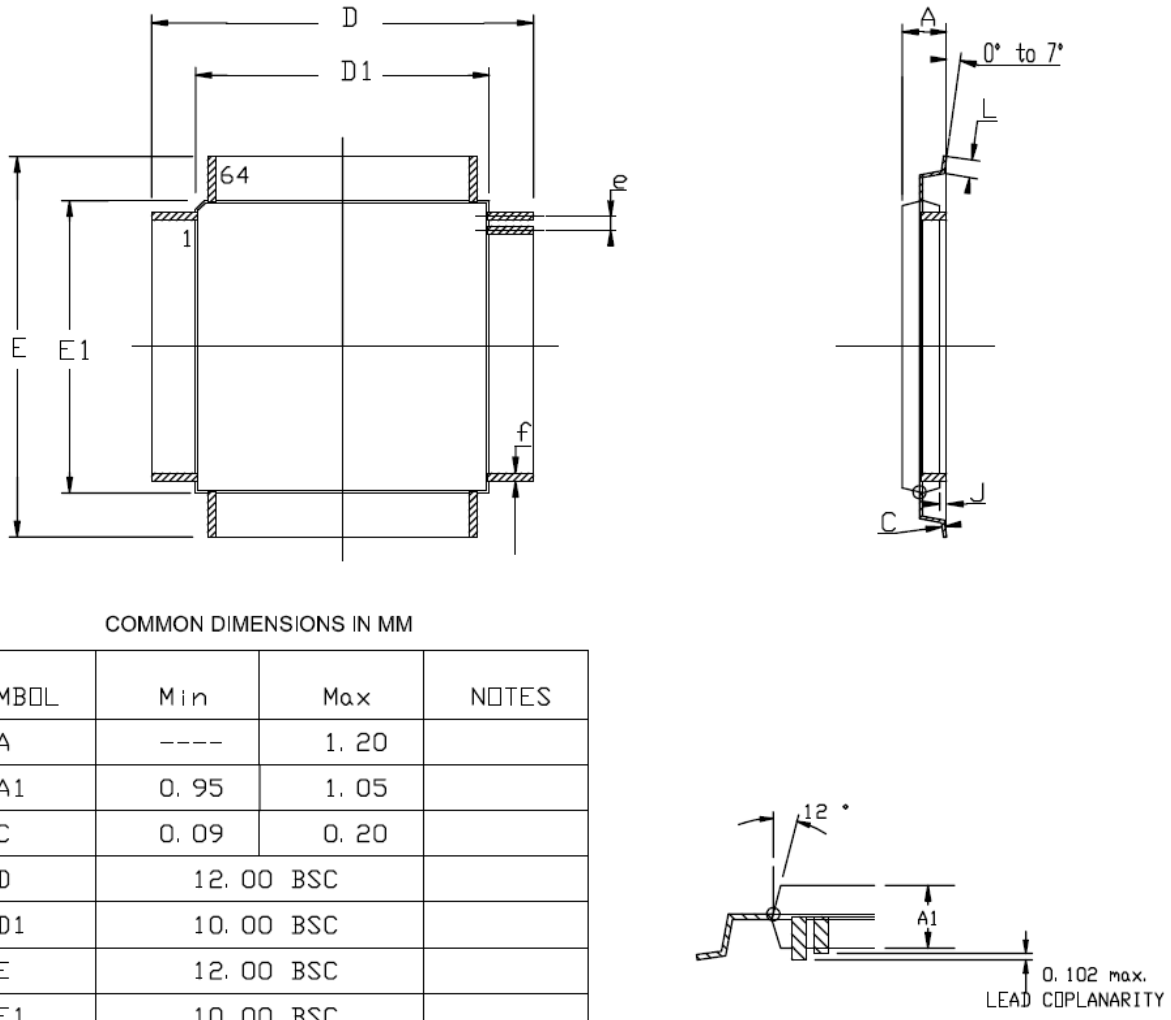
Table 10-12. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-13. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E1

Figure 10-7. TQFP-64 Package Drawing



COMMON DIMENSIONS IN MM

SYMBOL	Min	Max	NOTES
A	----	1.20	
A1	0.95	1.05	
C	0.09	0.20	
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
J	0.05	0.15	
L	0.45	0.75	
e	0.50 BSC		
f	0.17	0.27	

Table 10-20. Device and Package Maximum Weight

300	mg

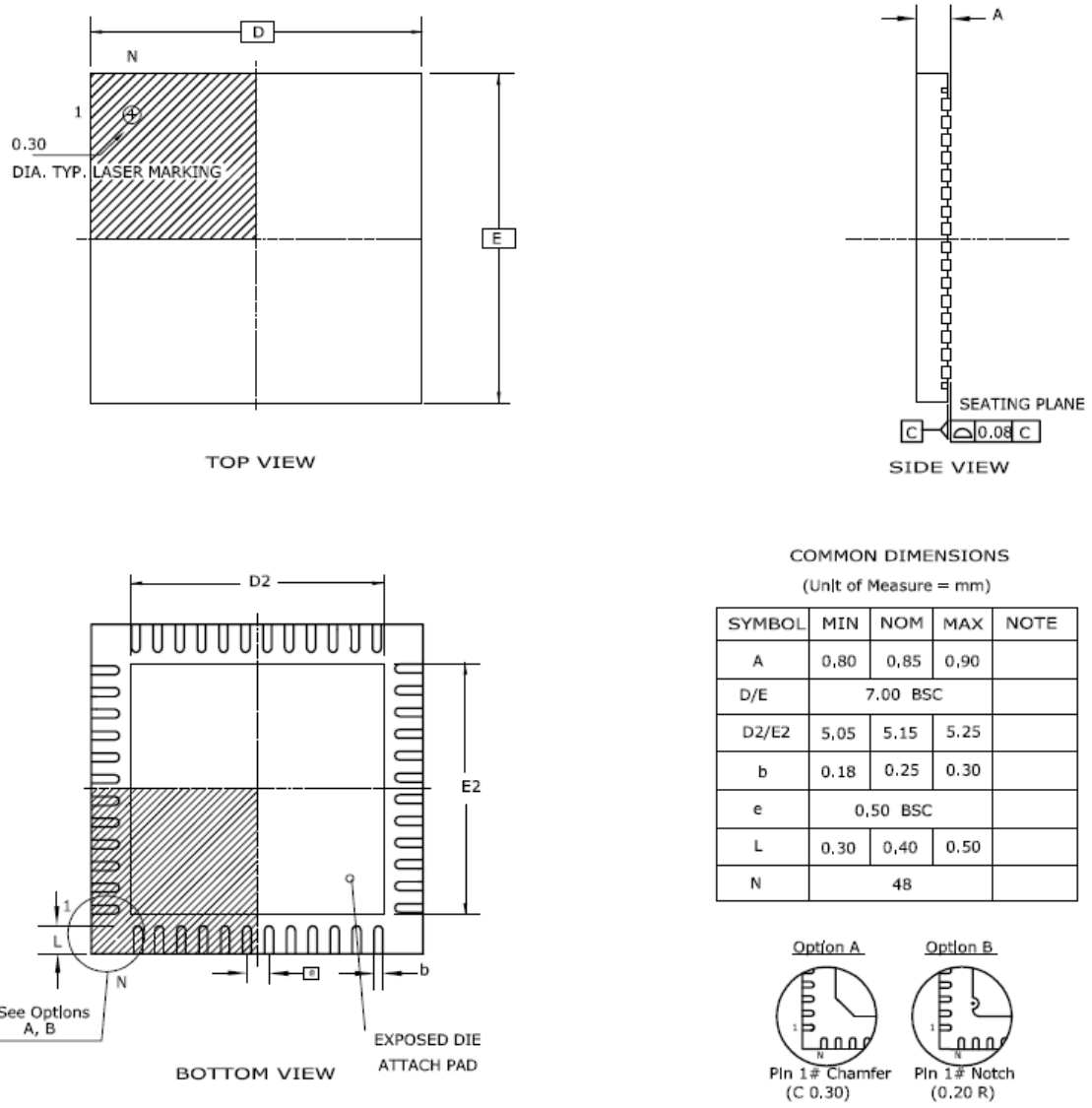
Table 10-21. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-22. Package Reference

JEDEC Drawing Reference	MS-026
JESD97 Classification	E3

Figure 10-10. QFN-48 Package Drawing for ATSAM4LC4/2 and ATSAM4LS4/2



SYMBOL	MIN	NOM	MAX	NOTE
A	0,80	0,85	0,90	
D/E		7.00 BSC		
D2/E2	5,05	5.15	5.25	
b	0.18	0.25	0.30	
e		0,50 BSC		
L	0.30	0,40	0.50	
N		48		

Note: The exposed pad is not connected to anything internally, but should be soldered to ground to increase board level reliability.

Table 10-29. Device and Package Maximum Weight

140	mg

Table 10-30. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 10-31. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3