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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	87
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TA)
Package / Case	132-WFQFN
Supplier Device Package	132-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microsemi/a3p250-qng132t

Table 2-15 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Advanced I/O Banks for A3P250 and A3P1000 Only

	VMV (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.22
3.3 V LVCMOS – Wide Range	3.3	–	16.22
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.65
1.5 V LVCMOS (JESD8-11)	1.5	–	0.98
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64
Differential			
LVDS	2.5	2.26	0.83
LVPECL	3.3	5.72	1.81

Notes:

1. *PDC6 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VMV.*

Table 2-16 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks for A3P250 and A3P1000 Only

	VMV (V)	Static Power PDC6 (mW) [1]	Dynamic Power PAC9 (µW/MHz) [2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.23
3.3 V LVCMOS – Wide Range	3.3	–	16.23
2.5 V LVCMOS	2.5	–	4.66
1.8 V LVCMOS	1.8	–	1.64
1.5 V LVCMOS (JESD8-11)	1.5	–	0.99
3.3 V PCI	3.3	–	17.64
3.3 V PCI-X	3.3	–	17.64

Notes:

1. *PDC6 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VMV.*

Table 2-56 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	5.64	0.05	1.10	0.45	5.74	4.78	2.50	2.43	8.20	7.24	ns
	–1	0.54	4.79	0.04	0.94	0.39	4.88	4.06	2.13	2.07	6.98	6.16	ns
6 mA	Std.	0.63	4.64	0.05	1.10	0.45	4.73	4.16	2.84	3.01	7.19	6.62	ns
	–1	0.54	3.95	0.04	0.94	0.39	4.02	3.54	2.42	2.56	6.11	5.63	ns
8 mA	Std.	0.63	4.64	0.05	1.10	0.45	4.73	4.16	2.84	3.01	7.19	6.62	ns
	–1	0.54	3.95	0.04	0.94	0.39	4.02	3.54	2.42	2.56	6.11	5.63	ns
12 mA	Std.	0.63	3.94	0.05	1.10	0.45	4.01	3.67	3.07	3.39	6.47	6.13	ns
	–1	0.54	3.35	0.04	0.94	0.39	3.41	3.12	2.61	2.88	5.51	5.21	ns
16 mA	Std.	0.63	3.94	0.05	1.10	0.45	4.01	3.67	3.07	3.39	6.47	6.13	ns
	–1	0.54	3.35	0.04	0.94	0.39	3.41	3.12	2.61	2.88	5.51	5.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-57 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.63	3.07	0.05	1.10	0.45	3.13	2.46	2.50	2.57	5.59	4.91	ns
	–1	0.54	2.61	0.04	0.94	0.39	2.66	2.09	2.13	2.19	4.75	4.18	ns
6 mA	Std.	0.63	2.51	0.05	1.10	0.45	2.55	1.97	2.84	3.16	5.01	4.43	ns
	–1	0.54	2.13	0.04	0.94	0.39	2.17	1.67	2.41	2.69	4.26	3.76	ns
8 mA	Std.	0.63	2.51	0.05	1.10	0.45	2.55	1.97	2.84	3.16	5.01	4.43	ns
	–1	0.54	2.13	0.04	0.94	0.39	2.17	1.67	2.41	2.69	4.26	3.76	ns
12 mA	Std.	0.63	2.24	0.05	1.10	0.45	2.28	1.72	3.07	3.54	4.74	4.18	ns
	–1	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56	ns
16 mA	Std.	0.63	2.24	0.05	1.10	0.45	2.28	1.72	3.07	3.54	4.74	4.18	ns
	–1	0.54	1.90	0.04	0.94	0.39	1.94	1.47	2.61	3.01	4.03	3.56	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-74 • 2.5 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	6.87	0.05	2.04	2.56	0.52	6.99	5.83	2.70	2.19	9.20	8.03	ns
	–1	0.68	5.84	0.05	1.73	2.17	0.44	5.95	4.96	2.29	1.86	7.82	6.83	ns
8 mA	Std.	0.80	5.62	0.05	2.04	2.56	0.52	5.72	4.94	3.08	2.90	7.92	7.14	ns
	–1	0.68	4.78	0.05	1.73	2.17	044	4.86	4.20	2.62	2.47	6.74	6.08	ns
12 mA	Std.	0.80	4.73	0.05	2.04	2.56	0.52	4.81	4.30	3.34	3.38	7.01	6.50	ns
	–1	0.68	4.02	0.05	1.73	2.17	0.44	4.09	3.65	2.84	2.87	5.97	5.53	ns
16 mA	Std.	0.80	4.46	0.05	2.04	2.56	0.52	4.53	4.16	3.39	3.50	6.74	6.36	ns
	–1	0.68	3.79	0.05	1.73	2.17	0.44	3.86	3.54	2.89	2.98	5.73	5.41	ns
24 mA	Std.	0.80	4.34	0.05	2.04	2.56	0.52	4.41	4.17	3.47	3.96	6.62	6.38	ns
	–1	0.68	3.69	0.05	1.73	2.17	0.44	3.75	3.55	2.95	3.96	5.63	5.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-75 • 2.5 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Pro I/Os for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.80	3.51	0.05	2.04	2.56	0.52	3.56	3.13	2.70	2.27	5.77	5.33	ns
	–1	0.68	2.98	0.05	1.73	2.17	0.44	3.03	2.66	2.29	1.93	4.91	4.53	ns
8 mA	Std.	0.80	2.87	0.05	2.04	2.56	0.52	2.92	2.40	3.08	3.01	5.12	4.61	ns
	–1	0.68	2.44	0.05	1.73	2.17	0.44	2.48	2.05	2.62	2.56	4.36	3.92	ns
12 mA	Std.	0.80	2.50	0.05	2.04	2.56	0.52	2.53	2.05	3.34	3.47	4.74	4.25	ns
	–1	0.68	2.12	0.05	1.73	2.17	0.44	2.15	1.74	2.84	2.95	4.03	3.62	ns
16 mA	Std.	0.80	2.43	0.05	2.04	2.56	0.52	2.47	1.98	3.39	3.59	4.67	4.19	ns
	–1	0.68	2.07	0.05	1.73	2.17	0.44	2.10	1.69	2.89	3.06	3.97	3.56	ns
24 mA	Std.	0.80	2.44	0.05	2.04	2.56	0.52	2.48	1.90	3.47	4.08	4.68	4.10	ns
	–1	0.68	2.08	0.05	1.73	2.17	0.44	2.11	1.61	2.95	3.47	3.98	3.49	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-92 • 1.8 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	8.81	0.05	1.43	0.45	8.98	7.51	2.48	1.61	11.44	9.97	ns
	–1	0.54	7.50	0.04	1.21	0.39	7.64	6.39	2.11	1.37	9.73	8.48	ns
4 mA	Std.	0.63	7.10	0.05	1.43	0.45	7.23	6.43	2.92	2.75	9.69	8.89	ns
	–1	0.54	6.04	0.04	1.21	0.39	6.15	5.47	2.48	2.34	8.24	7.56	ns
6 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns
8 mA	Std.	0.63	6.06	0.05	1.43	0.45	6.17	5.68	3.23	3.29	8.63	8.14	ns
	–1	0.54	5.16	0.04	1.21	0.39	5.25	4.84	2.75	2.80	7.34	6.93	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-93 • 1.8 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.63	3.94	0.05	1.32	0.45	4.01	3.72	2.47	1.67	6.47	6.18	ns
	–1	0.54	3.35	0.04	1.12	0.39	3.41	3.16	2.10	1.42	5.51	5.26	ns
4 mA	Std.	0.63	3.03	0.05	1.32	0.45	3.09	2.75	2.91	2.86	5.55	5.21	ns
	–1	0.54	2.58	0.04	1.12	0.39	2.63	2.34	2.48	2.44	4.72	4.43	ns
6 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns
8 mA	Std.	0.63	2.65	0.05	1.32	0.45	2.70	2.27	3.22	3.41	5.16	4.73	ns
	–1	0.54	2.26	0.04	1.12	0.39	2.30	1.93	2.74	2.90	4.39	4.02	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.*

Timing Characteristics

1.2 V DC Core Voltage

Table 2-108 • 1.2 V LVCMOS Low Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	12.61	0.05	2.65	3.75	0.52	12.10	9.50	5.11	4.66	14.31	11.71	ns
	–1	0.68	10.72	0.05	2.25	3.19	0.44	10.30	8.08	4.35	3.97	12.17	9.96	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-109 • 1.2 V LVCMOS High Slew
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V
Applicable to Pro I/O Banks for A3PE600L and A3PE3000L Only

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.80	5.16	0.05	2.65	3.75	0.52	4.98	4.39	5.10	4.81	7.19	6.60	ns
	–1	0.68	4.39	0.05	2.25	3.19	0.44	4.24	3.74	4.34	4.09	6.11	5.61	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-170 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-28 on page 2-91 for more information.*

Table 2-171 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* *See Figure 2-29 on page 2-93 for more information.*

Table 2-180 • Output Enable Register Propagation Delays
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.54	0.63	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.38	0.44	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.52	0.62	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.80	0.94	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.80	0.94	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.31	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.31	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Table 2-187 • Output DDR Propagation Delays
Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.74	0.87	ns
$t_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.40	0.47	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.40	0.47	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.85	1.00	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	0.28	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	0.22	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	0.36	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	0.32	ns
$F_{DDROMAX}$	Maximum Frequency for the Output DDR	250	250	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-188 • Output DDR Propagation Delays
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V for A3P250 and A3P1000

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.84	0.99	ns
$t_{DDRISUD1}$	Data_F Data Setup for Output DDR	0.46	0.54	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.46	0.54	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.96	1.13	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.31	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.37	0.43	ns
$F_{DDROMAX}$	Maximum Frequency for the Output DDR	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

Timing Characteristics

Table 2-192 • Register Delays
Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.14 V for A3PE600L and A3PE3000L

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.76	0.90	ns
t_{SUD}	Data Setup Time for the Core Register	0.59	0.70	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.63	0.74	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.55	0.65	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.55	0.65	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.31	0.36	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.31	0.36	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	0.34	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	0.64	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	0.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

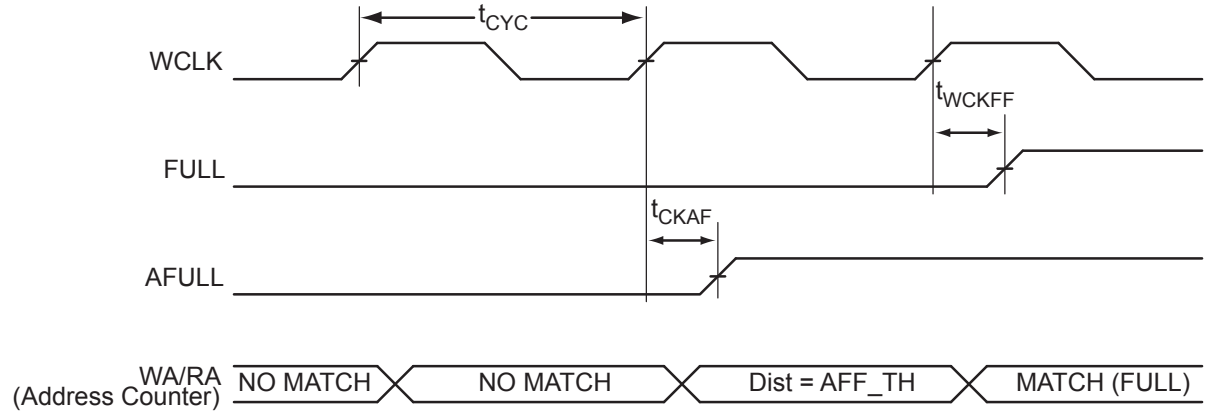

Figure 2-52 • **FIFO FULL Flag and AFULL Flag Assertion**

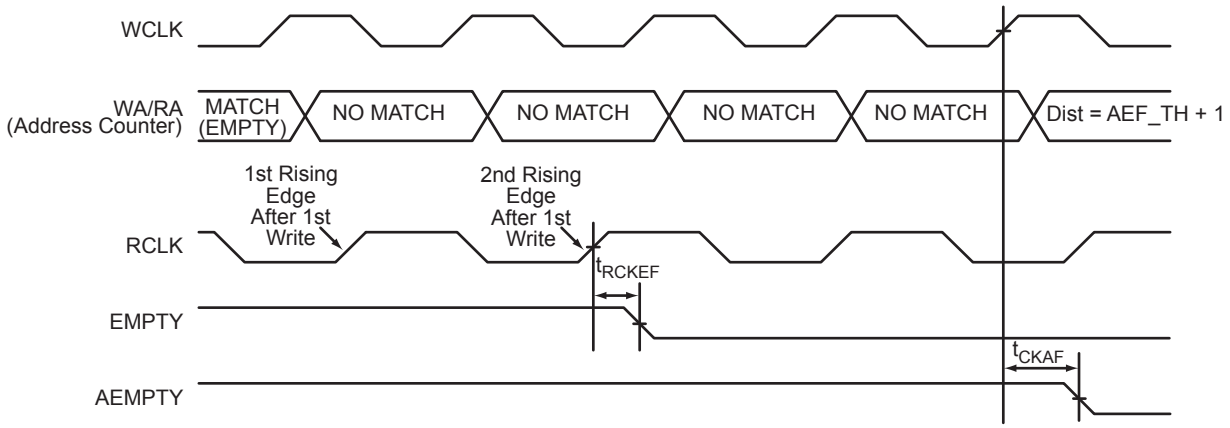

Figure 2-53 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

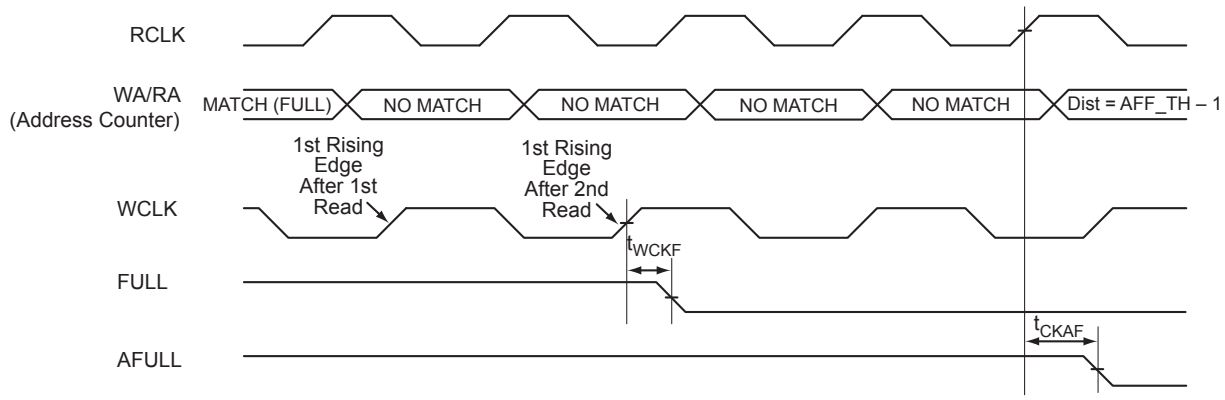

Figure 2-54 • **FIFO FULL Flag and AFULL Flag Deassertion**

Table 2-211 • FIFO Worst Military-Case Conditions: T_J = 125°C, VCC = 1.425 V for A3P1000

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.66	1.95	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	ns
t_{BKS}	BLK Setup Time	1.66	1.95	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on RD (flow-through)	2.84	3.33	ns
t_{CKQ2}	Clock HIGH to New Data Valid on RD (pipelined)	1.08	1.27	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.07	2.43	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	1.96	2.31	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	7.45	8.76	ns
t_{RSTFG}	RESET LOW to Empty/Full Flag Valid	2.04	2.40	ns
t_{RSTAF}	RESET LOW to Almost Empty/Full Flag Valid	7.38	8.67	ns
t_{RSTBQ}	RESET LOW to Data Out LOW on RD (flow-through)	1.11	1.31	ns
	RESET LOW to Data Out LOW on RD (pipelined)	1.11	1.31	ns
$t_{REMRSTB}$	RESET Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET Recovery	1.81	2.12	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.89	4.57	ns
F_{MAX}	Maximum Frequency for FIFO	257	219	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-6 for derating values.

VQ100	
Pin Number	**A3P250 Function**
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

VQ100	
Pin Number	**A3P250 Function**
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

VQ100	
Pin Number	**A3P250 Function**
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

PQ208	
Pin Number	A3P1000 Function
1	GND
2	GAA2/IO225PDB3
3	IO225NDB3
4	GAB2/IO224PDB3
5	IO224NDB3
6	GAC2/IO223PDB3
7	IO223NDB3
8	IO222PDB3
9	IO222NDB3
10	IO220PDB3
11	IO220NDB3
12	IO218PDB3
13	IO218NDB3
14	IO216PDB3
15	IO216NDB3
16	VCC
17	GND
18	VCCIB3
19	IO212PDB3
20	IO212NDB3
21	GFC1/IO209PDB3
22	GFC0/IO209NDB3
23	GFB1/IO208PDB3
24	GFB0/IO208NDB3
25	VCOMPLF
26	GFA0/IO207NPB3
27	VCCPLF
28	GFA1/IO207PPB3
29	GND
30	GFA2/IO206PDB3
31	IO206NDB3
32	GFB2/IO205PDB3
33	IO205NDB3
34	GFC2/IO204PDB3
35	IO204NDB3
36	VCC

PQ208	
Pin Number	A3P1000 Function
37	IO199PDB3
38	IO199NDB3
39	IO197PSB3
40	VCCIB3
41	GND
42	IO191PDB3
43	IO191NDB3
44	GEC1/IO190PDB3
45	GEC0/IO190NDB3
46	GEB1/IO189PDB3
47	GEB0/IO189NDB3
48	GEA1/IO188PDB3
49	GEA0/IO188NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO187RSB2
55	GEB2/IO186RSB2
56	GEC2/IO185RSB2
57	IO184RSB2
58	IO183RSB2
59	IO182RSB2
60	IO181RSB2
61	IO180RSB2
62	VCCIB2
63	IO178RSB2
64	IO176RSB2
65	GND
66	IO174RSB2
67	IO172RSB2
68	IO170RSB2
69	IO168RSB2
70	IO166RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P1000 Function
73	IO162RSB2
74	IO160RSB2
75	IO158RSB2
76	IO156RSB2
77	IO154RSB2
78	IO152RSB2
79	IO150RSB2
80	IO148RSB2
81	GND
82	IO143RSB2
83	IO141RSB2
84	IO139RSB2
85	IO137RSB2
86	IO135RSB2
87	IO133RSB2
88	VCC
89	VCCIB2
90	IO128RSB2
91	IO126RSB2
92	IO124RSB2
93	IO122RSB2
94	IO120RSB2
95	IO118RSB2
96	GDC2/IO116RSB2
97	GND
98	GDB2/IO115RSB2
99	GDA2/IO114RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO

FG484	
Pin Number	A3PE3000L Function
C18	GND
C19	IO76PPB1V4
C20	IO88NDB2V0
C21	IO94PPB2V1
C22	VCCIB2
D1	IO293PDB7V2
D2	IO303NDB7V3
D3	IO305NDB7V3
D4	GND
D5	GAA0/IO00NDB0V0
D6	GAA1/IO00PDB0V0
D7	GAB0/IO01NDB0V0
D8	IO20PDB0V2
D9	IO22PDB0V2
D10	IO30PDB0V3
D11	IO38NDB0V4
D12	IO52NDB1V1
D13	IO52PDB1V1
D14	IO66NDB1V3
D15	IO66PDB1V3
D16	GBB1/IO80PDB1V4
D17	GBA0/IO81NDB1V4
D18	GBA1/IO81PDB1V4
D19	GND
D20	IO88PDB2V0
D21	IO90PDB2V1
D22	IO94NPB2V1
E1	IO293NDB7V2
E2	IO299PPB7V3
E3	GND
E4	GAB2/IO308PDB7V4
E5	GAA2/IO309PDB7V4
E6	GNDQ
E7	GAB1/IO01PDB0V0
E8	IO20NDB0V2

FG484	
Pin Number	A3PE3000L Function
E9	IO22NDB0V2
E10	IO30NDB0V3
E11	IO38PDB0V4
E12	IO44NDB1V0
E13	IO58NDB1V2
E14	IO58PDB1V2
E15	GBC1/IO79PDB1V4
E16	GBB0/IO80NDB1V4
E17	GNDQ
E18	GBA2/IO82PDB2V0
E19	IO86NDB2V0
E20	GND
E21	IO90NDB2V1
E22	IO98PDB2V2
F1	IO299NPB7V3
F2	IO301NDB7V3
F3	IO301PDB7V3
F4	IO308NDB7V4
F5	IO309NDB7V4
F6	VMV7
F7	VCCPLA
F8	GAC0/IO02NDB0V0
F9	GAC1/IO02PDB0V0
F10	IO32NDB0V3
F11	IO32PDB0V3
F12	IO44PDB1V0
F13	IO50NDB1V1
F14	IO60PDB1V2
F15	GBC0/IO79NDB1V4
F16	VCCPLB
F17	VMV2
F18	IO82NDB2V0
F19	IO86PDB2V0
F20	IO96PDB2V1
F21	IO96NDB2V1

FG484	
Pin Number	A3PE3000L Function
F22	IO98NDB2V2
G1	IO289NDB7V1
G2	IO289PDB7V1
G3	IO291PPB7V2
G4	IO295PDB7V2
G5	IO297PDB7V2
G6	GAC2/IO307PDB7V4
G7	VCOMPLA
G8	GNDQ
G9	IO26NDB0V3
G10	IO26PDB0V3
G11	IO36PDB0V4
G12	IO42PDB1V0
G13	IO50PDB1V1
G14	IO60NDB1V2
G15	GNDQ
G16	VCOMPLB
G17	GBB2/IO83PDB2V0
G18	IO92PDB2V1
G19	IO92NDB2V1
G20	IO102PDB2V2
G21	IO102NDB2V2
G22	IO105NDB2V2
H1	IO286PSB7V1
H2	IO291NPB7V2
H3	VCC
H4	IO295NDB7V2
H5	IO297NDB7V2
H6	IO307NDB7V4
H7	IO287PDB7V1
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO36NDB0V4
H12	IO42NDB1V0

FG896	
Pin Number	A3PE3000L Function
A2	GND
A3	GND
A4	IO14NPB0V1
A5	GND
A6	IO07NPB0V0
A7	GND
A8	IO09NDB0V1
A9	IO17NDB0V2
A10	IO17PDB0V2
A11	IO21NDB0V2
A12	IO21PDB0V2
A13	IO33NDB0V4
A14	IO33PDB0V4
A15	IO35NDB0V4
A16	IO35PDB0V4
A17	IO41NDB1V0
A18	IO43NDB1V0
A19	IO43PDB1V0
A20	IO45NDB1V0
A21	IO45PDB1V0
A22	IO57NDB1V2
A23	IO57PDB1V2
A24	GND
A25	IO69PPB1V3
A26	GND
A27	GBC1/IO79PPB1V4
A28	GND
A29	GND
AA1	IO256PDB6V2
AA2	IO248PDB6V1
AA3	IO248NDB6V1
AA4	IO246NDB6V1
AA5	GEA1/IO234PDB6V0
AA6	GEA0/IO234NDB6V0
AA7	IO243PPB6V1
AA8	IO245NDB6V1

FG896	
Pin Number	A3PE3000L Function
AA9	GEB1/IO235PPB6V0
AA10	VCC
AA11	IO226PPB5V4
AA12	VCCIB5
AA13	VCCIB5
AA14	VCCIB5
AA15	VCCIB5
AA16	VCCIB4
AA17	VCCIB4
AA18	VCCIB4
AA19	VCCIB4
AA20	IO174PDB4V2
AA21	VCC
AA22	IO142NPB3V3
AA23	IO144NDB3V3
AA24	IO144PDB3V3
AA25	IO146NDB3V4
AA26	IO146PDB3V4
AA27	IO147PDB3V4
AA28	IO139NDB3V3
AA29	IO139PDB3V3
AA30	IO133NDB3V2
AB1	IO256NDB6V2
AB2	IO244PDB6V1
AB3	IO244NDB6V1
AB4	IO241PDB6V0
AB5	IO241NDB6V0
AB6	IO243NPB6V1
AB7	VCCIB6
AB8	VCCPLE
AB9	VCC
AB10	IO222PDB5V3
AB11	IO218PPB5V3
AB12	IO206NDB5V1
AB13	IO206PDB5V1
AB14	IO198NDB5V0

FG896	
Pin Number	A3PE3000L Function
AB15	IO198PDB5V0
AB16	IO192NDB4V4
AB17	IO192PDB4V4
AB18	IO178NDB4V3
AB19	IO178PDB4V3
AB20	IO174NDB4V2
AB21	IO162NPB4V1
AB22	VCC
AB23	VCCPLD
AB24	VCCIB3
AB25	IO150PDB3V4
AB26	IO148PDB3V4
AB27	IO147NDB3V4
AB28	IO145PDB3V3
AB29	IO143PDB3V3
AB30	IO137PDB3V2
AC1	IO254PDB6V2
AC2	IO254NDB6V2
AC3	IO240PDB6V0
AC4	GEC1/IO236PDB6V0
AC5	IO237PDB6V0
AC6	IO237NDB6V0
AC7	VCOMPLE
AC8	GND
AC9	IO226NPB5V4
AC10	IO222NDB5V3
AC11	IO216NPB5V2
AC12	IO210NPB5V2
AC13	IO204NDB5V1
AC14	IO204PDB5V1
AC15	IO194NDB5V0
AC16	IO188NDB4V4
AC17	IO188PDB4V4
AC18	IO182PPB4V3
AC19	IO170NPB4V2
AC20	IO164NDB4V1

FG896	
Pin Number	A3PE3000L Function
AC21	IO164PDB4V1
AC22	IO162PPB4V1
AC23	GND
AC24	VCOMPLD
AC25	IO150NDB3V4
AC26	IO148NDB3V4
AC27	GDA1/IO153PDB3V4
AC28	IO145NDB3V3
AC29	IO143NDB3V3
AC30	IO137NDB3V2
AD1	GND
AD2	IO242NPB6V1
AD3	IO240NDB6V0
AD4	GEC0/IO236NDB6V0
AD5	VCCIB6
AD6	GNDQ
AD6	GNDQ
AD7	VCC
AD8	VMV5
AD9	VCCIB5
AD10	IO224PPB5V3
AD11	IO218NPB5V3
AD12	IO216PPB5V2
AD13	IO210PPB5V2
AD14	IO202PPB5V1
AD15	IO194PDB5V0
AD16	IO190PDB4V4
AD17	IO182NPB4V3
AD18	IO176NDB4V2
AD19	IO176PDB4V2
AD20	IO170PPB4V2
AD21	IO166PDB4V1
AD22	VCCIB4
AD23	TCK
AD24	VCC
AD25	TRST

FG896	
Pin Number	A3PE3000L Function
AD26	VCCIB3
AD27	GDA0/IO153NDB3V4
AD28	GDC0/IO151NDB3V4
AD29	GDC1/IO151PDB3V4
AD30	GND
AE1	IO242PPB6V1
AE2	VCC
AE3	IO239PDB6V0
AE4	IO239NDB6V0
AE5	VMV6
AE5	VMV6
AE6	GND
AE7	GNDQ
AE8	IO230NDB5V4
AE9	IO224NPB5V3
AE10	IO214NPB5V2
AE11	IO212NDB5V2
AE12	IO212PDB5V2
AE13	IO202NPB5V1
AE14	IO200NDB5V0
AE15	IO196PDB5V0
AE16	IO190NDB4V4
AE17	IO184PDB4V3
AE18	IO184NDB4V3
AE19	IO172PDB4V2
AE20	IO172NDB4V2
AE21	IO166NDB4V1
AE22	IO160PDB4V0
AE23	GNDQ
AE24	VMV4
AE25	GND
AE26	GDB0/IO152NDB3V4
AE27	GDB1/IO152PDB3V4
AE28	VMV3
AE28	VMV3
AE29	VCC

FG896	
Pin Number	A3PE3000L Function
AE30	IO149PDB3V4
AF1	GND
AF2	IO238PPB6V0
AF3	VCCIB6
AF4	IO220NPB5V3
AF5	VCC
AF6	IO228NDB5V4
AF7	VCCIB5
AF8	IO230PDB5V4
AF9	IO229NDB5V4
AF10	IO229PDB5V4
AF11	IO214PPB5V2
AF12	IO208NDB5V1
AF13	IO208PDB5V1
AF14	IO200PDB5V0
AF15	IO196NDB5V0
AF16	IO186NDB4V4
AF17	IO186PDB4V4
AF18	IO180NDB4V3
AF19	IO180PDB4V3
AF20	IO168NDB4V1
AF21	IO168PDB4V1
AF22	IO160NDB4V0
AF23	IO158NPB4V0
AF24	VCCIB4
AF25	IO154NPB4V0
AF26	VCC
AF27	TDO
AF28	VCCIB3
AF29	GNDQ
AF29	GNDQ
AF30	GND
AG1	IO238NPB6V0
AG2	VCC
AG3	IO232NPB5V4
AG4	GND

FG896	
Pin Number	**A3PE3000L Function**
L8	IO293PDB7V2
L9	IO293NDB7V2
L10	IO307NPB7V4
L11	VCC
L12	VCC
L13	VCC
L14	VCC
L15	VCC
L16	VCC
L17	VCC
L18	VCC
L19	VCC
L20	VCC
L21	IO78NPB1V4
L22	IO104NPB2V2
L23	IO98NDB2V2
L24	IO98PDB2V2
L25	IO87PDB2V0
L26	IO87NDB2V0
L27	IO97PDB2V1
L28	IO101PDB2V2
L29	IO103PDB2V2
L30	IO119NDB3V0
M1	IO282NDB7V1
M2	IO282PDB7V1
M3	IO292NDB7V2
M4	IO292PDB7V2
M5	IO283NDB7V1
M6	IO285PDB7V1
M7	IO287PDB7V1
M8	IO289PDB7V1
M9	IO289NDB7V1
M10	VCCIB7
M11	VCC
M12	GND
M13	GND

FG896	
Pin Number	**A3PE3000L Function**
T2	VCCPLF
T3	GFA2/IO272PPB6V4
T4	GFA1/IO273PDB6V4
T5	IO272NPB6V4
T6	IO267NDB6V4
T7	IO267PDB6V4
T8	IO265PDB6V3
T9	IO263PDB6V3
T10	VCCIB6
T11	VCC
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	GND
T18	GND
T19	GND
T20	VCC
T21	VCCIB3
T22	IO109NPB2V3
T23	IO116NDB3V0
T24	IO118NDB3V0
T25	IO122NPB3V1
T26	GCA1/IO114PPB3V0
T27	GCB0/IO113NPB2V3
T28	GCA2/IO115PPB3V0
T29	VCCPLC
T30	IO121PDB3V0
U1	IO268PDB6V4
U2	IO264NDB6V3
U3	IO264PDB6V3
U4	IO258PDB6V3
U5	IO258NDB6V3
U6	IO257PPB6V2
U7	IO261PPB6V3

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "Military ProASIC3/EL Device Status" table on page II, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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