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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	23
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d8608ssc

  - Oscillator Operational Mode: Normal High Frequency Operation Enabled or 32 KHz Operation Enabled
  - Port 0: 0–3 Pull-Ups
  - Port 0: 4–7 Pull-Ups
  - Port 2: 0–7 Pull-Ups
  - Port 0: 0–3 Mouse Mode: Normal Mode (.5V_{DD} Input Threshold) vs. Mouse Mode (.4V_{DD} Input Threshold)
- Port 3 does not feature the pull-up option.

General Description

The Z86D86 is a 28-pin one-time programmable (OTP) infrared (IR) microcontroller. Based on a single-chip Z8 microcontroller (MCU) design, the Z86D86 features 237 bytes of general-purpose RAM and 32 KB of OTP ROM. ZiLOG's CMOS microcontrollers offer fast executing, efficient use of memory, sophisticated interrupts, input/output bit-manipulation capabilities, automated pulse generation/reception, and internal key-scan pull-up transistors.

The Z86L825 architecture is based on ZiLOG's 8-bit microcontroller core, featuring an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and batter-operated hand-held applications.

There are three basic address spaces available to support a wide range of configurations: program memory, register file, and Expanded Register File. The register file consists of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and 236 general-purpose registers. (Register FEh (SPH) can be used as a general-purpose register.) The Expanded Register File consists of two additional register groups (F and D).

The Z86D86 offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (Figure 9 on page 17).

Table 2. 28-Pin DIP and SOIC Pin Identification (Continued)

28-Pin DIP and SOIC	Standard Mode	Direction	Description
18	Pref1	Input	Analog ref input (must be pulled high externally, if not used)
11	P31	Input	IRQ2/modulator input
12	P32	Input	IRQ0
13	P33	Input	IRQ1
14	P34	Output	T8 output
15	P35	Output	T16 output
17	P36	Output	T8/T16 output
16	P37	Output	
10	XTAL1	Input	Crystal, oscillator clock
9	XTAL2	Output	Crystal, oscillator clock
8	V_{DD}		Power supply
22	V_{SS}		Ground

Absolute Maximum Ratings

Table 3 lists the absolute maximum ratings for the Z86D86 microcontroller.

Table 3. Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
V_{MAX}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temperature	–65°	+150°	C
T_A	Oper. Ambient Temperature	0°	70°	C

Notes:
* Voltage on all pins with respect to GND

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see Figure 4).

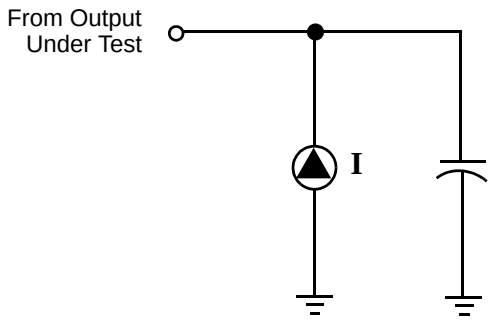

Figure 4. Test Load Diagram

Capacitance

Table 4 lists the capacitance for the Z86D86 microcontroller.

Table 4. Capacitance

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

Note: T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins returned to GND.

DC Characteristics

Table 5 lists the direct current (DC) characteristics.

Table 5. DC Characteristics

			T_A = 0 °C to +70 °C				
Symbol	**Parameter**	**V_{CC}**	**Min**	**Max**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	2.3 V	0.8 V_{CC}	V_{CC} + 0.3	V	Driven by External Clock Generator	
		5.5 V	0.8 V_{CC}	V_{CC} + 0.3	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	2.3 V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
		5.5 V	V_{SS}–0.3	0.2 V_{CC}	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	2.3 V	0.7 V_{CC}	V_{CC} + 0.3	V		
		5.5 V	0.7 V_{CC}	V_{CC} + 0.3	V		
V_{IL}	Input Low Voltage	2.3 V	V_{SS}–0.3	0.2 V_{CC}	V		
		5.5 V	V_{SS}–0.3	0.2 V_{CC}	V		
V_{OH1}	Output High Voltage	2.3 V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
		5.5 V	V_{CC}–0.4		V	I_{OH} = –0.5 mA	
V_{OH2}	Output High Voltage (P36, P37, P00, and P01)	2.3 V	V_{CC}–0.8		V	I_{OH} = –7 mA	
		5.5 V	V_{CC}–0.8		V	I_{OH} = –7 mA	
V_{OL1}	Output Low Voltage	2.3 V		0.4	V	I_{OL} = 1.0 mA	
		5.5 V		0.4	V	I_{OL} = 4.0 mA	
V_{OL2}	Output Low Voltage	2.3 V		0.8	V	I_{OL} = 5.0 mA	1
		5.5 V		0.8	V	I_{OL} = 7.0 mA	1
V_{OL2}	Output Low Voltage (P00, P01, P36, and P37)	2.3 V		0.8	V	I_{OL} = 10 mA	
		5.5 V		0.8	V	I_{OL} = 10 mA	
V_{OFFSET}	Comparator Input Offset Voltage	2.3 V		25	mV		
		5.5 V		25	mV		
V_{REF}	Comparator Reference Voltage	2.3 V	0	V_{CC}– 1.75	V		
		5.5 V	0	V_{CC}– 1.75	V		
I_{IL}	Input Leakage	2.3 V	–1	1	µA	V_{IN} = 0$_V$, V_{CC}	
		5.5 V	–1	1	µA	V_{IN} = 0$_V$, V_{CC}	
I_{OL}	Output Leakage	2.3 V	–1	1	µA	V_{IN} = 0$_V$, V_{CC}	
		5.5 V	–1	1	µA	V_{IN} = 0$_V$, V_{CC}	

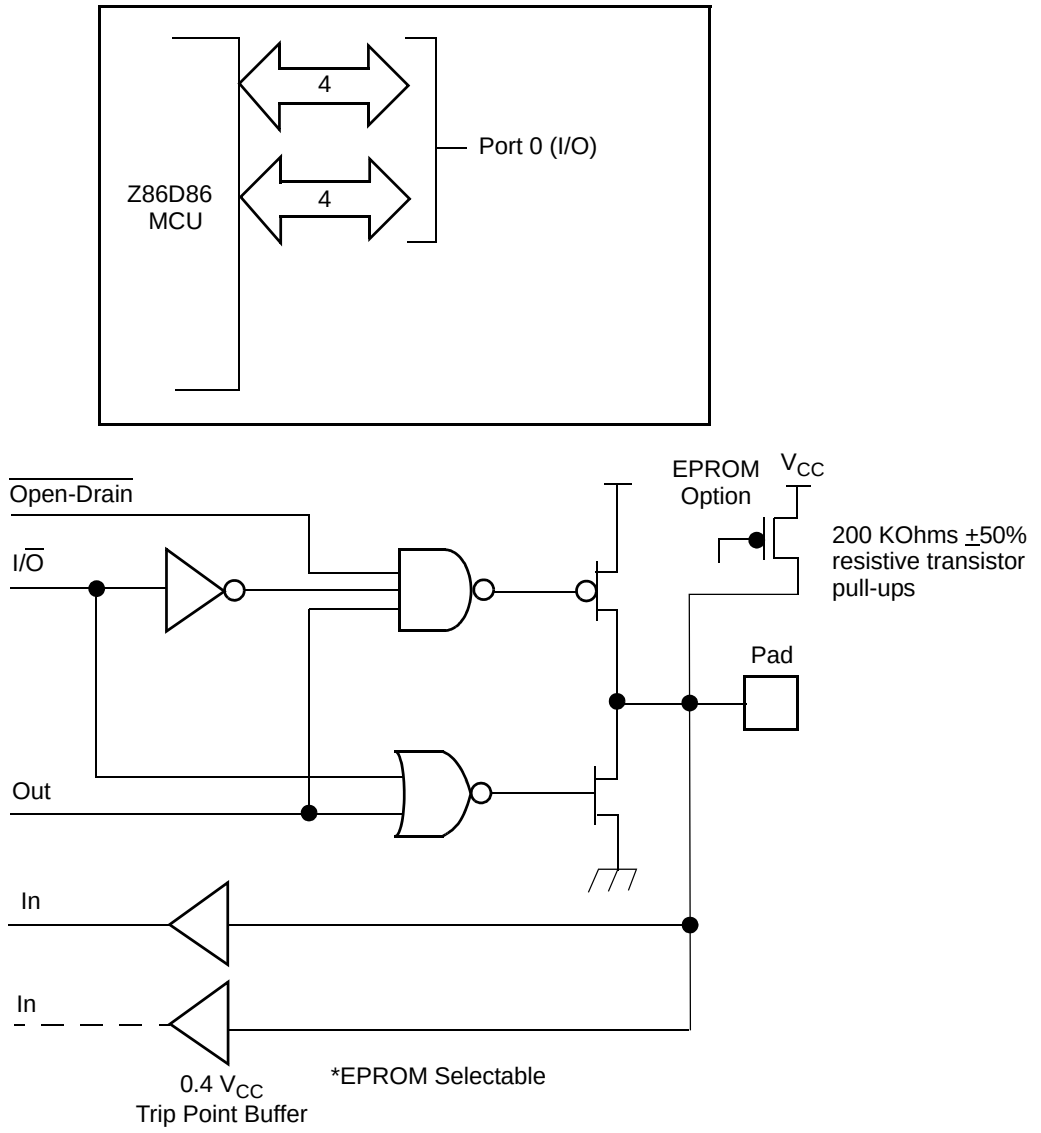

Figure 6. Port 0 Configuration

Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port. These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A mask option is available to connect eight 200 KΩ (±50%) pull-up transistors on this port. Bits programmed as outputs are

T16 Common Control Register" on page 39). Other edge-detect and IRQ modes are described in Table 7.

Table 7. Pin Assignments

Pin	I/O	C/T	Comp.	Int.
Pref1			RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for the counter/timers and the AND/OR logic. Control is performed by programming bits D5–D4 of CTR1 and bit 0 of CTR2.

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 8 on page 15. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

Note: Comparators are powered down by entering STOP Mode. For P31–P33 to be used in a Stop-Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These outputs can be programmed to output on P34 and P37 through the PCON register (Figure 9).

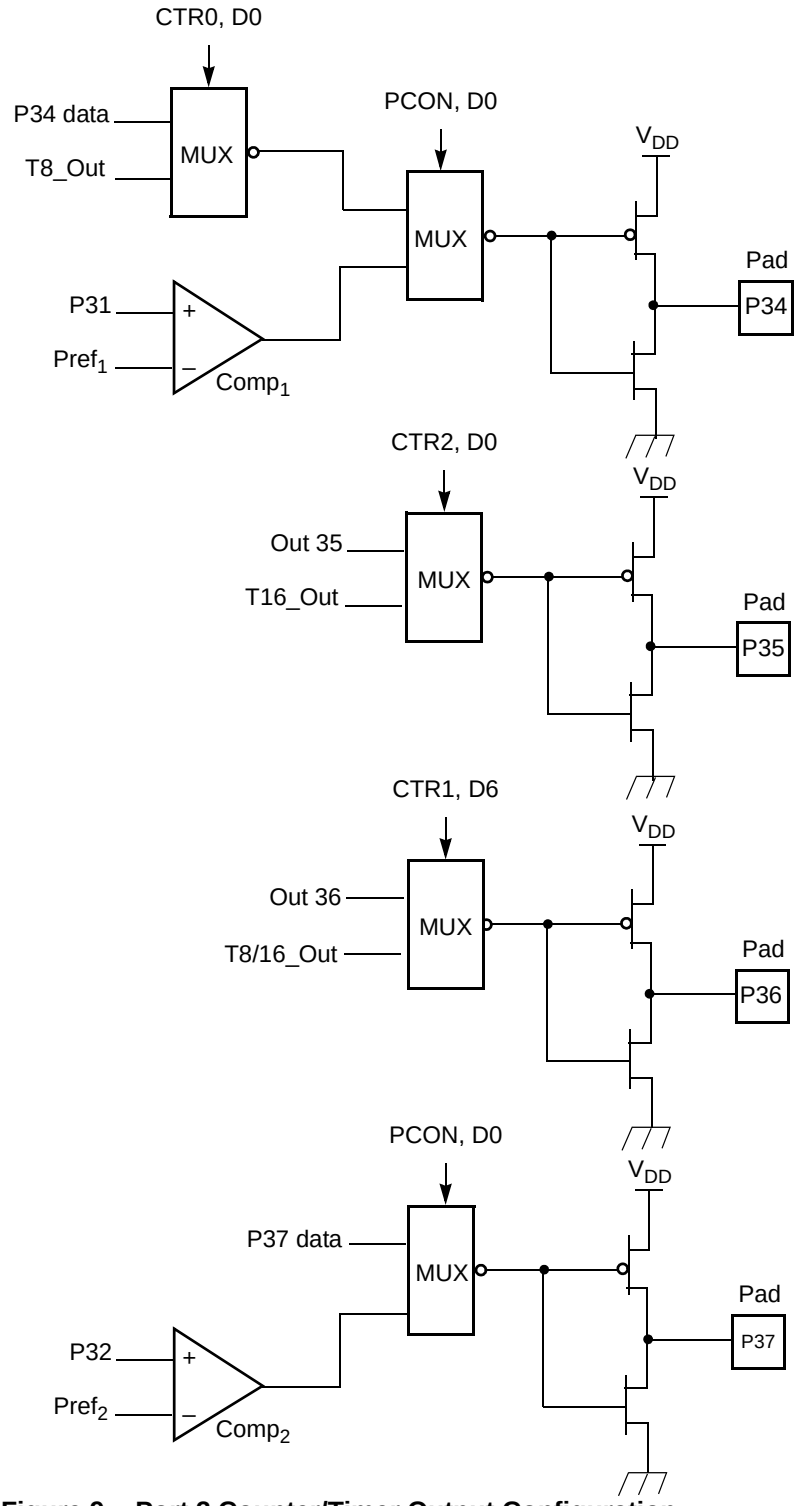

Figure 9. Port 3 Counter/Timer Output Configuration

Functional Description

The Z86D86 incorporates special functions to enhance the Z8's functionality in consumer and battery-operated applications.

Program Memory

The Z86D86 family addresses 32 KB of internal program memory. The first twelve bytes are reserved for interrupt vectors. These locations contain the five 16-bit vectors that correspond to the five available interrupts.

RAM

The Z86D86 device has 237 bytes of RAM that make up the register file.

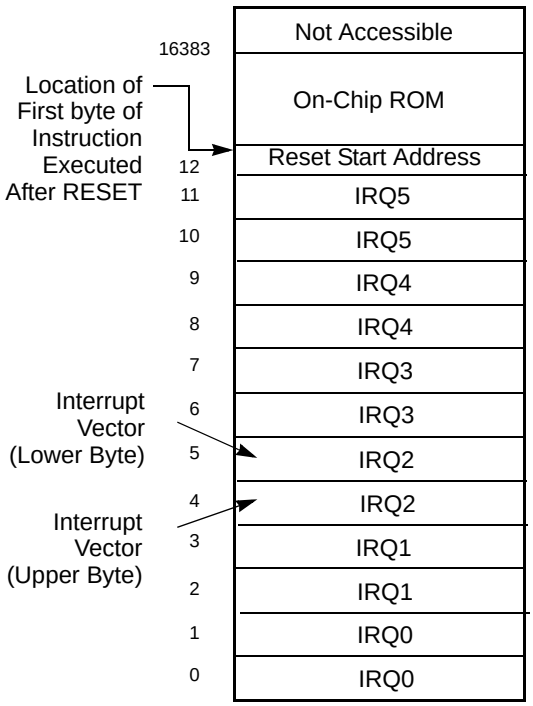

Figure 10. Program Memory Map (32K ROM)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as

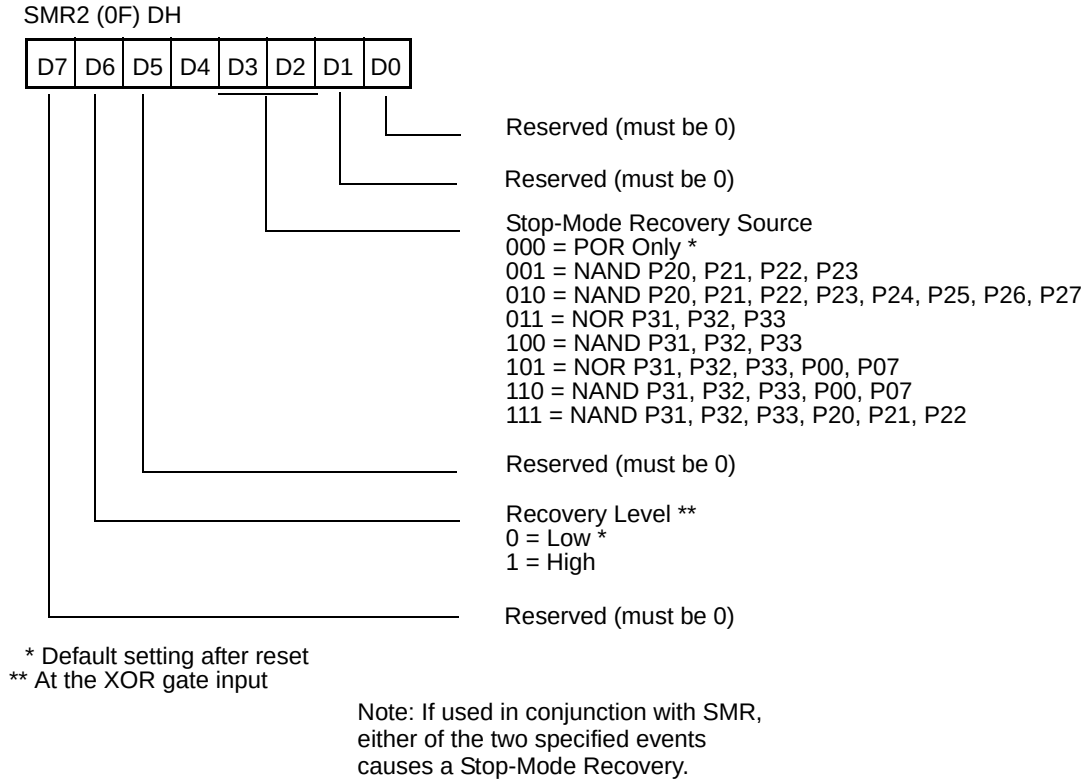

Figure 18. Stop-Mode Recovery Register 2—(0F) 0DH: D2–D4, D6 Write Only

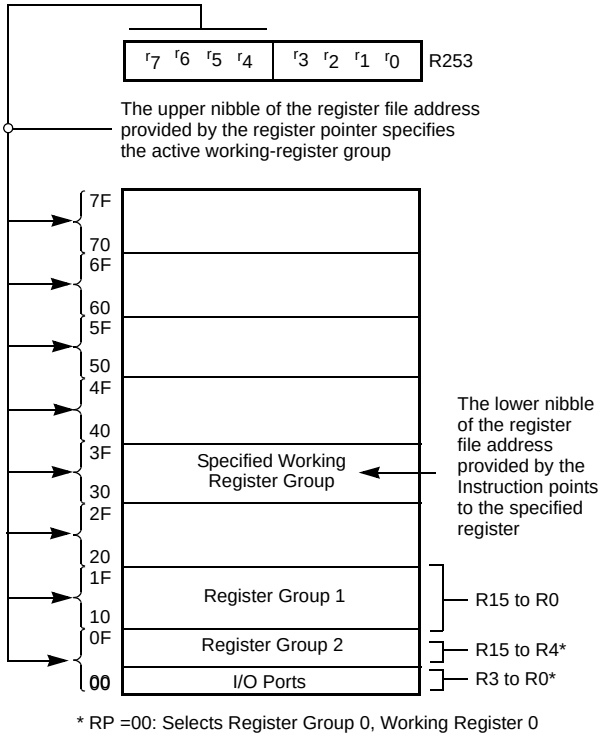

Figure 31. Register Pointer

Stack

The Z86D86 internal register file is used for the stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

Note: When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed.

Counter/Timer Registers

Table 8 describes the expanded register group D.

Table 8. Expanded Register Group D

(D)0Ch	LVD
(D)0Bh	HI8
(D)0Ah	LO8
(D)09h	HI16
(D)08h	LO16
(D)07h	TC16H
(D)06h	TC16L
(D)05h	TC8H
(D)04h	TC8L
(D)03h	Reserved
(D)02h	CTR2
(D)01h	CTR1
(D)00h	CTR0

Register Description

LBD(D)0Ch—Low Battery Detection Register

Bit 0 enables/disables the Low Battery Detection Circuit. Bit 1 flags if low battery is detected. Interrupt 5 is triggered when the flag bit is set, given that IRQ5 is not masked. See Table 9.

Note: The LVD flag will be valid after enabling the detection for 20 μS (design estimation, not tested in production). LVD does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

Table 12. HI16(D)09h

Field	Bit Position		Description
T16_Capture_HI	76543210	R W	Captured Data No Effect

L016(D)08h

This register (Table 13) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

Table 13. L016(D)08h

Field	Bit Position		Description
T16_Capture_LO	76543210	R W	Captured Data No Effect

TC16H(D)07h

Table 14 describes the Counter/Timer2 MS-Byte Hold Register.

Table 14. TC16H(D)07h

Field	Bit Position		Description
T16_Data_HI	76543210	R/W	Data

TC16L(D)06h

Table 15 describes the Counter/Timer2 LS-Byte Hold Register.

Table 15. TC16L(D)06h

Field	Bit Position		Description
T16_Data_LO	76543210	R/W	Data

TC8H(D)05h

Table 16 describes the Counter/Timer8 High Hold Register.

Table 16. TC8H(D)05h

Field	Bit Position		Description
T8_Level_HI	76543210	R/W	Data

TC8L(D)04h

Table 17 describes the Counter/Timer8 Low Hold Register.

Table 17. TC8L(D)04h

Field	Bit Position		Description
T8_Level_LO	76543210	R/W	Data

CTR0 Counter/Timer8 Control Register

Table 18 describes the CTR0 (D)00 Counter/Timer8 Control Register.

Table 18. CTR0 (D)00 Counter/Timer8 Control Register

Field	Bit Position		Value	Description
T8_Enable	7-------	R	0*	Counter Disabled
			1	Counter Enabled
		W	0	Stop Counter
			1	Enable Counter
Single/Modulo-N	-6-------	R/W	0	Modulo-N
			1	Single Pass
Time_Out	--5------	R	0	No Counter Time-Out
			1	Counter Time-Out Occurred
		W	0	No Effect
			1	Reset Flag to 0
T8 _Clock	---43---	R/W	0 0	SCLK
			0 1	SCLK/2
			1 0	SCLK/4
			1 1	SCLK/8
Capture_INT_MASK	-----2--	R/W	0	Disable Data Capture Int.
			1	Enable Data Capture Int.

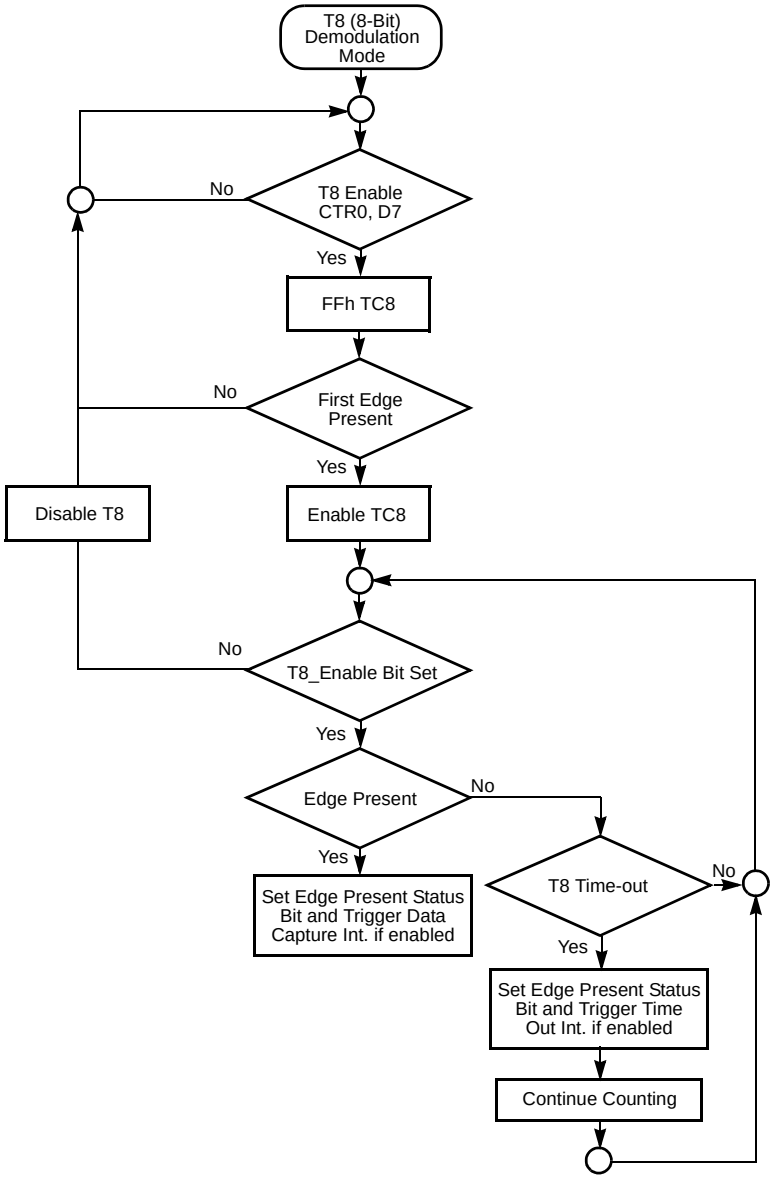

Figure 38. Demodulation Mode Flowchart

Output Circuit

Figure 43 shows the output circuit.

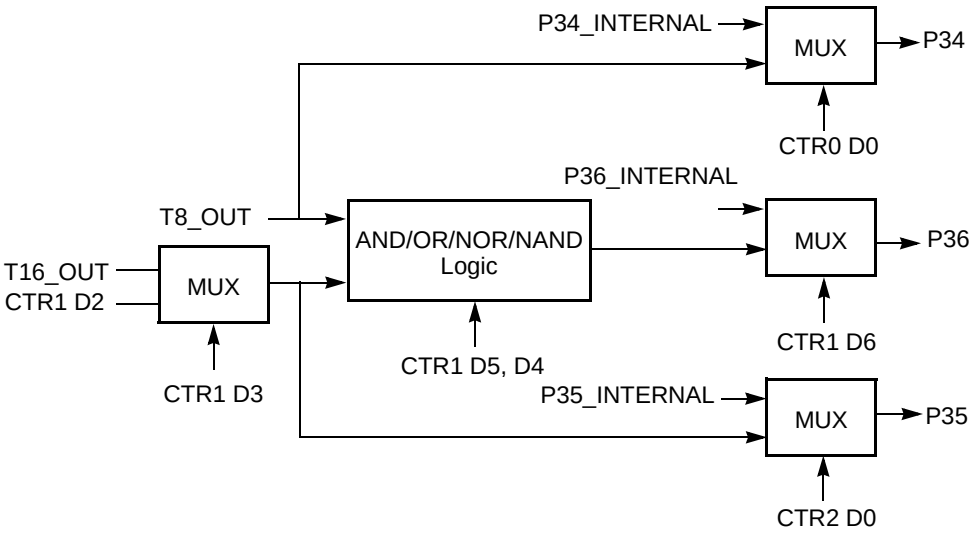

Figure 43. Output Circuit

Interrupts

The Z86D86 features six different interrupts. The interrupts are maskable and prioritized, as shown in Figure 44. The six sources are divided as follows: three sources are claimed by Port 3 lines P33–P31, two by the counter/timers, and one by LBD (seeTable 21). The Interrupt Mask Register, globally or individually, enables or disables the six interrupt requests.

For 32-kHz crystal operation, an external feedback resistor (Rf) and a serial resistor (Rd) are required. See Figure 45.

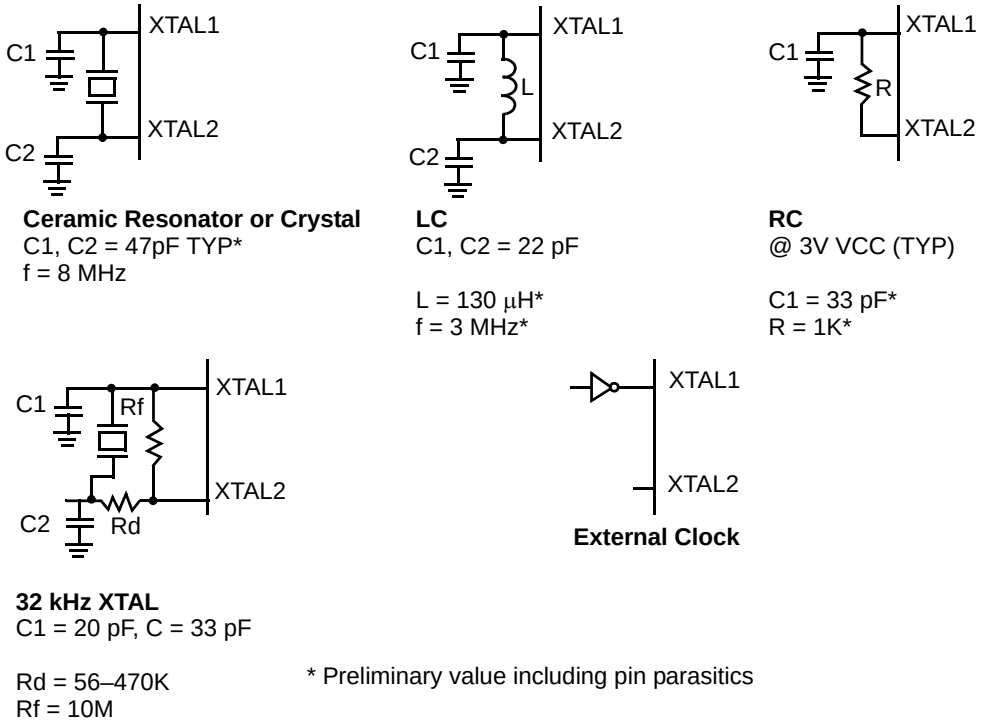

Figure 45. Oscillator Configuration

The crystal needs to be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (see Figure 45).

Power-On Reset (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows V_{CC} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status including waking up from V_{LV} Standby
- Stop-Mode Recovery (if D5 of SMR = 1)
- WDT Time-Out

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, and LC oscillators).

HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. STOP Mode is terminated only by a reset (such as WDT time-out), POR, SMR, or external reset. This termination causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, you need to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To execute this action, you must execute a NOP (op code = FFH) immediately before the appropriate sleep instruction. For example:

```
FF      NOP         ; clear the pipeline
6F      STOP        ; enter STOP Mode
```

or

```
FF      NOP         ; clear the pipeline
7F      HALT        ; enter HALT Mode
```

Port Configuration Register (PCON)

The PCON register configures the comparator output on Port 3. It is located in the expanded register 2 at Bank F, location 00, as shown in Figure 46.

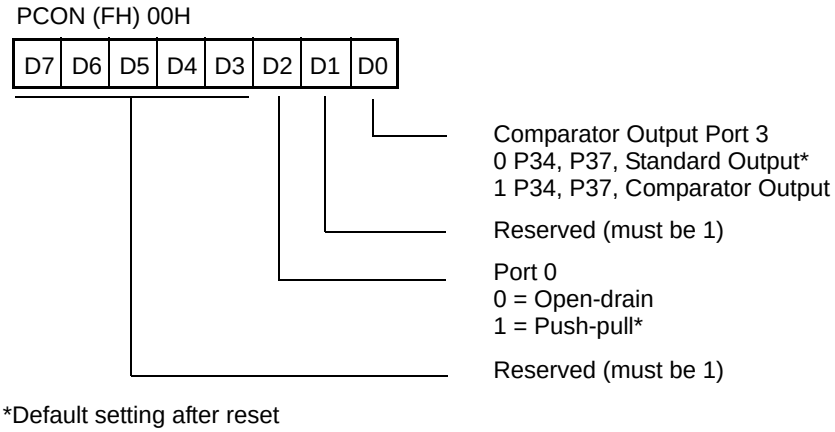

Figure 46. Port Configuration Register (PCON)—Write Only

Comparator Output Port 3 (D0)

Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the port to its standard (/O configuration.

Port 0 Output Mode (D2)

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

Stop-Mode Recovery Register (SMR)

This register selects the clock divide value and determines the mode of Stop-Mode Recovery (Figure 47). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level at the XOR-gate input is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4, or the SMR register, specify the source of the Stop-Mode Recovery signal. Bit D0 determines if SCLK/TCLK (shown in Figure 48) are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.

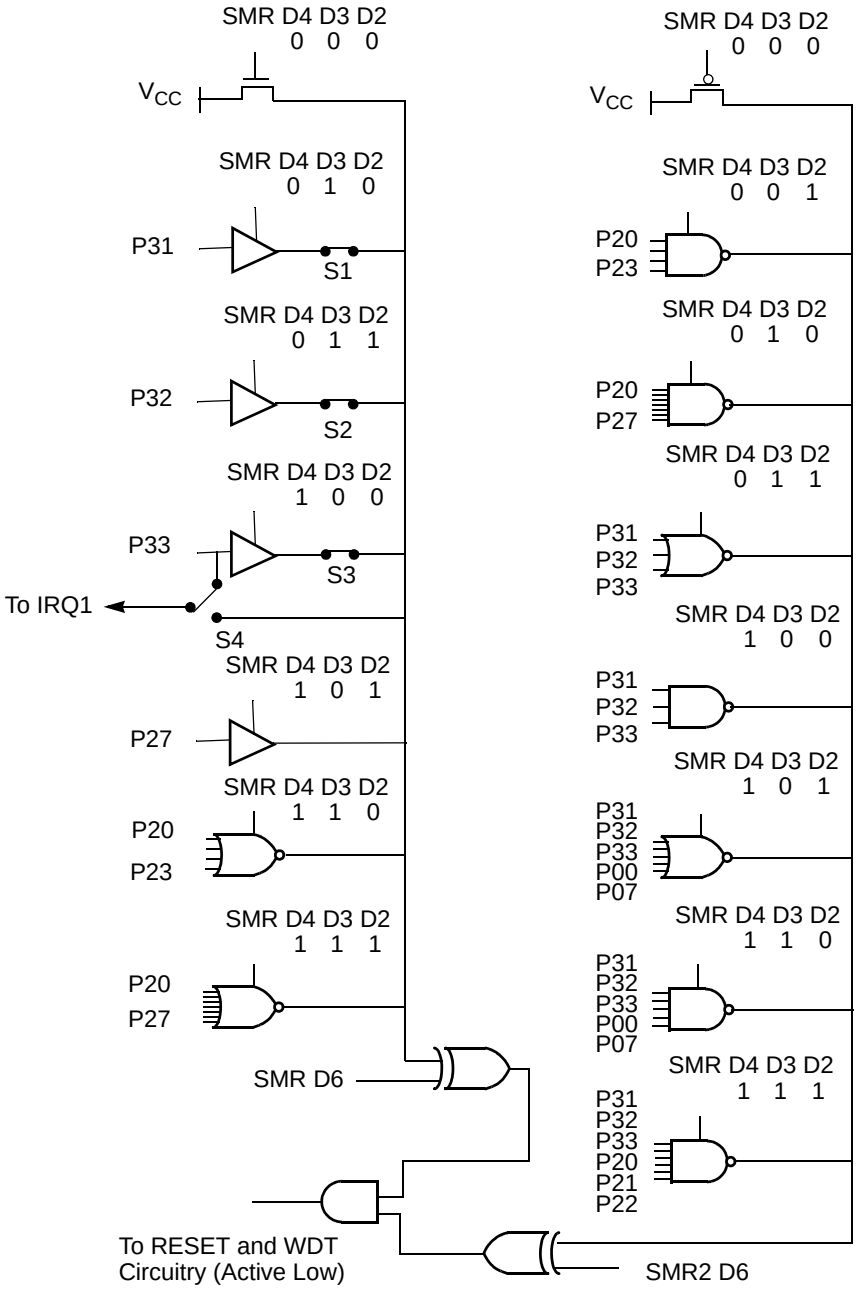

Figure 49. Stop-Mode Recovery Source

Customer Feedback Form

Z86D86 28-Pin Low-Voltage OTP Microcontroller

If you experience any problems while operating this product, or if you note any inaccuracies while reading this product specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	email

Product Information

Serial # or Board Fab #/Rev #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126-3432
Fax: (408) 558-8300

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.

_____

_____

_____