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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LVD, POR, WDT
Number of I/O	23
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	237 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86d8608ssc00tr

Table of Contents

List of Tables

T16 Common Control Register" on page 39). Other edge-detect and IRQ modes are described in Table 7.

Table 7. Pin Assignments

Pin	I/O	C/T	Comp.	Int.
Pref1			RF1	
P31	IN	IN	AN1	IRQ2
P32	IN		AN2	IRQ0
P33	IN		RF2	IRQ1
P34	OUT	T8	AO1	
P35	OUT	T16		
P36	OUT	T8/16		
P37	OUT		AO2	
P20	I/O	IN		

Port 3 also provides output for the counter/timers and the AND/OR logic. Control is performed by programming bits D5–D4 of CTR1 and bit 0 of CTR2.

Comparator Inputs

In analog mode, P31 and P32 have a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as indicated in Figure 8 on page 15. In digital mode, P33 is used as D3 of the Port 3 input register, which then generates IRQ1.

Note: Comparators are powered down by entering STOP Mode. For P31–P33 to be used in a Stop-Mode Recovery source, these inputs must be placed into digital mode.

Comparator Outputs

These outputs can be programmed to output on P34 and P37 through the PCON register (Figure 9).

Functional Description

The Z86D86 incorporates special functions to enhance the Z8's functionality in consumer and battery-operated applications.

Program Memory

The Z86D86 family addresses 32 KB of internal program memory. The first twelve bytes are reserved for interrupt vectors. These locations contain the five 16-bit vectors that correspond to the five available interrupts.

RAM

The Z86D86 device has 237 bytes of RAM that make up the register file.

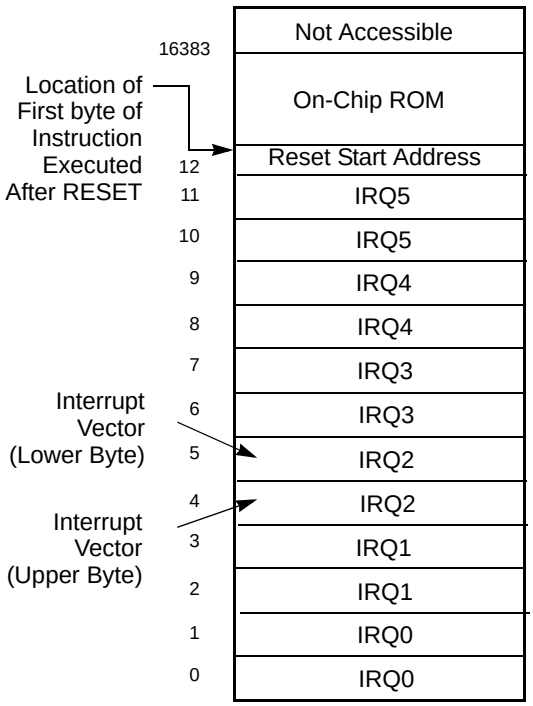


Figure 10. Program Memory Map (32K ROM)

Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as

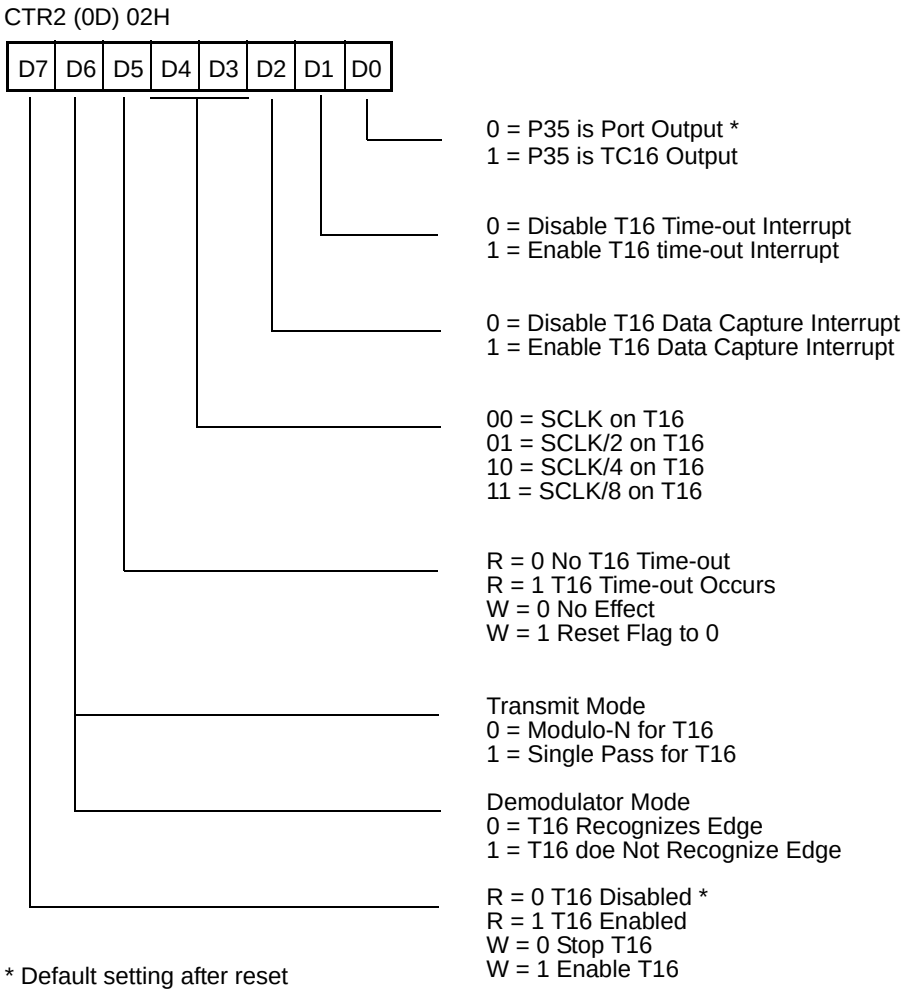


Figure 15. T16 Control Register—(0D) 2H: Read/Write Except Where Noted

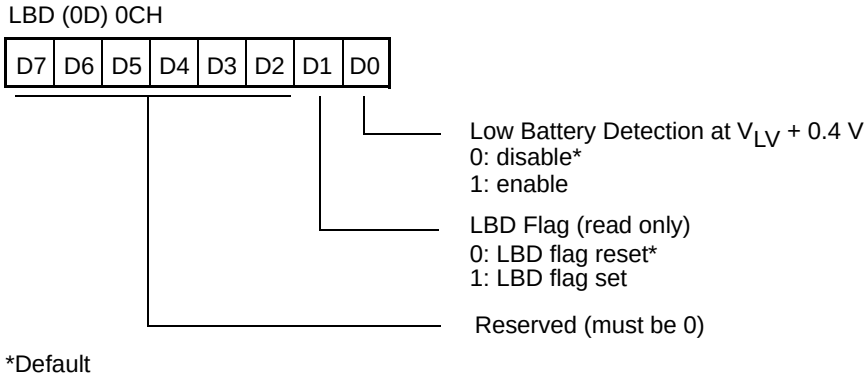
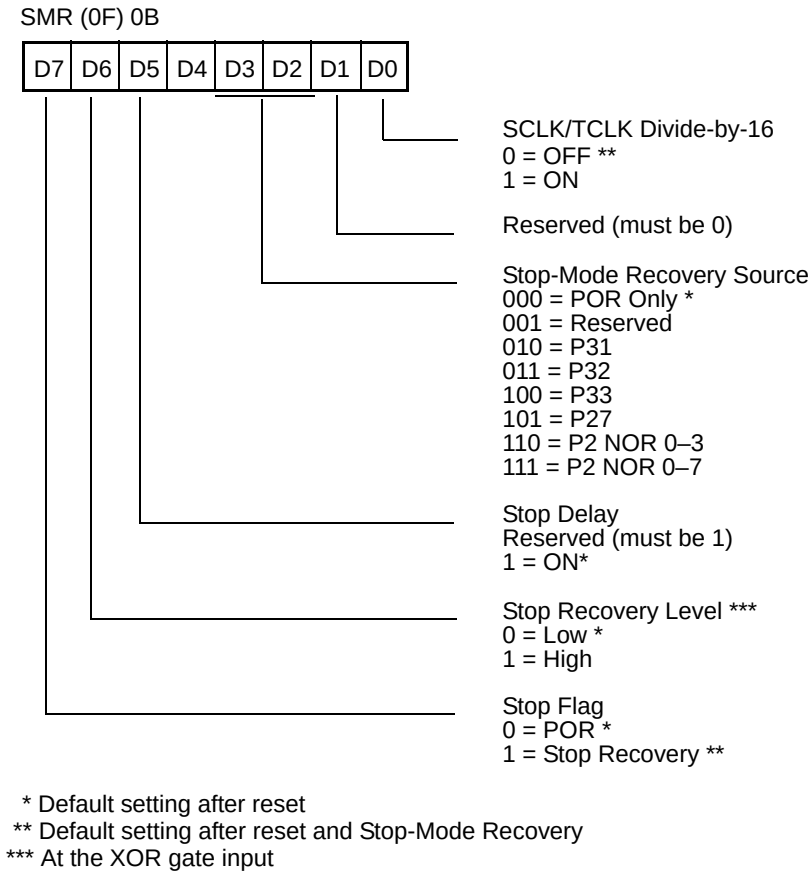


Figure 16. Low Battery Detection

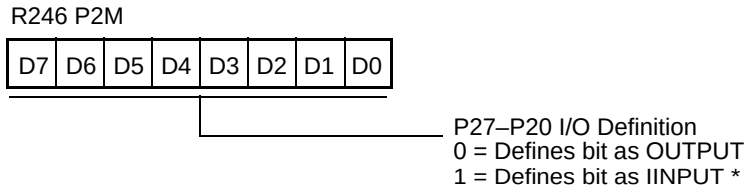
Expanded Register File Control Registers (0F)

Figure 17 through Figure 30 show the expanded register file control registers (0F).



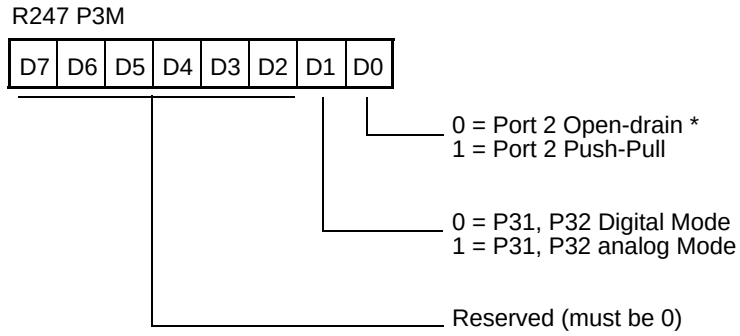
* Default setting after reset
** Default setting after reset and Stop-Mode Recovery
*** At the XOR gate input

Figure 17. Stop-Mode Recovery Register—(0F) 0BH: D6–D0 = Write Only, D7 = Read Only



*Default setting after reset

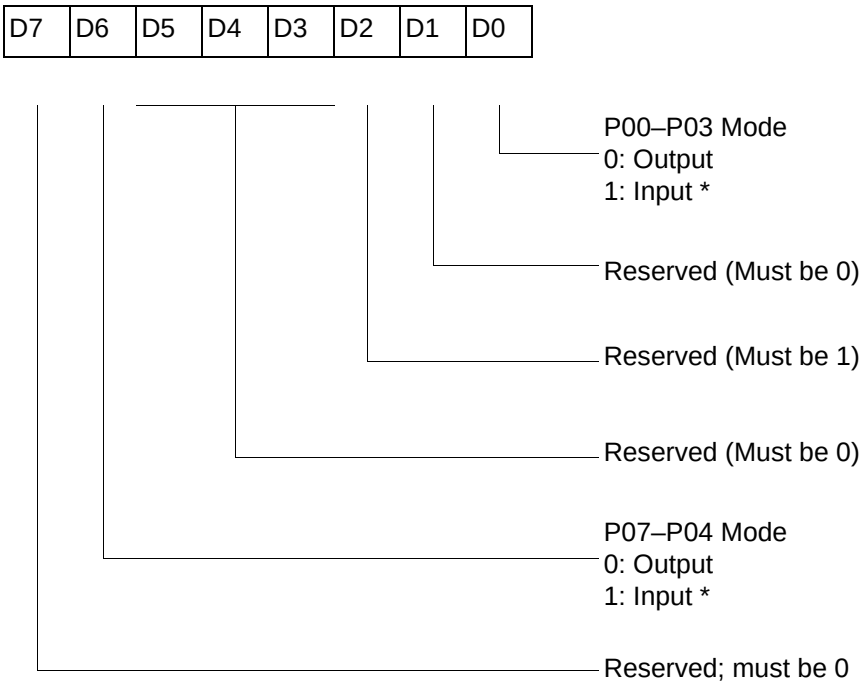
Figure 21. Port 2 Mode Register—F6H: Write Only



*Default setting after reset

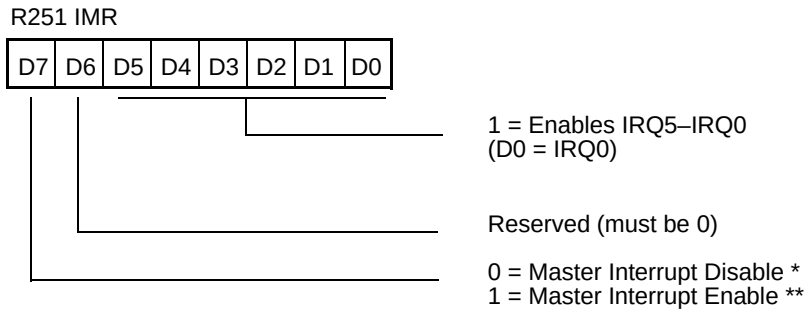
Figure 22. Port 3 Mode Register—F7H: Write Only

R248 P01M



* Default setting after reset; only P00, P01 and P07 are available on 20-pin configurations.

Figure 23. Port 0 and 1 Mode Register—F8H: Write Only



* Default setting after reset
** Only by using E1, D1 instruction. D1 is required before changing the IMR register.

Figure 26. Interrupt Mask Register—FBH: Read/Write

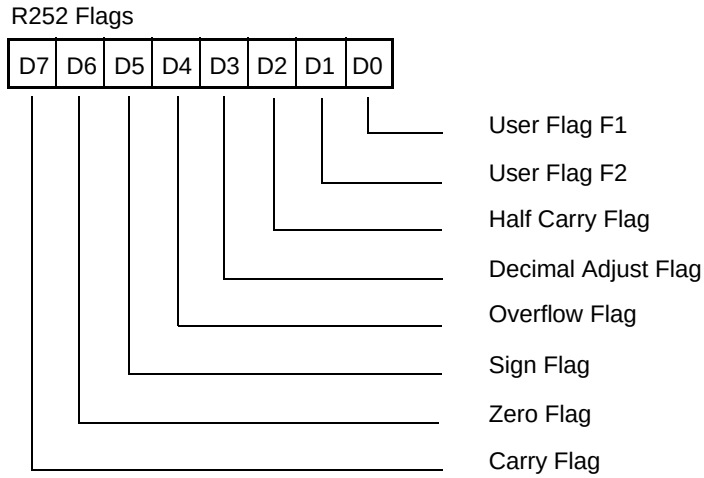


Figure 27. Flag Register—FCH: Read/Write

Counter/Timer Registers

Table 8 describes the expanded register group D.

Table 8. Expanded Register Group D

(D)0Ch	LVD
(D)0Bh	HI8
(D)0Ah	LO8
(D)09h	HI16
(D)08h	LO16
(D)07h	TC16H
(D)06h	TC16L
(D)05h	TC8H
(D)04h	TC8L
(D)03h	Reserved
(D)02h	CTR2
(D)01h	CTR1
(D)00h	CTR0

Register Description

LBD(D)0Ch—Low Battery Detection Register

Bit 0 enables/disables the Low Battery Detection Circuit. Bit 1 flags if low battery is detected. Interrupt 5 is triggered when the flag bit is set, given that IRQ5 is not masked. See Table 9.

Note: The LVD flag will be valid after enabling the detection for 20 μS (design estimation, not tested in production). LVD does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

Table 19. CTR1(D)01h Register (Continued)

Field	Bit Position		Value	Description
Transmit_Submode/Glitch_Filter	----32--	R/W		Transmit Mode
			00	Normal Operation
			01	Ping-Pong Mode
			10	T16_Out = 0
			11	T16_Out = 1
				Demodulation Mode
			00	No Filter
			01	4 SCLK Cycle
			10	8 SCLK Cycle
			11	Reserved
Initial_T8_Out/Rising Edge	------1-			Transmit Mode
		R/W	0	T8_OUT is 0 Initially
			1	T8_OUT is 1 Initially
				Demodulation Mode
		R	0	No Rising Edge
			1	Rising Edge Detected
		W	0	No Effect
			1	Reset Flag to 0
Initial_T16_Out/Falling_Edge	-------0			Transmit Mode
		R/W	0	T16_OUT is 0 initially.
			1	T16_OUT is 1 initially.
				Demodulation Mode
		R	0	No Falling Edge
			1	Falling Edge Detected
		W	0	No Effect
			1	Reset Flag to 0

Note:
*Default upon Power-On Reset

Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

P36_Out/Demodulator_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

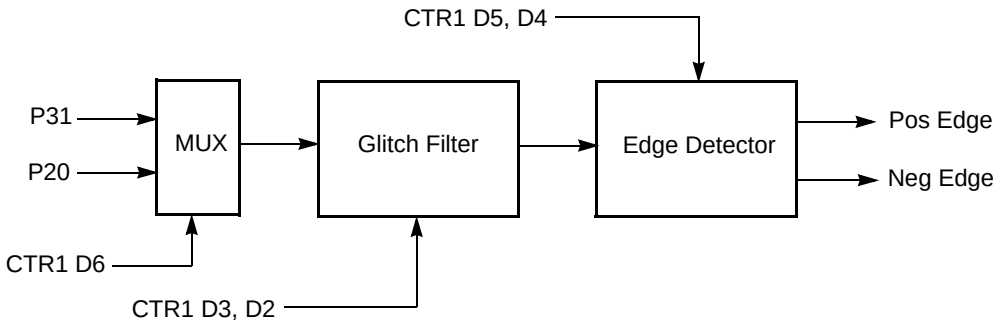


Figure 32. Glitch Filter Circuitry

Eight-Bit Counter/Timer Circuits

Figure 33 shows the 8-bit counter/timer circuits.

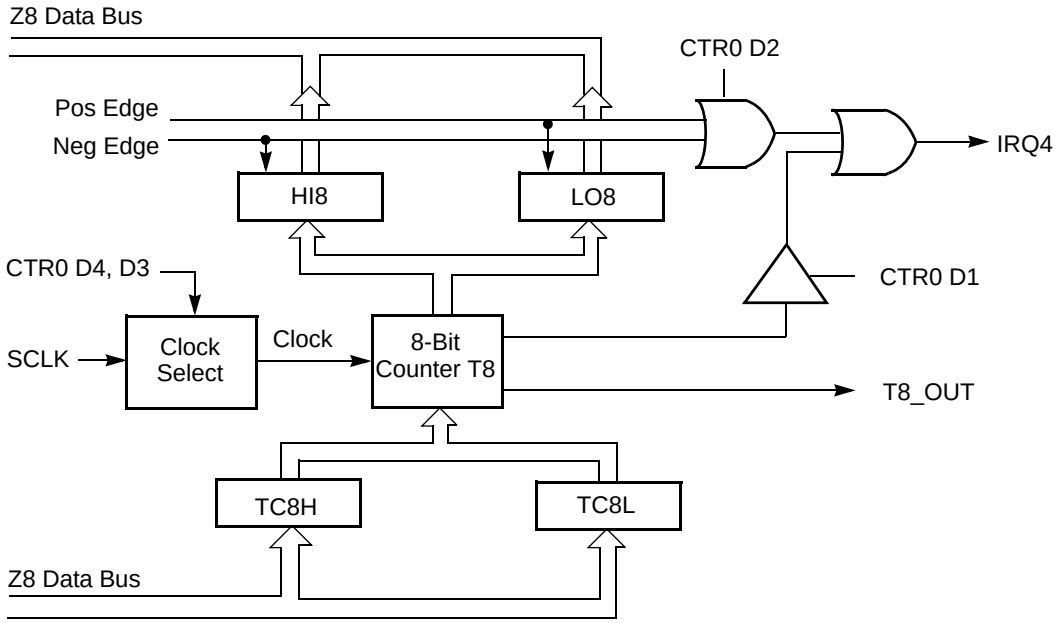


Figure 33. 8-Bit Counter/Timer Circuits

Sixteen-Bit Counter/Timer Circuits

Figure 39 shows the 16-bit counter/timer circuits.

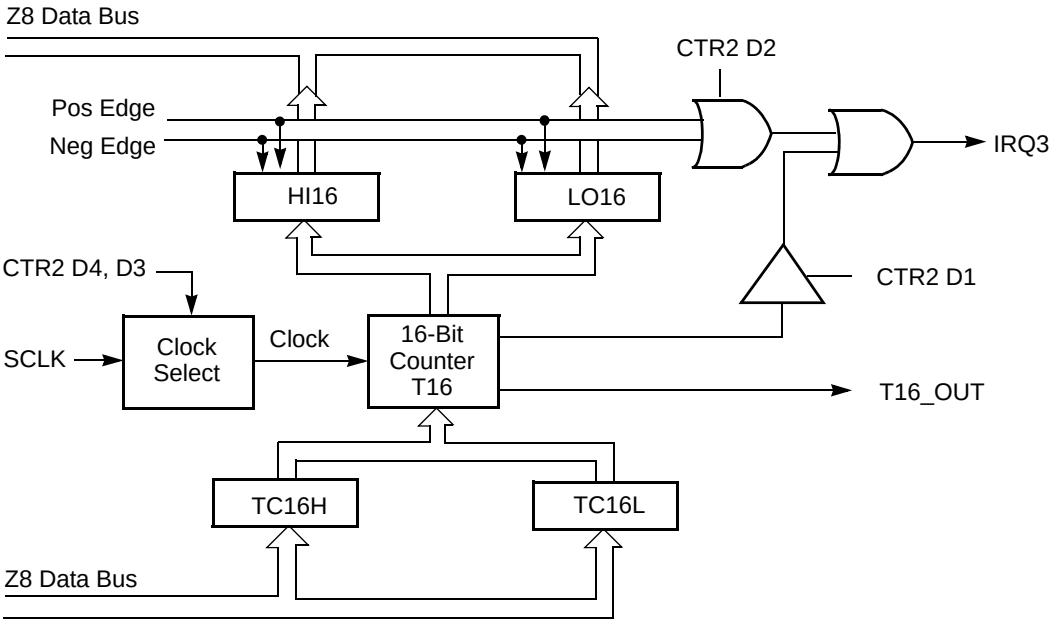


Figure 39. 16-Bit Counter/Timer Circuits

T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16, when not enabled, is dependent on CTR1, D0. If the result is a 0, T16_OUT is a 1; if it is a 1, T16_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H * 256 + TC16L is loaded, and T16_OUT is switched to its initial value (CTR1, D0). When T16 counts down to 0, T16_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2, D1), and a status bit (CTR2, D5) is set.

Note: Global interrupts override this function as described in “Interrupts” on page 54.

If T16 is in Single-Pass Mode, T16 is stopped at this point (see Figure 40). If T16 is in Modulo-N Mode, T16 is loaded with TC16H * 256 + TC16L and the counting continues (see Figure 41).

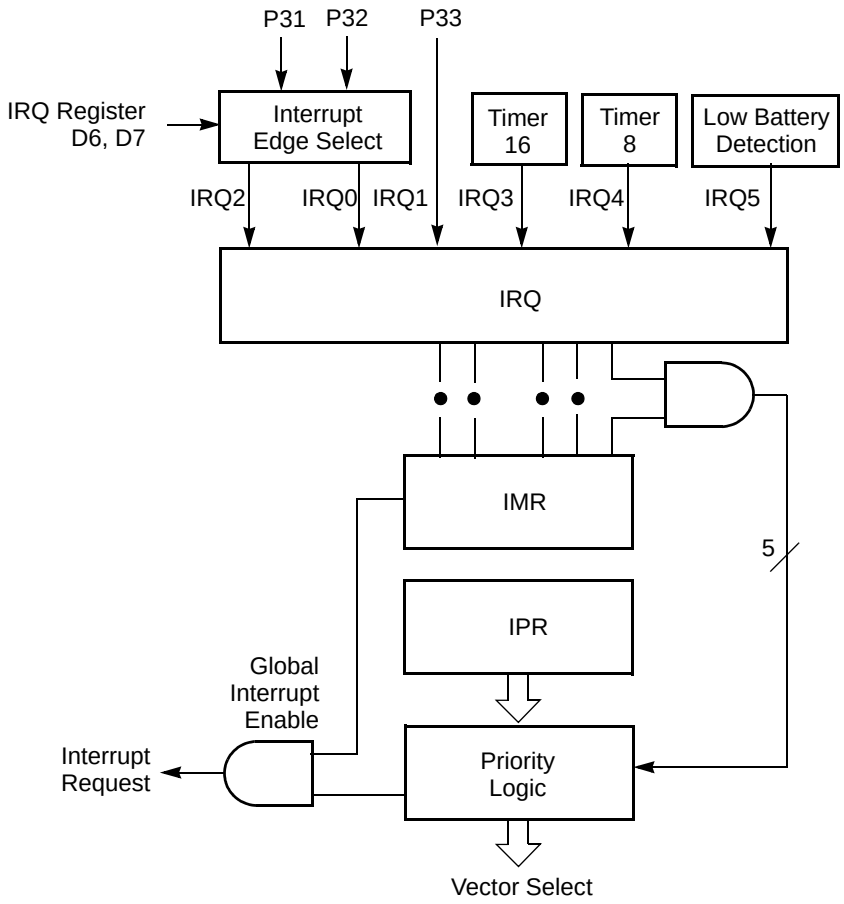


Figure 44. Interrupt Block Diagram

Table 21. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ0	P32	0,1	External (P32), Rising Falling Edge Triggered
IRQ1	P33	2,3	External (P33), Falling Edge Triggered
IRQ2	P31, T_{IN}	4,5	External (P31), Rising Falling Edge Triggered
IRQ3	T16	6,7	Internal
IRQ4	T8	8,9	Internal
IRQ5	LBD	10,11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority Register. An interrupt machine cycle is activated when an interrupt request is granted. As a result, all subsequent interrupt are disabled, and the Program Counter and Status Flags are saved. The cycle then branches to the program memory vector location reserved for that interrupt. All Z86D86 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked, and the Interrupt Request register is polled to determine which of the interrupt requests require service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered; all are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in Table 22.

Table 22. IRQ Register*

IRQ		Interrupt Edge	
D7	**D6**	**IRQ2 (P31)**	**IRQ0 (P32)**
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge
*In stop mode, the comparators are turned off.

Clock

The Z86D86 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86D86 on-chip oscillator can be driven with a low-cost RC network or other suitable external clock source.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, and LC oscillators).

HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 µA or less. STOP Mode is terminated only by a reset (such as WDT time-out), POR, SMR, or external reset. This termination causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, you need to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To execute this action, you must execute a NOP (op code = FFH) immediately before the appropriate sleep instruction. For example:

```
FF      NOP         ; clear the pipeline
6F      STOP        ; enter STOP Mode
```

or

```
FF      NOP         ; clear the pipeline
7F      HALT        ; enter HALT Mode
```

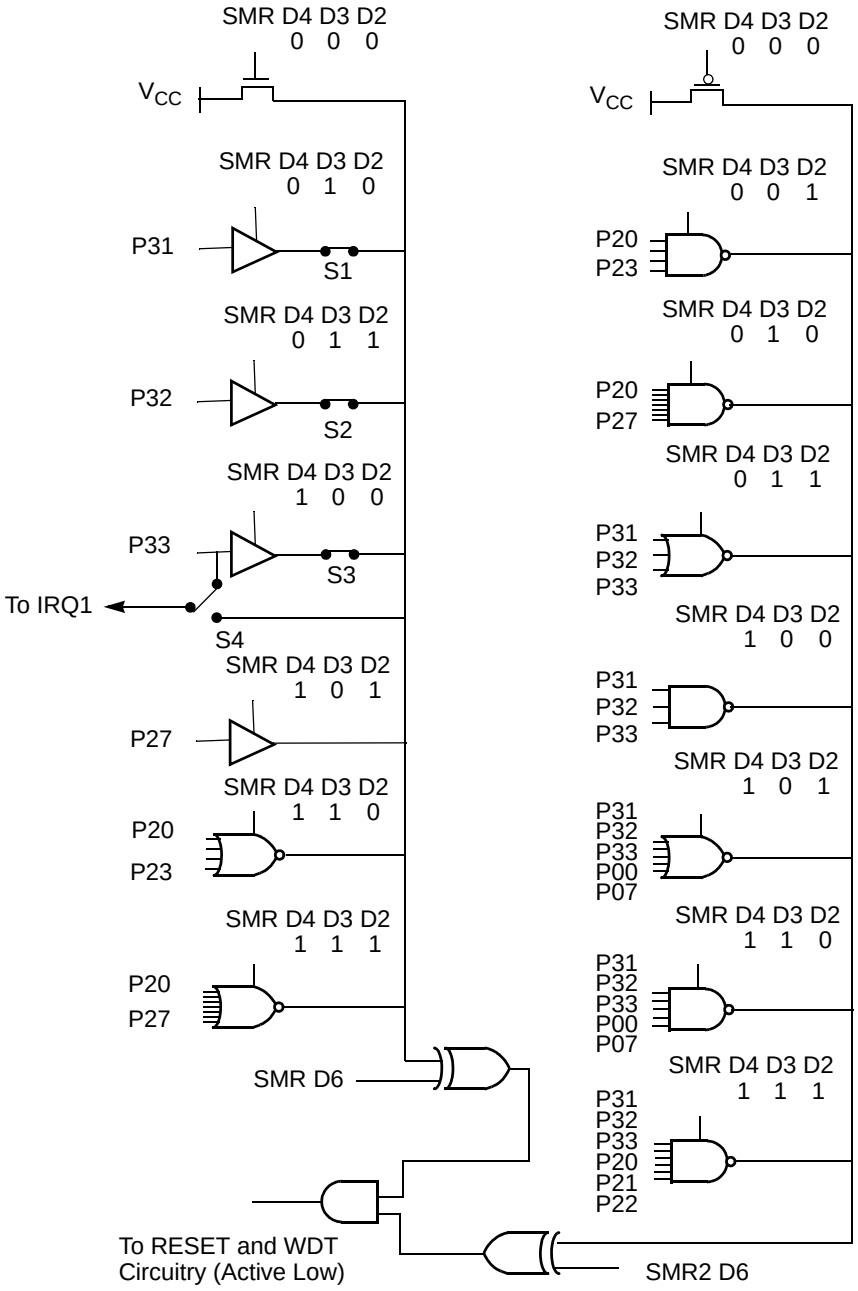
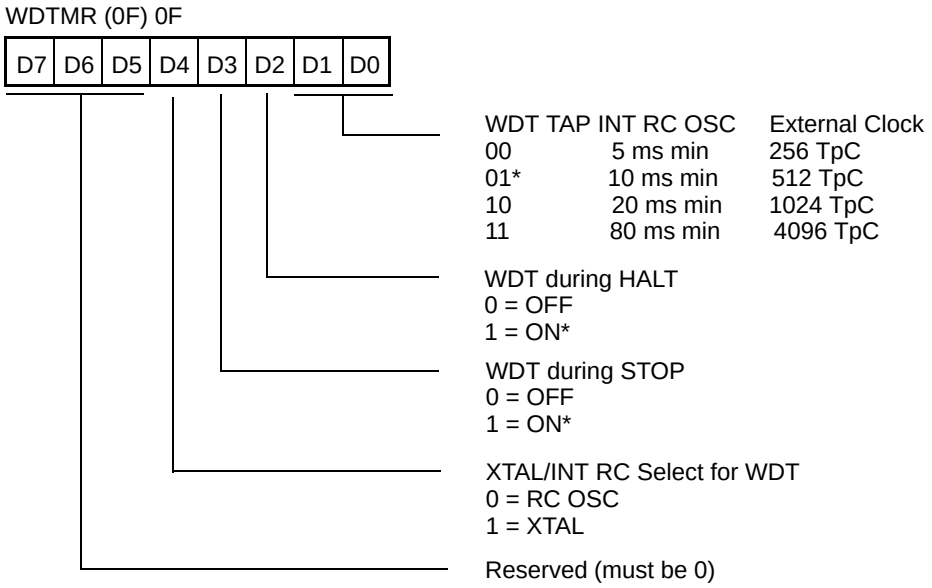


Figure 49. Stop-Mode Recovery Source



* Default setting after reset

Figure 51. Watch-Dog Timer Mode Register—Write Only

WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as indicated in Table 25.

Table 25. WDT Time Select*

D1	D0	Time-Out of Internal RC OSC	Time-Out of XTAL Clock
0	0	5 ms min	256 TpC
0	1	10 ms min	512 TpC
1	0	20 ms min	1024 TpC
1	1	80 ms min	4096 TpC

Notes:
*TpC = XTAL clock cycle. The default on reset is 10 ms.

WDTMR During HALT (D2)

This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

Mask Selectable Options

There are six Mask Selectable Options to choose from based on ROM code requirements. These are listed in Table 26.

Table 26. Mask Selectable Options

RC/Other	RC/XTAL
32 kHz XTAL	On/Off
Port 04–07 Pull-Ups	On/Off
Port 00–03 Pull-Ups	On/Off
Port 20–27 Pull-Ups	On/Off
Port 0:0–3 Mouse Mode 0.4 V_{CC} Trip	On/Off

Low Voltage/Standby

An on-chip Voltage Comparator checks that the V_{CC} is at the required level for correct operation of the device. Reset is globally driven when V_{CC} falls below V_{LV}. A further small drop in V_{CC} causes the XTAL1 and XTAL2 circuitry to stop the crystal or resonator clock. Typical low-voltage power consumpion in this Low Voltage Standby mode (I_{LV}) is about 100 µA. If the V_{CC} is allowed to stay above Vram, the RAM content is preserved. When the power level is returned to above V_{LV}, the device performs a POR and functions normally.

Low Battery Detection and Flag

A Low Battery Detection circuit can be used to signal dropping voltage levels. Expanded Register Bank 0Dh register 0Ch bit 0 and 1 are used for this option.

Bit D0 is used to enable/disable this function.

Bit D1 is the status flag bit of this LBD.

The minimum operating voltage varies with the temperature and operating frequency, while VLV varies with temperature only.