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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Active |
| Type | Fixed Point |
| Interface | Host Interface, Serial Port |
| Clock Rate | 75MHz |
| Non-Volatile Memory | External |
| On-Chip RAM | 80kB |
| Voltage - I/O | 3.30V |
| Voltage - Core | 2.50V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/adsp-2185mkstz-300 |

# ADSP-2185M* PRODUCT PAGE QUICK LINKS

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**Application Notes**

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- AN-334: Digital Signal Processing Techniques
- AN-524: ADV601/ADV611 Bin Width Calculation in ADSP-21xx DSP
- EE-06: ADSP-21xx Serial Port Startup Issues
- EE-100: ADSP-218x External Overlay Memory
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- EE-103: Performing Level Conversion Between 5v and 3.3v IC's
- EE-104: Setting Up Streams with the VisualDSP Debugger
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- EE-133: Converting From Legacy Architecture Files To Linker Description Files for the ADSP-218x
- EE-139: Interfacing the ADSP-2191 to an AD7476 via the SPI Port
- EE-142: Autobuffering, C and FFTs on the ADSP-218x
- EE-144: Creating a Master-Slave SPI Interface Between Two ADSP-2191 DSPs
- EE-145: SPI Booting of the ADSP-2191 using the Atmel AD25020N on an EZ-KIT Lite Evaluation Board

## DESIGN RESOURCES

- ADSP-2185M Material Declaration
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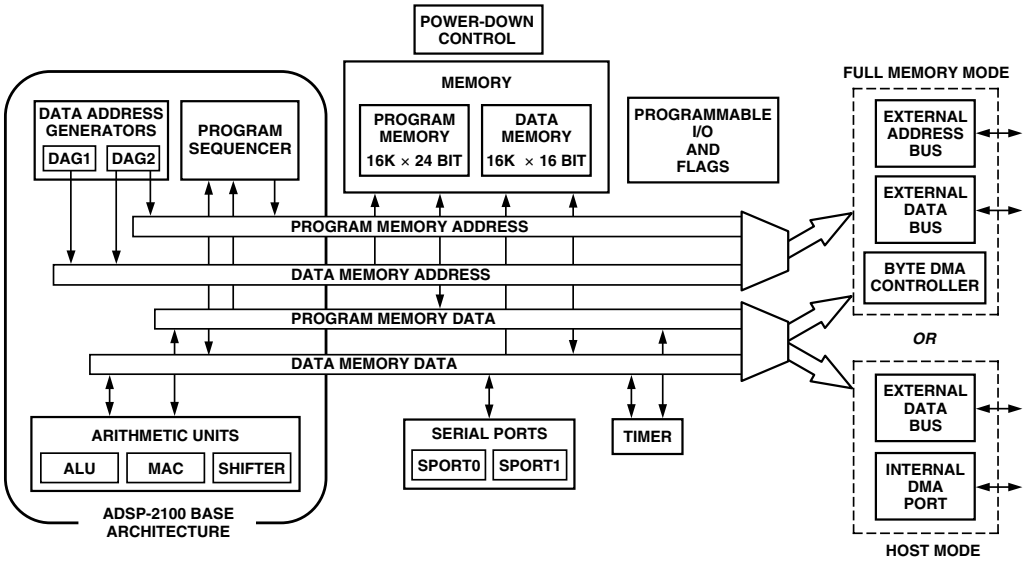



*Figure 1. Functional Block Diagram*

**ARCHITECTURE OVERVIEW**

The ADSP-2185M instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2185M assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1 is an overall block diagram of the ADSP-2185M. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations.

The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2185M executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2185M to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2185M can fetch an operand from program memory and the next instruction in the same cycle.

In lieu of the address and data bus for external memory connection, the ADSP-2185M may be configured for 16-bit Internal DMA port (IDMA port) connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low-cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of

external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2185M to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2185M can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal. The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation.

Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2185M provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, eight flags are programmable as inputs or outputs, and three flags are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) decrements every n processor cycle, where n is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

**Serial Ports**

The ADSP-2185M incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2185M SPORTs. For additional information on Serial Ports, refer to the *ADSP-2100 Family User's Manual.*

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulsewidths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time- division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the FI and FO signals. The internally generated serial clock may still be used in this configuration.

**PIN DESCRIPTIONS**

The ADSP-2185M is available in a 100-lead LQFP package and a 144-Ball Mini-BGA package. In order to maintain maximum functionality and reduce package size and pin count, some serial port, programmable flag, interrupt and external bus pins have dual, multiplexed functionality. The external bus pins are configured during $\overline{RESET}$ only, while serial port pins are software configurable during program execution. Flag and interrupt functionality is retained concurrently on multiplexed pins. In cases where pin functionality is reconfigurable, the default state is shown in plain text; alternate functionality is shown in italics.

**Memory Interface Pins**

The ADSP-2185M processor can be used in one of two modes: Full Memory Mode, which allows BDMA operation with full external overlay memory and I/O capability, or Host Mode, which allows IDMA operation with limited external addressing capabilities. The operating mode is determined by the state of the Mode C pin during $\overline{\text{RESET}}$ and cannot be changed while the processor is running.

The following tables list the active signals at specific pins of the DSP during either of the two operating modes (Full Memory or Host). A signal in one table shares a pin with a signal from the other table, with the active signal determined by the mode set. For the shared pins and their alternate signals (e.g., A4/IAD3), refer to the package pinout tables.

**Full Memory Mode Pins (Mode C = 0)**

| Pin Name | # of Pins | I/O | Function |
|---|---|---|---|
| A13:0 | 14 | O | Address Output Pins for Program, Data, Byte, and I/O Spaces |
| D23:0 | 24 | I/O | Data I/O Pins for Program, Data, Byte, and I/O Spaces (8 MSBs are also used as Byte Memory Addresses.) |

**Host Mode Pins (Mode C = 1)**

| Pin Name | # of Pins | I/O | Function |
|---|---|---|---|
| IAD15:0 | 16 | I/O | IDMA Port Address/Data Bus |
| A0 | 1 | O | Address Pin for External I/O, Program, Data, or Byte Access[1] |
| D23:8 | 16 | I/O | Data I/O Pins for Program, Data, Byte, and I/O Spaces |
| $\overline{\text{IWR}}$ | 1 | I | IDMA Write Enable |
| $\overline{\text{IRD}}$ | 1 | I | IDMA Read Enable |
| IAL | 1 | I | IDMA Address Latch Pin |
| $\overline{\text{IS}}$ | 1 | I | IDMA Select |
| $\overline{\text{IACK}}$ | 1 | O | IDMA Port Acknowledge Configurable in Mode D; Open Drain |

NOTE

[1]In Host Mode, external peripheral addresses can be decoded using the A0, $\overline{\text{CMS}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{IOMS}}$ signals.

**Terminating Unused Pins**

The following table shows the recommendations for terminating unused pins.

**Pin Terminations**

| Pin Name | I/O 3-State (Z) | Reset State | Hi-Z* Caused By | Unused Configuration |
|---|---|---|---|---|
| XTAL | I | I | | Float |
| CLKOUT | O | O | | Float |
| A13:1 or | O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| IAD 12:0 | I/O (Z) | Hi-Z | $\overline{IS}$ | Float |
| A0 | O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| D23:8 | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| D7 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IWR}$ | I | I | | High (Inactive) |
| D6 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IRD}$ | I | I | $\overline{BR}$, $\overline{EBR}$ | High (Inactive) |
| D5 or | I/O (Z) | Hi-Z | | Float |
| IAL | I | I | | Low (Inactive) |
| D4 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IS}$ | I | I | | High (Inactive) |
| D3 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IACK}$ | | | | Float |
| D2:0 or | I/O (Z) | Hi-Z | $\overline{BR}$, $\overline{EBR}$ | Float |
| IAD15:13 | I/O (Z) | Hi-Z | $\overline{IS}$ | Float |
| $\overline{PMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{DMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{BMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{IOMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{CMS}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{RD}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{WR}$ | O (Z) | O | $\overline{BR}$, $\overline{EBR}$ | Float |
| $\overline{BR}$ | I | I | | High (Inactive) |
| $\overline{BG}$ | O (Z) | O | EE | Float |
| $\overline{BGH}$ | O | O | | Float |
| $\overline{IRQ2}$/*PF7* | I/O (Z) | I | | Input = High (Inactive) or Program as Output, Set to 1, Let Float |
| $\overline{IRQL1}$/*PF6* | I/O (Z) | I | | Input = High (Inactive) or Program as Output, Set to 1, Let Float |
| $\overline{IRQL0}$/*PF5* | I/O (Z) | I | | Input = High (Inactive) or Program as Output, Set to 1, Let Float |
| $\overline{IRQE}$/*PF4* | I/O (Z) | I | | Input = High (Inactive) or Program as Output, Set to 1, Let Float |
| SCLK0 | I/O | I | | Input = High or Low, Output = Float |
| RFS0 | I/O | I | | High or Low |
| DR0 | I | I | | High or Low |
| TFS0 | I/O | I | | High or Low |
| DT0 | O | O | | Float |
| SCLK1 | I/O | I | | Input = High or Low, Output = Float |
| RFS1/$\overline{IRQ0}$ | I/O | I | | High or Low |
| DR1/FI | I | I | | High or Low |
| TFS1/$\overline{IRQ1}$ | I/O | I | | High or Low |
| DT1/FO | O | O | | Float |
| $\overline{EE}$ | I | I | | Float |
| $\overline{EBR}$ | I | I | | Float |
| $\overline{EBG}$ | O | O | | Float |
| $\overline{ERESET}$ | I | I | | Float |
| $\overline{EMS}$ | O | O | | Float |
| $\overline{EINT}$ | I | I | | Float |
| ECLK | I | I | | Float |
| ELIN | I | I | | Float |
| ELOUT | O | O | | Float |

NOTES

*Hi-Z = High Impedance.

1. If the CLKOUT pin is not used, turn it OFF, using CLKODIS in SPORT0 autobuffer control register.
2. If the Interrupt/Programmable Flag pins are not used, there are two options: Option 1: When these pins are configured as INPUTS at reset and function as interrupts and input flag pins, pull the pins High (inactive). Option 2: Program the unused pins as OUTPUTS, set them to 1, prior to enabling interrupts, and let pins float.
3. All bidirectional pins have three-stated outputs. When the pin is configured as an output, the output is Hi-Z (high impedance) when inactive.
4. CLKIN, $\overline{RESET}$, and PF3:0/MODE D:A are not included in the table because these pins must be used.

**Interrupts**

The interrupt controller allows the processor to respond to the 11 possible interrupts and reset with minimum overhead. The ADSP-2185M provides four dedicated external interrupt input pins: $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, and $\overline{IRQE}$ (shared with the PF7:4 pins). In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FI and FO, for a total of six external interrupts. The ADSP-2185M also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power- down and reset). The $\overline{IRQ2}$, $\overline{IRQ0}$, and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and $\overline{IRQE}$ is edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table I.

**Table I. Interrupt Priority and Interrupt Vector Addresses**

| Source Of Interrupt | Interrupt Vector Address (Hex) |
|---|---|
| Reset (or Power-Up with PUCR = 1) | 0000 (Highest Priority) |
| Power-Down (Nonmaskable) | 002C |
| $\overline{IRQ2}$ | 0004 |
| $\overline{IRQL1}$ | 0008 |
| $\overline{IRQL0}$ | 000C |
| SPORT0 Transmit | 0010 |
| SPORT0 Receive | 0014 |
| $\overline{IRQE}$ | 0018 |
| BDMA Interrupt | 001C |
| SPORT1 Transmit or $\overline{IRQ1}$ | 0020 |
| SPORT1 Receive or $\overline{IRQ0}$ | 0024 |
| Timer | 0028 (Lowest Priority) |

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2185M masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect serial port autobuffering or DMA transfers.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$ external interrupts to be either edge- or level-sensitive. The $\overline{IRQE}$ pin is an external edge sensitive interrupt and can be forced and cleared. The $\overline{IRQL0}$ and $\overline{IRQL1}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop, and subroutine nesting. The following instructions allow global enable or disable servicing of the interrupts (including power down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

*ENA INTS;*
*DIS INTS;*

When the processor is reset, interrupt servicing is enabled.

**LOW POWER OPERATION**

The ADSP-2185M has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power-Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

**Power-Down**

The ADSP-2185M processor has a low power feature that lets the processor enter a very low-power dormant state through hardware or software control. Following is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual*, "System Interface" chapter, for detailed information about the power-down feature.

- Quick recovery from power-down. The processor begins executing instructions in as few as 200 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power-down without affecting the lowest power rating and 200 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits approximately 4096 CLKIN cycles for the crystal oscillator to start or stabilize), and letting the oscillator run to allow 200 CLKIN cycle start-up.
- Power-down is initiated by either the power-down pin ($\overline{PWD}$) or the software power-down force bit. Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge-sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{RESET}$ pin also can be used to terminate power-down.
- Power-down acknowledge pin indicates when the processor has entered power-down.

**Idle**

When the ADSP-2185M is in the Idle Mode, the processor waits indefinitely in a low-power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. In Idle mode IDMA, BDMA and autobuffer cycle steals still occur.

**Slow Idle**
The IDLE instruction is enhanced on the ADSP-2185M to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction.

The format of the instruction is:

*IDLE (n);*

where *n* = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE (n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-2185M will remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE (n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

**SYSTEM INTERFACE**
Figure 2 shows typical basic system configurations with the ADSP-2185M, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories (mode-selectable). Programmable wait state generation allows the processor to connect easily to slow peripheral devices. The ADSP-2185M also provides four external interrupts and two serial ports or six external interrupts and one serial port. Host Memory Mode allows access to the full external data bus, but limits addressing to a single address bit (A0). Through the use of external hardware, additional system peripherals can be added in this mode to generate and latch address signals.

**Clock Signals**
The ADSP-2185M can be clocked by either a crystal or a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, nor operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual,* for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input must be left unconnected.

The ADSP-2185M uses an input clock with a frequency equal to half the instruction rate; a 37.50 MHz input clock yields a 13 ns processor cycle (which is equivalent to 75 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2185M includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

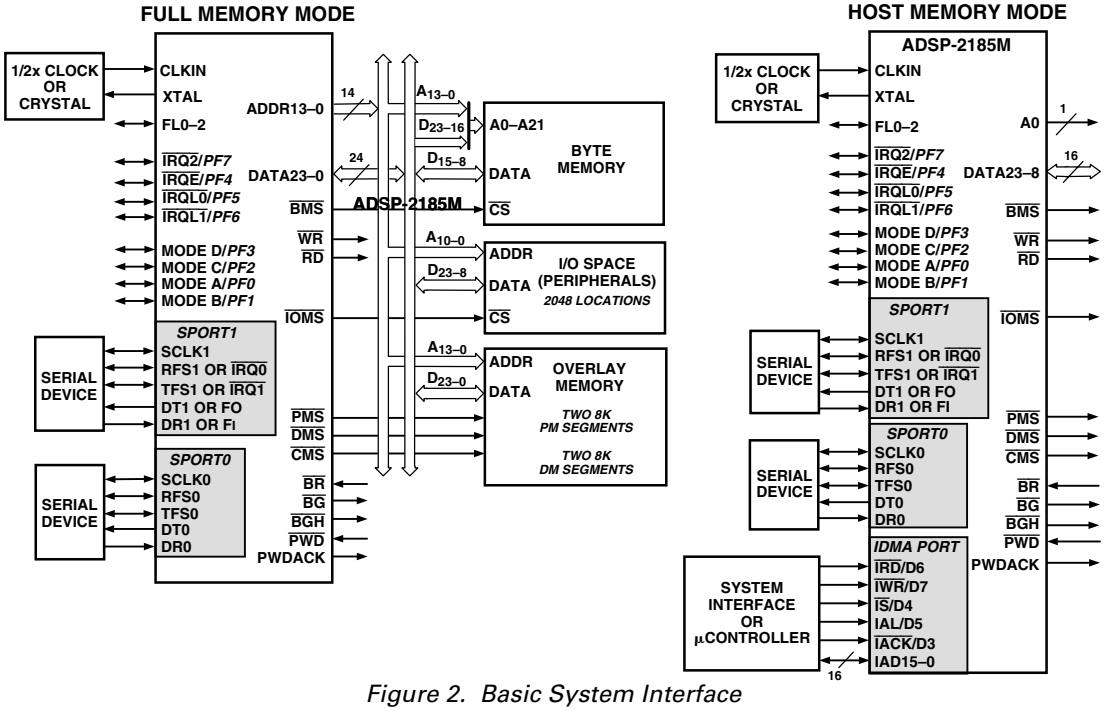



*Figure 2. Basic System Interface*

**Data Memory**

**Data Memory (Full Memory Mode)** is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2185M has 16K words on Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register and the wait state mode bit.

**Data Memory (Host Mode)** allows access to all internal memory. External overlay access is limited by a single external address line (A0).

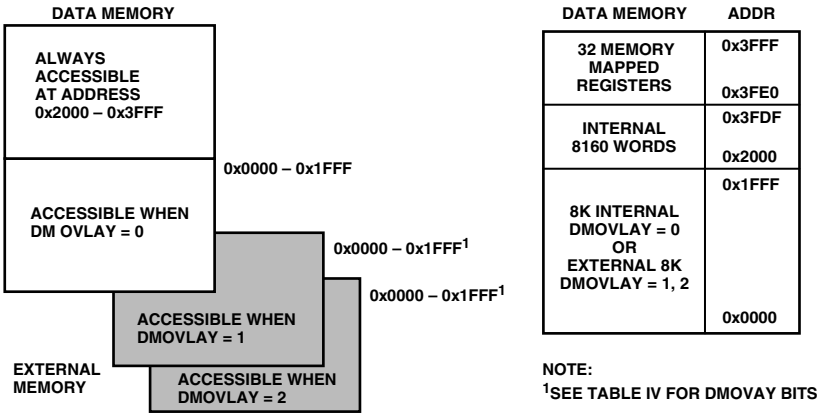



*Figure 5. Data Memory Map*

**Table IV. DMOVLAY Bits**

| DMOVLAY | Memory | A13 | A12:0 |
|---|---|---|---|
| 0 | Internal | Not Applicable | Not Applicable |
| 1 | External Overlay 1 | 0 | 13 LSBs of Address Between 0x2000 and 0x3FFF |
| 2 | External Overlay 2 | 1 | 13 LSBs of Address Between 0x2000 and 0x3FFF |

**Memory Mapped Registers (New to the ADSP-2185M)**

The ADSP-2185M has three memory mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait State Control, Programmable Flag and Composite Select Control, and System Control) provide the ADSP-2185M's wait state and $\overline{\text{BMS}}$ control features. Default bit values at reset are shown; if no value is shown, the bit is undefined at reset. Reserved bits are shown on a grey field. These bits should always be written with zeros.

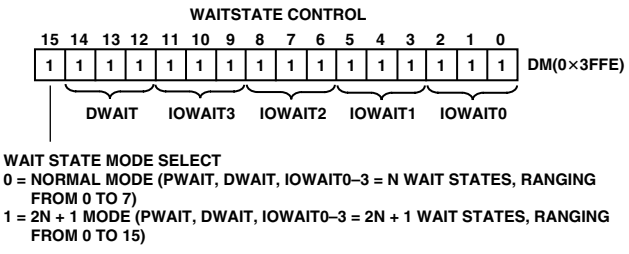



*Figure 6. Wait State Control Register*

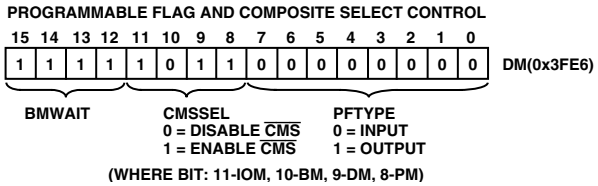



*Figure 7. Programmable Flag and Composite Control Register*

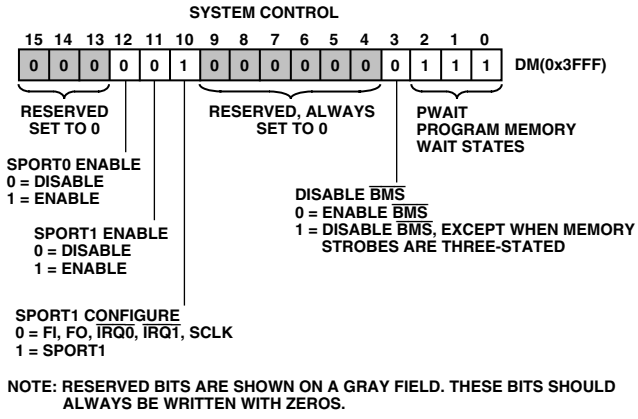



*Figure 8. System Control Register*

**I/O Space (Full Memory Mode)**

The ADSP-2185M supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers, IOWAIT0–3, which in combination with the wait state mode bit, specify up to 15 wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table V.

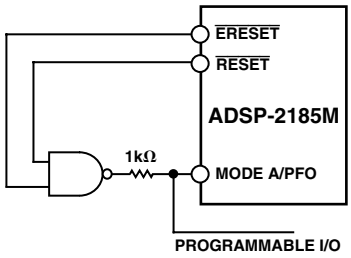



*Figure 12. Mode A Pin/EZ-ICE Circuit*

See the ADSP-2100 Family EZ-Tools data sheet for complete information on ICE products.

The ICE-Port interface consists of the following ADSP-2185M pins: $\overline{\text{EBR}}$, $\overline{\text{EINT}}$, EE, $\overline{\text{EBG}}$, ECLK, $\overline{\text{ERESET}}$, ELIN, $\overline{\text{EMS}}$, and ELOUT

These ADSP-2185M pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2185M and the connector must be kept as short as possible, no longer than 3 inches.

The following pins are also used by the EZ-ICE: $\overline{\text{BR}}$, $\overline{\text{BG}}$, $\overline{\text{RESET}}$, and GND.

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2185M in the target system. This causes the processor to use its $\overline{\text{ERESET}}$, $\overline{\text{EBR}}$, and $\overline{\text{EBG}}$ pins instead of the $\overline{\text{RESET}}$, $\overline{\text{BR}}$, and $\overline{\text{BG}}$ pins. The $\overline{\text{BG}}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

**Target Board Connector for EZ-ICE Probe**
The EZ-ICE connector (a standard pin strip header) is shown in Figure 13. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

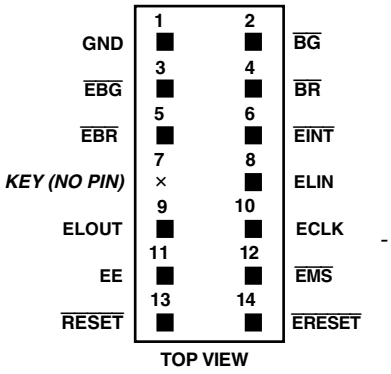



*Figure 13. Target Board Connector for EZ-ICE*

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—Pin 7 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

**Target Memory Interface**
For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

**PM, DM, BM, IOM, AND CM**
Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ- ICE may approach published worst-case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst-case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2185M ($\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$, and $\overline{\text{IOMS}}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

**Target System Interface Signals**
When the EZ-ICE board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{\text{RESET}}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{\text{BR}}$ signal.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{\text{RESET}}$ and $\overline{\text{BR}}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{\text{BR}}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{\text{BG}}$) is asserted by the EZ- ICE board's DSP.

# ADSP-2185M–SPECIFICATIONS

## RECOMMENDED OPERATING CONDITIONS

| Parameter | K Grade Min | K Grade Max | B Grade Min | B Grade Max | Unit |
|---|---|---|---|---|---|
| $V_{DDINT}$ | 2.37 | 2.63 | 2.25 | 2.75 | V |
| $V_{DDEXT}$ | 2.37 | 3.6 | 2.25 | 3.6 | V |
| $V_{INPUT}$[1] | $V_{IL}$ = –0.3 | $V_{IH}$ = +3.6 | $V_{IL}$ = –0.3 | $V_{IH}$ = +3.6 | V |
| $T_{AMB}$ | 0 | +70 | –40 | +85 | °C |

NOTES

[1]The ADSP-2185M is 3.3 V tolerant (always accepts up to 3.6 V max $V_{IH}$), but voltage compliance (on outputs, $V_{OH}$) depends on the input $V_{DDEXT}$; because $V_{OH}$ (max) ≈ $V_{DDEXT}$ (max). This applies to bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

Specifications subject to change without notice.

## ELECTRICAL CHARACTERISTICS

| Parameter | | Test Conditions | K/B Grades Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Hi-Level Input Voltage[1, 2] | @ $V_{DDINT}$ = max | 1.5 | | | V |
| $V_{IH}$ | Hi-Level CLKIN Voltage | @ $V_{DDINT}$ = max | 2.0 | | | V |
| $V_{IL}$ | Lo-Level Input Voltage[1, 3] | @ $V_{DDINT}$ = min | | | 0.7 | V |
| $V_{OH}$ | Hi-Level Output Voltage[1, 4, 5] | @ $V_{DDEXT}$ = min, $I_{OH}$ = –0.5 mA | 2.0 | | | V |
| | | @ $V_{DDEXT}$ = 3.0 V, $I_{OH}$ = –0.5 mA | 2.4 | | | V |
| | | @ $V_{DDEXT}$ = min, $I_{OH}$ = –100 µA[6] | $V_{DDEXT}$ – 0.3 | | | V |
| $V_{OL}$ | Lo-Level Output Voltage[1, 4, 5] | @ $V_{DDEXT}$ = min, $I_{OL}$ = 2 mA | | | 0.4 | V |
| $I_{IH}$ | Hi-Level Input Current[3] | @ $V_{DDINT}$ = max, $V_{IN}$ = 3.6 V | | | 10 | µA |
| $I_{IL}$ | Lo-Level Input Current[3] | @ $V_{DDINT}$ = max, $V_{IN}$ = 0 V | | | 10 | µA |
| $I_{OZH}$ | Three-State Leakage Current[7] | @ $V_{DDEXT}$ = max, $V_{IN}$ = 3.6 V[8] | | | 10 | µA |
| $I_{OZL}$ | Three-State Leakage Current[7] | @ $V_{DDEXT}$ = max, $V_{IN}$ = 0 V[8] | | | 10 | µA |
| $I_{DD}$ | Supply Current (Idle)[9] | @ $V_{DDINT}$ = 2.5, $t_{CK}$ = 15 ns | | 9 | | mA |
| $I_{DD}$ | Supply Current (Idle)[9] | @ $V_{DDINT}$ = 2.5, $t_{CK}$ = 13.3 ns | | 10 | | mA |
| $I_{DD}$ | Supply Current (Dynamic)[10] | @ $V_{DDINT}$ = 2.5, $t_{CK}$ = 15 ns[11], $T_{AMB}$ = 25°C | | 35 | | mA |
| $I_{DD}$ | Supply Current (Dynamic)[10] | @ $V_{DDINT}$ = 2.5, $t_{CK}$ = 13.3 ns[11], $T_{AMB}$ = 25°C | | 38 | | mA |
| $I_{DD}$ | Supply Current (Power-Down)[12] | @ $V_{DDINT}$ = 2.5, $T_{AMB}$ = 25°C in Lowest Power Mode | | 100 | | µA |
| $C_I$ | Input Pin Capacitance[3, 6] | @ $V_{IN}$ = 2.5 V, $f_{IN}$ = 1.0 MHz, $T_{AMB}$ = 25°C | | | 8 | pF |
| $C_O$ | Output Pin Capacitance[6, 7, 12, 13] | @ $V_{IN}$ = 2.5 V, $f_{IN}$ = 1.0 MHz, $T_{AMB}$ = 25°C | | | 8 | pF |

NOTES

[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2185M outputs are CMOS-compatible and will drive to $V_{DDEXT}$ and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.

[8]0 V on $\overline{\text{BR}}$.

[9]Idle refers to ADSP-2185M state of operation during execution of IDLE instruction. Deasserted pins are driven to either $V_{DD}$ or GND.

[10]$I_{DD}$ measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (Types 1, 4, 5, 12, 13, 14), 30% are Type 2 and Type 6, and 20% are idle instructions.

[11]$V_{IN}$ = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[12]See Chapter 9 of the *ADSP-2100 Family User's Manual* for details.

[13]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS**[1]

| Parameter | Value Min | Value Max |
|---|---|---|
| Internal Supply Voltage ($V_{DDINT}$) | –0.3 V | +3.0 V |
| External Supply Voltage ($V_{DDEXT}$) | –0.3 V | +4.0 V |
| Input Voltage[2] | –0.5 V | +4.0 V |
| Output Voltage Swing[3] | –0.5 V | $V_{DDEXT}$ + 0.5 V |
| Operating Temperature Range | –40°C | +85°C |
| Storage Temperature Range | –65°C | +150°C |
| Lead Temperature (5 sec) LQFP | | 280°C |

NOTES
[1]Stresses greater than those listed may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Applies to Bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and Input only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).
[3]Applies to Output pins ($\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0, DT0, DT1, CLKOUT, FL2–0, $\overline{\text{BGH}}$).

**ESD SENSITIVITY**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-2185M features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


# TIMING SPECIFICATIONS

**GENERAL NOTES**

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

**TIMING NOTES**

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

**MEMORY TIMING SPECIFICATIONS**

The table below shows common memory device specifications and the corresponding ADSP-2185M timing parameters, for your convenience.

| Memory Device Specification | Parameter | Timing Parameter Definition[1] |
|---|---|---|
| Address Setup to Write Start | $t_{ASW}$ | A0–A13, $\overline{\text{xMS}}$ Setup before $\overline{\text{WR}}$ Low |
| Address Setup to Write End | $t_{AW}$ | A0–A13, $\overline{\text{xMS}}$ Setup before $\overline{\text{WR}}$ Deasserted |
| Address Hold Time | $t_{WRA}$ | A0–A13, $\overline{\text{xMS}}$ Hold before $\overline{\text{WR}}$ Low |
| Data Setup Time | $t_{DW}$ | Data Setup before $\overline{\text{WR}}$ High |
| Data Hold Time | $t_{DH}$ | Data Hold after $\overline{\text{WR}}$ High |
| OE to Data Valid | $t_{RDD}$ | $\overline{\text{RD}}$ Low to Data Valid |
| Address Access Time | $t_{AA}$ | A0–A13, $\overline{\text{xMS}}$ to Data Valid |

NOTE
[1]$\overline{\text{xMS}}$ = $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{CMS}}$ or $\overline{\text{IOMS}}$.

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Bus Request–Bus Grant** | | | | |
| *Timing Requirements:* | | | | |
| $t_{BH}$ | $\overline{BR}$ Hold after CLKOUT High[1] | $0.25t_{CK} + 2$ | | ns |
| $t_{BS}$ | $\overline{BR}$ Setup before CLKOUT Low[1] | $0.25t_{CK} + 10$ | | ns |
| *Switching Characteristics:* | | | | |
| $t_{SD}$ | CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable | | $0.25t_{CK} + 8$ | ns |
| $t_{SDB}$ | $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low | 0 | | ns |
| $t_{SE}$ | $\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable | 0 | | ns |
| $t_{SEC}$ | $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High | $0.25t_{CK} - 3$ | | ns |
| $t_{SDBH}$ | $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2] | 0 | | ns |
| $t_{SEH}$ | $\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2] | 0 | | ns |

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor or BDMA requires control of the bus to continue.

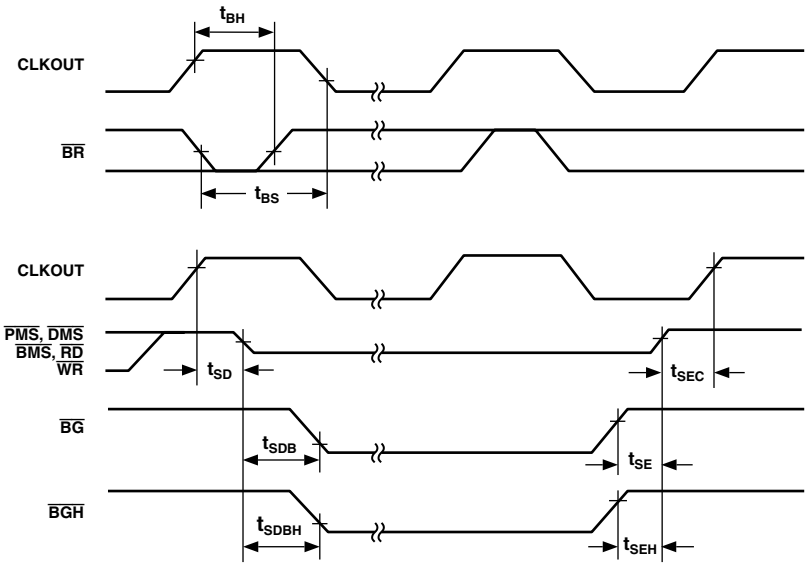



*Figure 23. Bus Request–Bus Grant*

**Serial Ports**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **Serial Ports** | | | | |
| *Timing Requirements:* | | | | |
| $t_{SCK}$ | SCLK Period | 26.6 | | ns |
| $t_{SCS}$ | DR/TFS/RFS Setup before SCLK Low | 4 | | ns |
| $t_{SCH}$ | DR/TFS/RFS Hold after SCLK Low | 7 | | ns |
| $t_{SCP}$ | SCLKIN Width | 12 | | ns |
| *Switching Characteristics*: | | | | |
| $t_{CC}$ | CLKOUT High to SCLKOUT | $0.25t_{CK}$ | $0.25t_{CK}$ + 6 | ns |
| $t_{SCDE}$ | SCLK High to DT Enable | 0 | | ns |
| $t_{SCDV}$ | SCLK High to DT Valid | | 12 | ns |
| $t_{RH}$ | $TFS/RFS_{OUT}$ Hold after SCLK High | 0 | | ns |
| $t_{RD}$ | $TFS/RFS_{OUT}$ Delay from SCLK High | | 12 | ns |
| $t_{SCDH}$ | DT Hold after SCLK High | 0 | | ns |
| $t_{TDE}$ | TFS (Alt) to DT Enable | 0 | | ns |
| $t_{TDV}$ | TFS (Alt) to DT Valid | | 12 | ns |
| $t_{SCDD}$ | SCLK High to DT Disable | | 12 | ns |
| $t_{RDV}$ | RFS (Multichannel, Frame Delay Zero) to DT Valid | | 12 | ns |

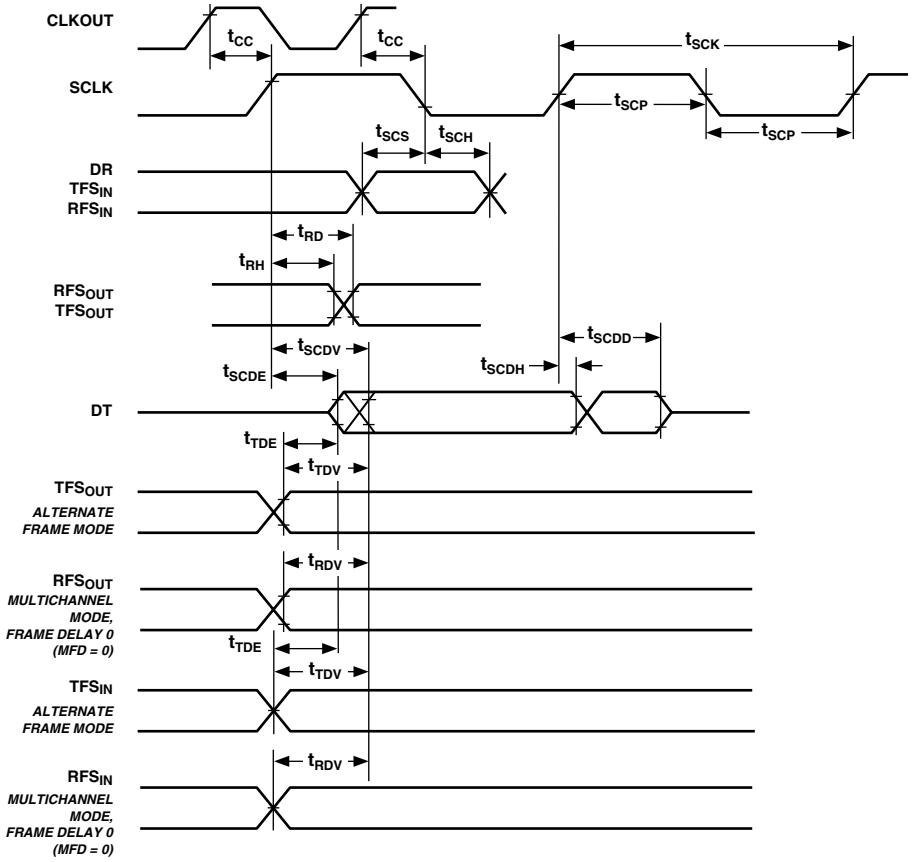



*Figure 26. Serial Ports*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **IDMA Write, Long Write Cycle** | | | | |
| *Timing Requirements:* | | | | |
| $t_{IKW}$ | $\overline{IACK}$ Low before Start of Write[1] | 0 | | ns |
| $t_{IKSU}$ | IAD15–0 Data Setup before End of Write[2, 3, 4] | $0.5t_{CK}$ + 5 | | ns |
| $t_{IKH}$ | IAD15–0 Data Hold after End of Write[2, 3, 4] | 0 | | ns |
| *Switching Characteristics*: | | | | |
| $t_{IKLW}$ | Start of Write to $\overline{IACK}$ Low[4] | $1.5t_{CK}$ | | ns |
| $t_{IKHW}$ | Start of Write to $\overline{IACK}$ High | | 10 | ns |

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]If Write Pulse ends before $\overline{IACK}$ Low, use specifications $t_{IDSU}$, $t_{IDH}$.
[3]If Write Pulse ends after $\overline{IACK}$ Low, use specifications $t_{IKSU}$, $t_{IKH}$.
[4]This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*.

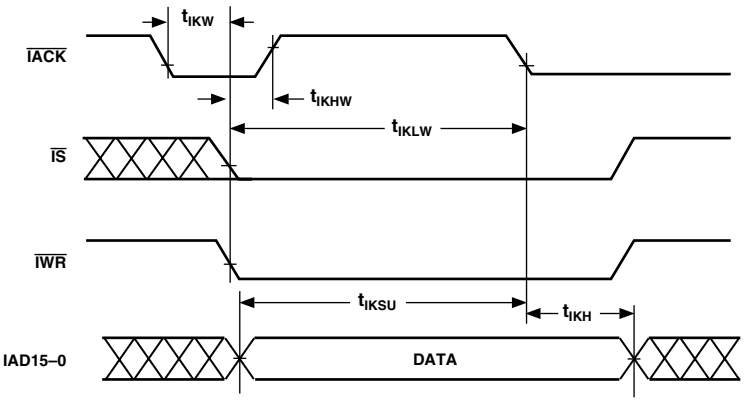



*Figure 29. IDMA Write, Long Write Cycle*

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| **IDMA Read, Short Read Cycle in Short Read Only Mode**[1] | | | | |
| *Timing Requirements:* | | | | |
| $t_{IKR}$ | $\overline{IACK}$ Low before Start of Read[2] | 0 | | ns |
| $t_{IRP}$ | Duration of Read[3] | 10 | | ns |
| *Switching Characteristics:* | | | | |
| $t_{IKHR}$ | $\overline{IACK}$ High after Start of Read[2] | | 10 | ns |
| $t_{IKDH}$ | IAD15–0 Previous Data Hold after End of Read[3] | 0 | | ns |
| $t_{IKDD}$ | IAD15–0 Previous Data Disabled after End of Read[3] | | 10 | ns |
| $t_{IRDE}$ | IAD15–0 Previous Data Enabled after Start of Read | 0 | | ns |
| $t_{IRDV}$ | IAD15–0 Previous Data Valid after Start of Read | | 10 | ns |

NOTES
[1]Short Read Only is enabled by setting Bit 14 of the IDMA Overlay Register to 1 (0x3FE7). Short Read Only can be enabled by the processor core writing to the register or by an external host writing to the register. Disabled by default.
[2]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low. Previous data remains until end of read.
[3]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

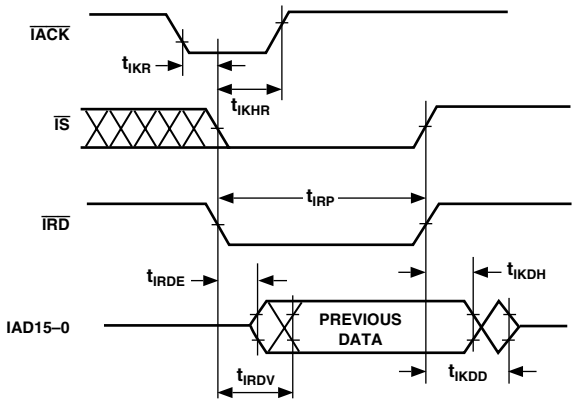
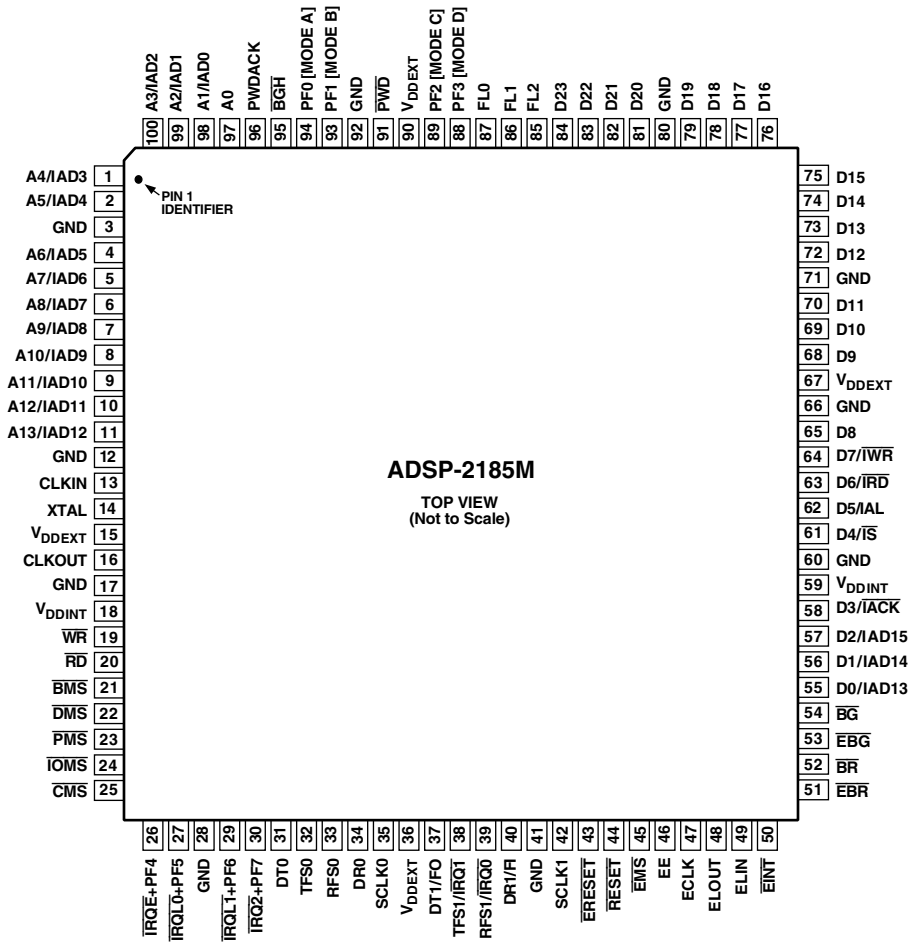



*Figure 32. IDMA Read, Short Read Only Cycle*

**100-LEAD LQFP PIN CONFIGURATION**



The Mini-BGA package pinout is shown in the table below. Pin names in bold text replace the plain text named functions when Mode C = 1. A + sign separates two functions when either function can be active for either major I/O mode. Signals enclosed in brackets [ ] are state bits latched from the value of the pin at the deassertion of $\overline{\text{RESET}}$.

The multiplexed pins DT1/FO, TFS1/$\overline{\text{IRQ1}}$, RFS1/$\overline{\text{IRQ0}}$, and DR1/FI, are mode selectable by setting Bit 10 (SPORT1 configure) of the System Control Register. If Bit 10 = 1, these pins have serial port functionality. If Bit 10 = 0, these pins are the external interrupt and flag pins. This bit is set to 1 by default upon reset.

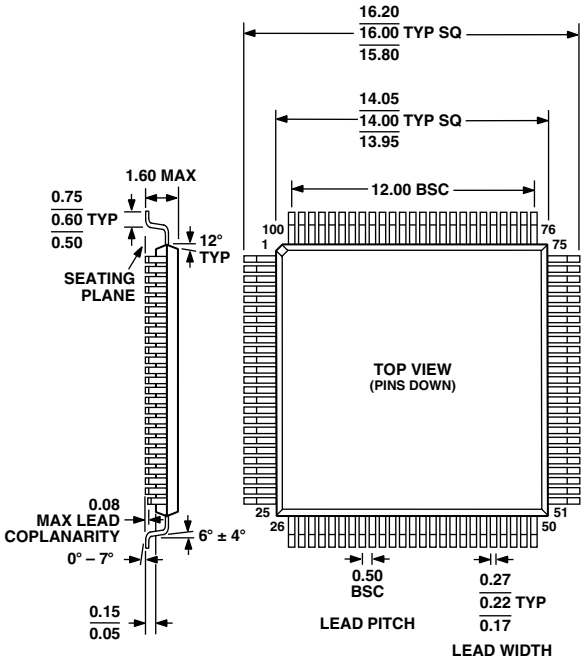
**Mini-BGA Package Pinout**

| Ball # | Pin Name | Ball # | Pin Name | Ball # | Pin Name | Ball # | Pin Name |
|---|---|---|---|---|---|---|---|
| A01 | A2/**IAD1** | D01 | NC | G01 | XTAL | K01 | NC |
| A02 | A1/**IAD0** | D02 | $\overline{\text{WR}}$ | G02 | NC | K02 | NC |
| A03 | GND | D03 | NC | G03 | GND | K03 | NC |
| A04 | A0 | D04 | $\overline{\text{BGH}}$ | G04 | A10/**IAD9** | K04 | $\overline{\text{BMS}}$ |
| A05 | NC | D05 | A9/**IAD8** | G05 | NC | K05 | $\overline{\text{DMS}}$ |
| A06 | GND | D06 | PF1 [MODE B] | G06 | NC | K06 | RFS0 |
| A07 | NC | D07 | PF2 [MODE C] | G07 | NC | K07 | TFS1/$\overline{\text{IRQ1}}$ |
| A08 | NC | D08 | NC | G08 | D6/**$\overline{\text{IRD}}$** | K08 | SCLK1 |
| A09 | NC | D09 | D13 | G09 | D5/**IAL** | K09 | $\overline{\text{ERESET}}$ |
| A10 | D22 | D10 | D12 | G10 | NC | K10 | $\overline{\text{EBR}}$ |
| A11 | GND | D11 | NC | G11 | NC | K11 | $\overline{\text{BR}}$ |
| A12 | GND | D12 | GND | G12 | D4/**$\overline{\text{IS}}$** | K12 | $\overline{\text{EBG}}$ |
| B01 | A4/**IAD3** | E01 | $V_{DDEXT}$ | H01 | CLKIN | L01 | $\overline{\text{IRQE}}$ + PF4 |
| B02 | A3/**IAD2** | E02 | $V_{DDEXT}$ | H02 | GND | L02 | NC |
| B03 | GND | E03 | A8/**IAD7** | H03 | GND | L03 | $\overline{\text{IRQL1}}$ + PF6 |
| B04 | NC | E04 | FL0 | H04 | GND | L04 | $\overline{\text{IOMS}}$ |
| B05 | NC | E05 | PF0 [MODE A] | H05 | $V_{DDINT}$ | L05 | GND |
| B06 | GND | E06 | FL2 | H06 | DT0 | L06 | $\overline{\text{PMS}}$ |
| B07 | $V_{DDEXT}$ | E07 | PF3 [MODE D] | H07 | TFS0 | L07 | DR0 |
| B08 | D23 | E08 | GND | H08 | D2/**IAD15** | L08 | GND |
| B09 | D20 | E09 | GND | H09 | D3/**$\overline{\text{IACK}}$** | L09 | $\overline{\text{RESET}}$ |
| B10 | D18 | E10 | $V_{DDEXT}$ | H10 | GND | L10 | ELIN |
| B11 | D17 | E11 | GND | H11 | NC | L11 | ELOUT |
| B12 | D16 | E12 | D10 | H12 | GND | L12 | $\overline{\text{EINT}}$ |
| C01 | PWDACK | F01 | A13/**IAD12** | J01 | CLKOUT | M01 | $\overline{\text{IRQL0}}$ + PF5 |
| C02 | A6/**IAD5** | F02 | NC | J02 | $V_{DDINT}$ | M02 | $\overline{\text{IRQL2}}$ + PF7 |
| C03 | $\overline{\text{RD}}$ | F03 | A12/**IAD11** | J03 | NC | M03 | NC |
| C04 | A5/**IAD4** | F04 | A11/**IAD10** | J04 | $V_{DDEXT}$ | M04 | $\overline{\text{CMS}}$ |
| C05 | A7/**IAD6** | F05 | FL1 | J05 | $V_{DDEXT}$ | M05 | GND |
| C06 | $\overline{\text{PWD}}$ | F06 | NC | J06 | SCLK0 | M06 | DT1/FO |
| C07 | $V_{DDEXT}$ | F07 | NC | J07 | D0/**IAD13** | M07 | DR1/FI |
| C08 | D21 | F08 | D7/**$\overline{\text{IWR}}$** | J08 | RFS1/$\overline{\text{IRQ0}}$ | M08 | GND |
| C09 | D19 | F09 | D11 | J09 | $\overline{\text{BG}}$ | M09 | NC |
| C10 | D15 | F10 | D8 | J10 | D1/**IAD14** | M10 | $\overline{\text{EMS}}$ |
| C11 | NC | F11 | NC | J11 | $V_{DDINT}$ | M11 | EE |
| C12 | D14 | F12 | D9 | J12 | $V_{DDINT}$ | M12 | ECLK |

## OUTLINE DIMENSIONS

Dimensions shown in millimeters.

### 100-Lead Metric Thin Plastic Quad Flatpack (LQFP) (ST-100)

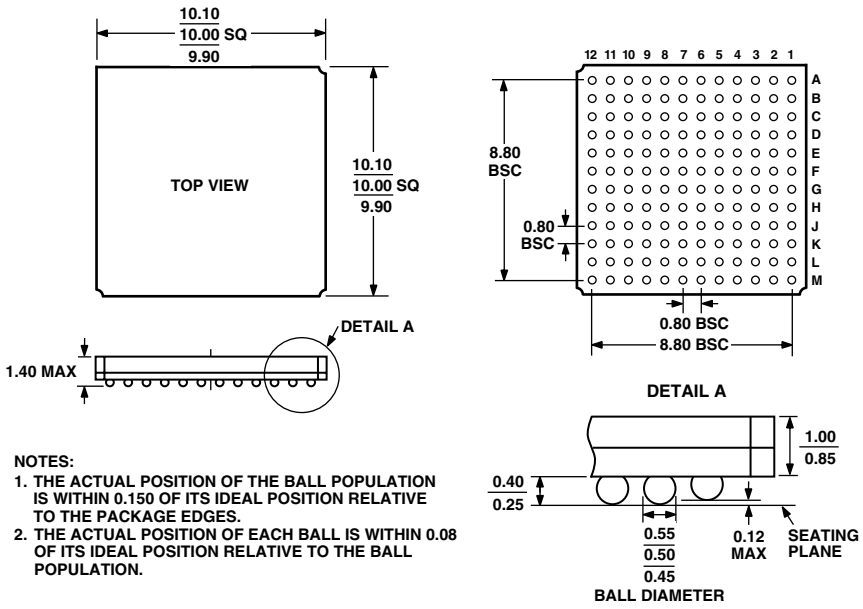



NOTE:
THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.08 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION.

## OUTLINE DIMENSIONS

Dimensions shown in millimeters.

### 144-Ball Mini-BGA
### (CA-144)




NOTES:
1. THE ACTUAL POSITION OF THE BALL POPULATION IS WITHIN 0.150 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.08 OF ITS IDEAL POSITION RELATIVE TO THE BALL POPULATION.

## ORDERING GUIDE

| Part Number | Ambient Temperature Range | Instruction Rate | Package Description* | Package Option |
|---|---|---|---|---|
| ADSP-2185MKST-300 | 0°C to 70°C | 75 | 100-Lead LQFP | ST-100 |
| ADSP-2185MBST-266 | –40°C to +85°C | 66 | 100-Lead LQFP | ST-100 |
| ADSP-2185MKCA-300 | 0°C to 70°C | 75 | 144-Ball Mini-BGA | CA-144 |
| ADSP-2185MBCA-266 | –40°C to +85°C | 66 | 144-Ball Mini-BGA | CA-144 |

*In 1998, JEDEC reevaluated the specifications for the TQFP package designation, assigning it to packages 1.0 mm thick. Previously labeled TQFP packages (1.6 mm thick) are now designated as LQFP.

C02047–3.5–10/00 (rev. 0)

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