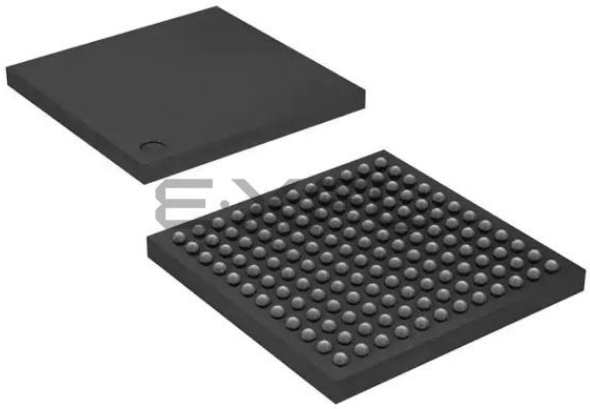

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	95
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 53x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk61fn1m0vmd15

- Communication interfaces
  - Ethernet controller with MII and RMII interface to external PHY and hardware IEEE 1588 capability
  - USB high-/full-/low-speed On-the-Go controller with ULPI interface
  - USB full-/low-speed On-the-Go controller with on-chip transceiver
  - USB Device Charger detect (USBDCD)
  - Two Controller Area Network (CAN) modules
  - Three SPI modules
  - Two I2C modules
  - Six UART modules
  - Secure Digital Host Controller (SDHC)
  - Two I2S modules

Table of Contents

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers: PK61 and MK61

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
K##	Kinetis family	• K61
A	Key attribute	• F = Cortex-M4 w/ DSP and FPU
M	Flash memory type	• N = Program flash only • X = Program flash and FlexMemory
FFF	Program flash memory size	• 512 = 512 KB • 1M0 = 1 MB

Table continues on the next page...

Field	Description	Values
T	Temperature range (°C)	• V = –40 to 105 • C = –40 to 85
PP	Package identifier	• MD = 144 MAPBGA (13 mm x 13 mm)
CC	Maximum CPU frequency (MHz)	• 15 = 150 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MK61FN1M0VMD15

3 Terminology and guidelines

3.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -9mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3mA	V_{DD} – 0.5	—		V	
	Output high voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6mA	 V_{DD} – 0.5 V_{DD} – 0.5	 — —	— — 	 V V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
I_{OHT_io60}	Output high current total for fast digital ports	—	—	100	mA	
V_{OH_Tamper}	Output high voltage — high drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -10mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -3mA	V_{BAT} – 0.5 V_{BAT} – 0.5	— —	— —	V V	
	Output high voltage — low drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OH} = -2mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OH} = -0.6mA	V_{BAT} – 0.5 V_{BAT} – 0.5	— —	— —	V V	
I_{OH_Tamper}	Output high current total for Tamper pins	—	—	100	mA	
V_{OL}	Output low voltage — high drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 10 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 5 mA	 — —	— — 	 0.5 0.5	 V V	
	Output low voltage — low drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 1 mA	 — —	— — 	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{OLT_io60}	Output low current total for fast digital ports	—	—	100	mA	
V_{OL_Tamper}	Output low voltage — high drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 10mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 3mA	— —	— —	0.5 0.5	V V	
	Output low voltage — low drive strength • 2.7 V ≤ V_{BAT} ≤ 3.6 V, I_{OL} = 2mA • 1.71 V ≤ V_{BAT} ≤ 2.7 V, I_{OL} = 0.6mA	— —	— —	0.5 0.5	V V	
I_{OL_Tamper}	Output low current total for Tamper pins	—	—	100	mA	

I_{INA}	Input leakage current, analog pins and digital pins configured as analog inputs
	• V_{SS} ≤ V_{IN} ≤ V_{DD}
	  • All pins except EXTAL32, XTAL32, EXTAL, XTAL
	  • EXTAL (PTA18) and XTAL (PTA19)
	  • EXTAL32, XTAL32
		
		—
		—
		—
			
			0.002
			0.004
			0.075
				
				0.5
				1.5
				10
					
					µA
					µA
					µA
						1, 2

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{IND}	Input leakage current, digital pins					2, 3
	• $V_{SS} \le V_{IN} \le V_{IL}$					
	• All digital pins	—	0.002	0.5	µA	
	• $V_{IN} = V_{DD}$					
	• All digital pins except PTD7	—	0.002	0.5	µA	
	• PTD7	—	0.004	1	µA	
I_{IND}	Input leakage current, digital pins					2, 3, 4
	• $V_{IL} < V_{IN} < V_{DD}$					
	• V_{DD} = 3.6 V	—	18	26	µA	
	• V_{DD} = 3.0 V	—	12	19	µA	
	• V_{DD} = 2.5 V	—	8	13	µA	
	• V_{DD} = 1.7 V	—	3	6	µA	
I_{IND}	Input leakage current, digital pins					2, 3
	• $V_{DD} < V_{IN} < 5.5$ V	—	1	50	µA	
Z_{IND}	Input impedance examples, digital pins					2, 5
	• V_{DD} = 3.6 V	—	—	48	kΩ	
	• V_{DD} = 3.0 V	—	—	55	kΩ	
	• V_{DD} = 2.5 V	—	—	57	kΩ	
	• V_{DD} = 1.7 V	—	—	85	kΩ	
I_{IN_Tamper}	Input leakage current (per Tamper pin) for full temperature range	—	—	1	µA	
I_{IN_Tamper}	Input leakage current (per Tamper pin) at 25°C	—	—	0.025	µA	
R_{PU}	Internal pullup resistors (except Tamper pins)	20	—	50	kΩ	6
R_{PD}	Internal pulldown resistors (except Tamper pins)	20	—	50	kΩ	7

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
2. Digital pins have an associated GPIO port function and have 5V tolerant inputs, except EXTAL and XTAL.
3. Internal pull-up/pull-down resistors disabled.
4. Characterized, not tested in production.
5. Examples calculated using V_{IL} relation, V_{DD}, and max I_{IND}: $Z_{IND}=V_{IL}/I_{IND}$. This is the impedance needed to pull a high signal to a level below V_{IL} due to leakage when $V_{IL} < V_{IN} < V_{DD}$. These examples assume signal source low = 0 V. See Figure 2.
6. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}
7. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{DD}

Table 10. General switching specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
t_{io50}	Port rise and fall time (high drive strength)				6
	• Slew disabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	7	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	3	ns	—
	• Slew enabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	28	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	14	ns	—
t_{io50}	Port rise and fall time (low drive strength)				7
	• Slew disabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	18	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	9	ns	—
	• Slew enabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	48	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	24	ns	—
t_{io60}	Port rise and fall time (high drive strength)				6
	• Slew disabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	6	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	3	ns	—
	• Slew enabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	28	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	14	ns	—
t_{io60}	Port rise and fall time (low drive strength)				7
	• Slew disabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	18	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	6	ns	—
	• Slew enabled				
	• 1.71 ≤ V_{DD} ≤ 2.7V	—	48	ns	—
	• 2.7 ≤ V_{DD} ≤ 3.6V	—	24	ns	—

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75 pF load
5. 15 pF load
6. 25 pF load
7. 15 pF load

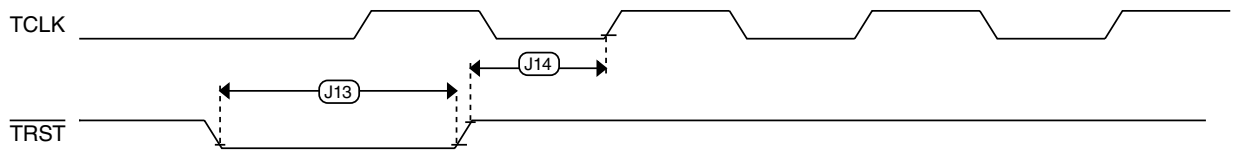


Figure 10. $\overline{\text{TRST}}$ timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only	—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 4.5	—	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00	(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	(16/5) x f_{ints_t}	—	—	kHz	
FLL						
f_{fll_ref}	FLL reference frequency range	31.25	—	39.0625	kHz	

Table continues on the next page...

Table 15. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
PLL0,1							
f_{pll_ref}	PLL reference frequency range		8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency		180	—	360	MHz	
f_{vcoclk}	PLL output frequency		90	—	180	MHz	
f_{vcoclk_90}	PLL quadrature output frequency		90	—	180	MHz	
I_{pll}	PLL0 operating current • VCO @ 184 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 23)		—	2.8	—	mA	
I_{pll}	PLL0 operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	4.7	—	mA	7
I_{pll}	PLL1 operating current • VCO @ 184 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 23)		—	2.3	—	mA	7
I_{pll}	PLL1 operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	3.6	—	mA	7
t_{pll_lock}	Lock detector detection time		—	—	100×10^{-6} + 1075(1/f_{pll_ref})	s	8
J_{cyc_pll}	PLL period jitter (RMS)						9

Table continues on the next page...

6.3.2.2 Oscillator frequency specifications

Table 17. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	1
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	60	MHz	2, 3
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	1000	—	ms	4, 5
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	500	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Frequencies less than 8 MHz are not in the PLL range.
2. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
3. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz oscillator electrical characteristics

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

Table 23. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	70 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	630 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	2.5 M	6.4 M	—	writes	
$n_{nvmwree2k}$	• EEPROM backup to FlexRAM ratio = 2,048	10 M	25 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup per subsystem. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the FTFE to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write\_efficiency} \times n_{nvmcycee}$$

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$$T_{NFC} = T_L + T_H = \frac{T_{input\ clock}}{SCALER}$$

The SCALER value is derived from the fractional divider specified in the SIM's CLKDIV4 register:

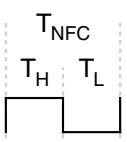
$$SCALER = \frac{SIM\_CLKDIV4[NFCFRAC] + 1}{SIM\_CLKDIV4[NFCDIV] + 1}$$

In case the reciprocal of SCALER is an integer, the duty cycle of NFC clock is 50%, means $T_H = T_L$. In case the reciprocal of SCALER is not an integer:

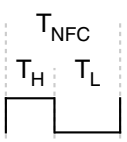
$$T_L = (1 + SCALER / 2) \times \frac{T_{NFC}}{2}$$

$$T_H = (1 - SCALER / 2) \times \frac{T_{NFC}}{2}$$

For example, if SCALER is 0.2, then $T_H = T_L = T_{NFC}/2$.



However, if SCALER is 0.667, then $T_L = 2/3 \times T_{NFC}$ and $T_H = 1/3 \times T_{NFC}$.



NOTE

The reciprocal of SCALER must be a multiple of 0.5. For example, 1, 1.5, 2, 2.5, etc.

Table 25. NFC specifications

Num	Description	Min.	Max.	Unit
t_{CLS}	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
t_{CLH}	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
t_{CS}	$\overline{\text{NFC\_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
t_{CH}	$\overline{\text{NFC\_CEn}}$ hold time	$T_H + T_L$	—	ns

Table continues on the next page...

Table 25. NFC specifications (continued)

Num	Description	Min.	Max.	Unit
t_{WP}	$\overline{\text{NFC\_WP}}$ pulse width	$T_L - 1$	—	ns
t_{ALS}	NFC_ALE setup time	$2T_H + T_L$	—	ns
t_{ALH}	NFC_ALE hold time	$T_H + T_L$	—	ns
t_{DS}	Data setup time	$T_L - 1$	—	ns
t_{DH}	Data hold time	$T_H - 1$	—	ns
t_{WC}	Write cycle time	$T_H + T_L - 1$	—	ns
t_{WH}	$\overline{\text{NFC\_WE}}$ hold time	$T_H - 1$	—	ns
t_{RR}	Ready to $\overline{\text{NFC\_RE}}$ low	$4T_H + 3T_L + 90$	—	ns
t_{RP}	$\overline{\text{NFC\_RE}}$ pulse width	$T_L + 1$	—	ns
t_{RC}	Read cycle time	$T_L + T_H - 1$	—	ns
t_{REH}	$\overline{\text{NFC\_RE}}$ high hold time	$T_H - 1$	—	ns
t_{IS}	Data input setup time	11	—	ns

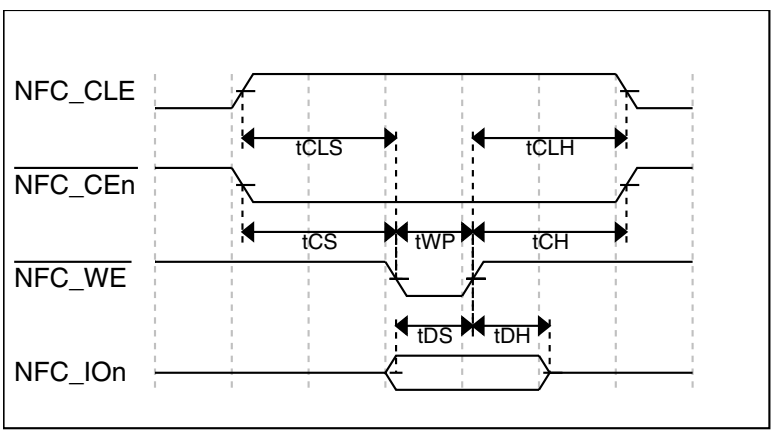


Figure 13. Command latch cycle timing

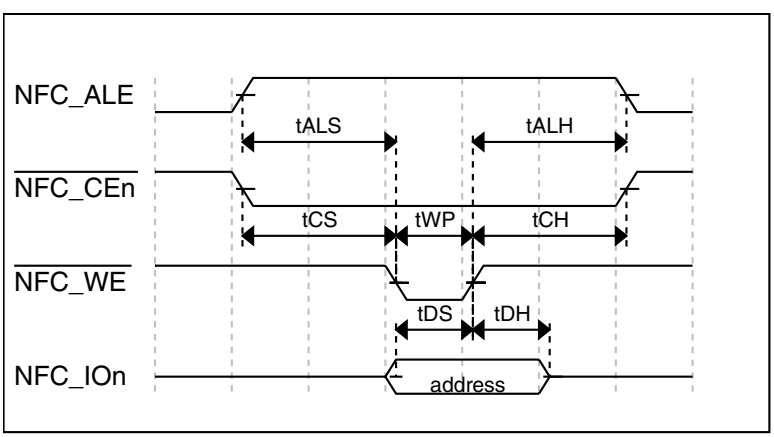


Figure 14. Address latch cycle timing

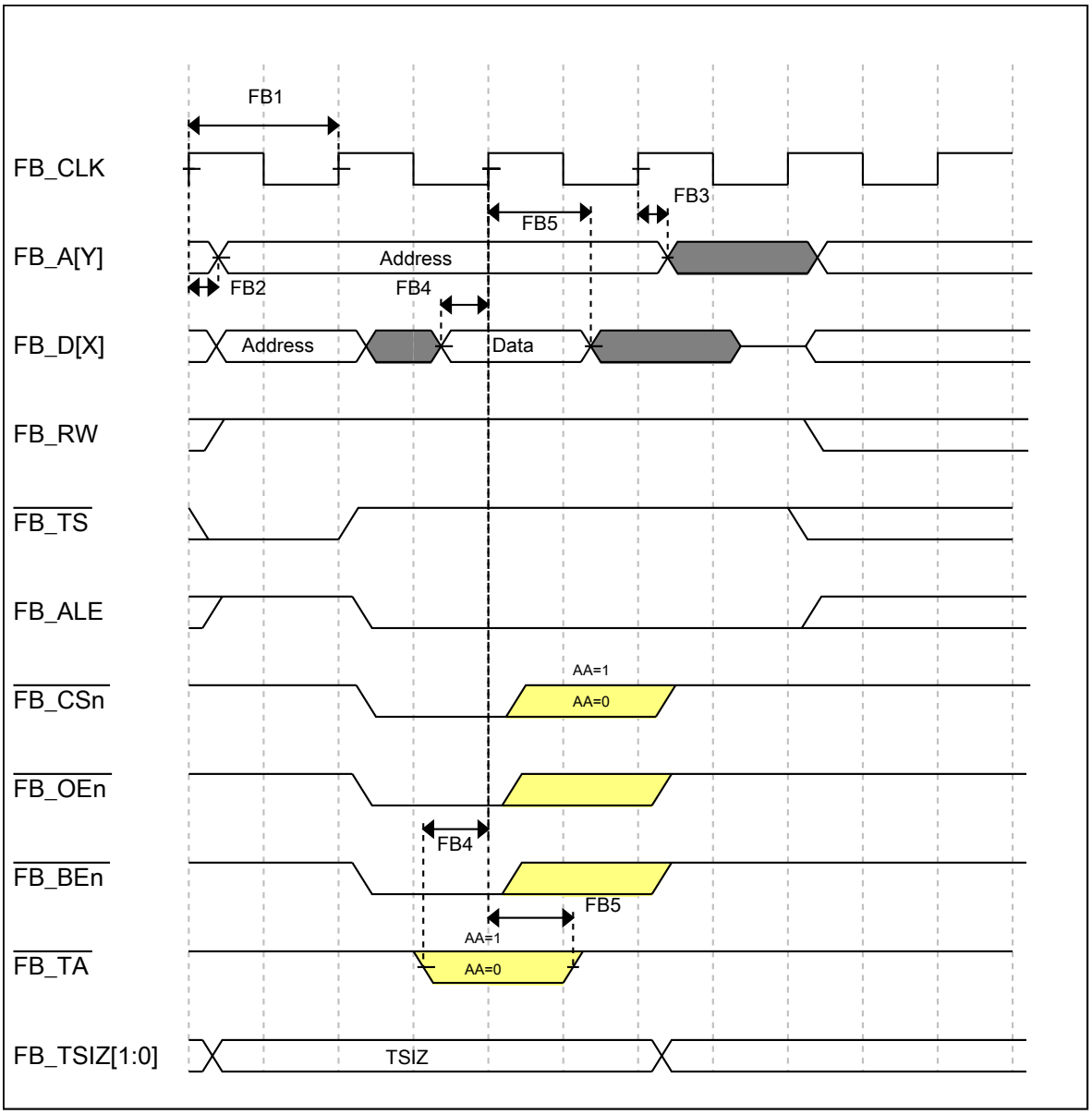


Figure 18. FlexBus read timing diagram

Table 30. 16-bit ADC with PGA operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
		No ADC hardware averaging Continuous conversions enabled Peripheral clock = 50 MHz					

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. ADC must be configured to use the internal voltage reference (VREF_OUT)
3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
4. For single ended configurations the input impedance of the driven input is $R_{PGAD}/2$
5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for F_{in}=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics

Table 31. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
I_{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	µA	2
I_{DC_PGA}	Input DC current		$\frac{2}{R_{PGAD}}\left(\frac{(V_{REFPGA}\times 0.583)-V_{CM}}{(Gain+1)}\right)$			A	3
		Gain =1, V_{REFPGA}=1.2V, V_{CM}=0.5V	—	1.54	—	µA	
		Gain =64, V_{REFPGA}=1.2V, V_{CM}=0.1V	—	0.57	—	µA	
G	Gain[4]	• PGAG=0 • PGAG=1 • PGAG=2 • PGAG=3 • PGAG=4 • PGAG=5 • PGAG=6	0.95 1.9 3.8 7.6 15.2 30.0 58.8	1 2 4 8 16 31.6 63.3	1.05 2.1 4.2 8.4 16.6 33.2 67.8		R_{AS} < 100Ω
BW	Input signal bandwidth	• 16-bit modes • < 16-bit modes	— —	— —	4 40	kHz kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V_{DDA}= 3V ±100mV,

Table continues on the next page...

6.6.3.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/μs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

6.8.5 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin.

Table 43. ULPI timing specifications

Num	Description	Min.	Typ.	Max.	Unit
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input setup (control and data)	5	—	—	ns
U3	Input hold (control and data)	1	—	—	ns
U4	Output valid (control and data)	—	—	9.5	ns
U5	Output hold (control and data)	1	—	—	ns

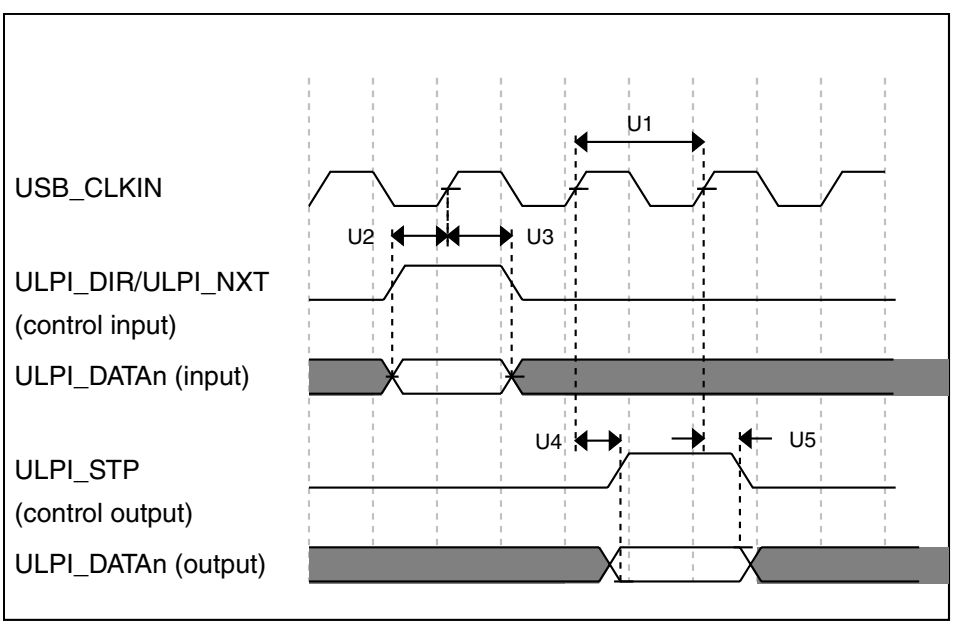


Figure 29. ULPI timing diagram

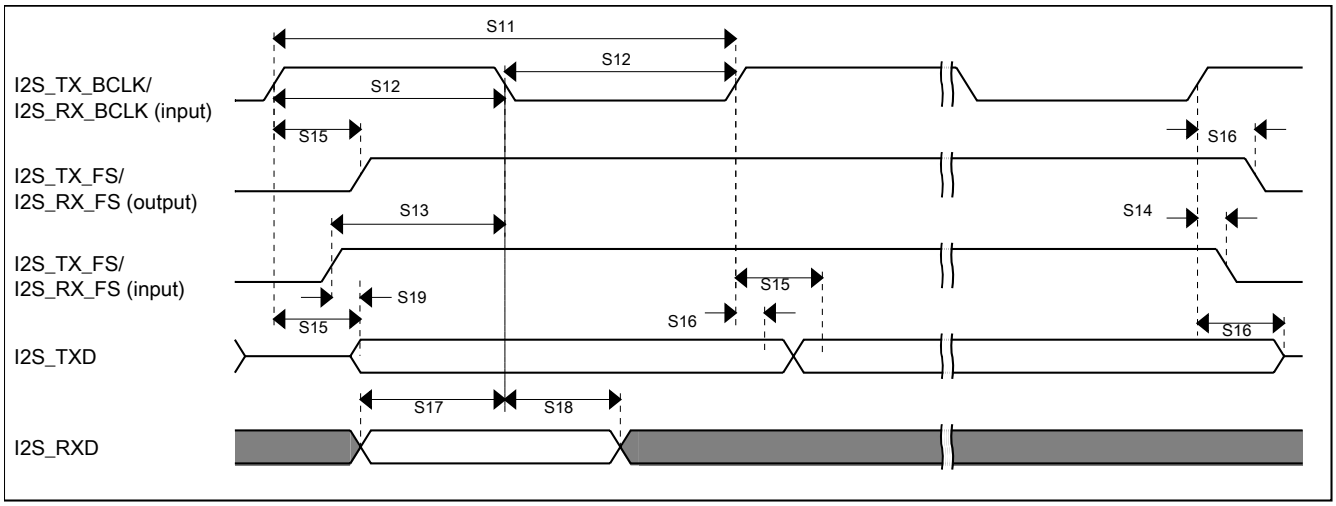


Figure 39. I2S/SAI timing — slave modes

6.8.12.3 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 55. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	-1.6	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

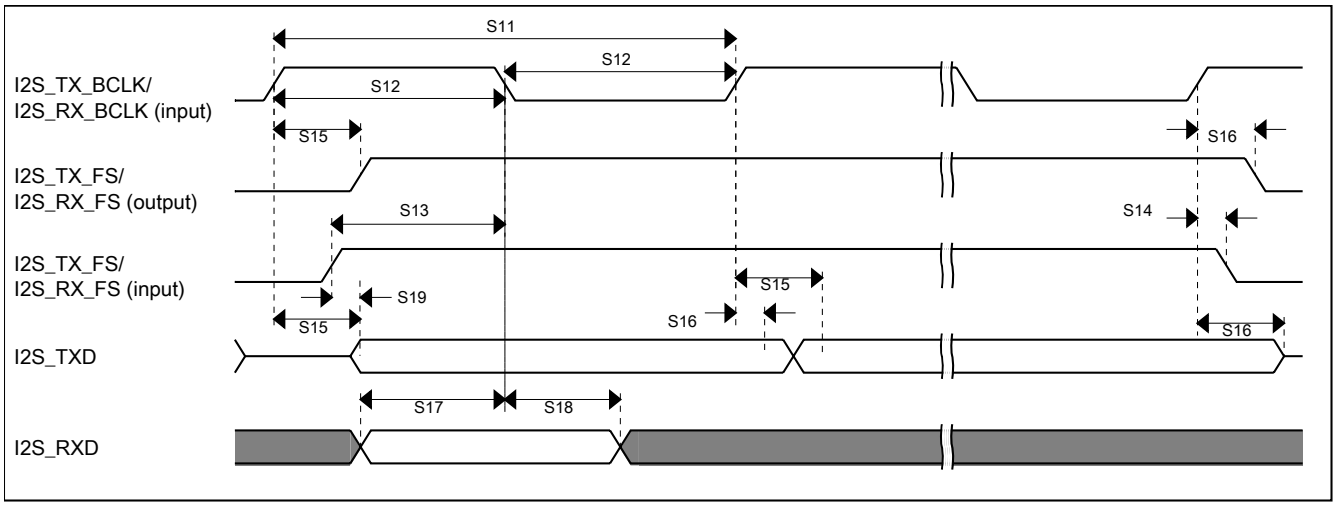


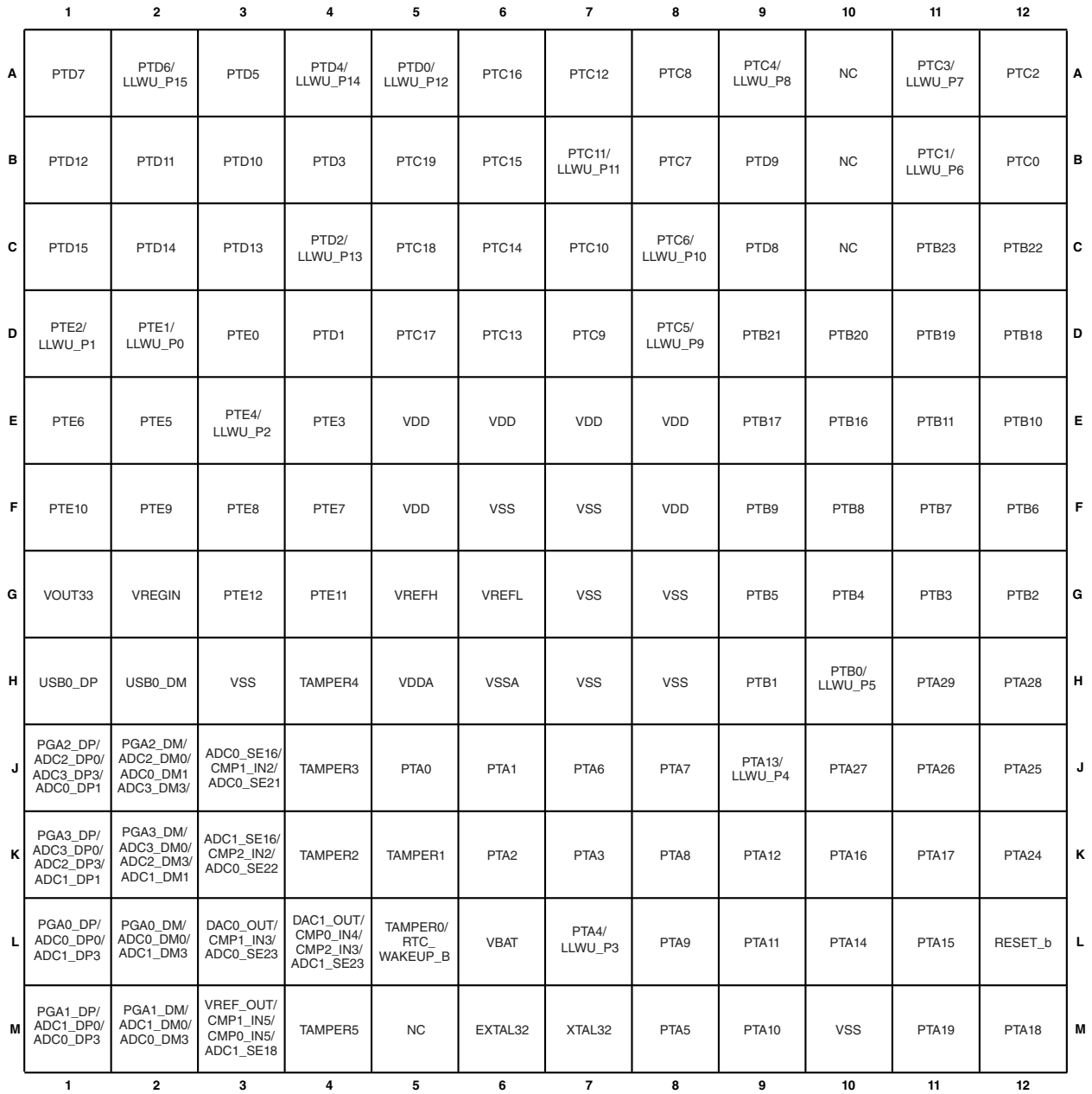
Figure 41. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 57. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f_{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C_{REF}	Internal reference capacitor	—	1	—	pF	
V_{DELTA}	Oscillator delta voltage	—	600	—	mV	2, 5
I_{REF}	Reference oscillator current source base current • 2 µA setting (REFCHRG = 0) • 32 µA setting (REFCHRG = 15)	— —	2 36	3 50	µA	2, 6
I_{ELE}	Electrode oscillator current source base current • 2 µA setting (EXTCHRG = 0) • 32 µA setting (EXTCHRG = 15)	— —	2 36	3 50	µA	2, 7
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	—	fF/count	11
Res	Resolution	—	—	16	bits	
T_{Con20}	Response time @ 20 pF	8	15	25	µs	12
I_{TSI_RUN}	Current added in run mode	—	55	—	µA	
I_{TSI_LP}	Low power mode current adder	—	1.3	2.5	µA	13



	1	2	3	4	5	6	7	8	9	10	11	12	
A	PTD7	PTD6/ LLWU_P15	PTD5	PTD4/ LLWU_P14	PTD0/ LLWU_P12	PTC16	PTC12	PTC8	PTC4/ LLWU_P8	NC	PTC3/ LLWU_P7	PTC2	A
B	PTD12	PTD11	PTD10	PTD3	PTC19	PTC15	PTC11/ LLWU_P11	PTC7	PTD9	NC	PTC1/ LLWU_P6	PTC0	B
C	PTD15	PTD14	PTD13	PTD2/ LLWU_P13	PTC18	PTC14	PTC10	PTC6/ LLWU_P10	PTD8	NC	PTB23	PTB22	C
D	PTE2/ LLWU_P1	PTE1/ LLWU_P0	PTE0	PTD1	PTC17	PTC13	PTC9	PTC5/ LLWU_P9	PTB21	PTB20	PTB19	PTB18	D
E	PTE6	PTE5	PTE4/ LLWU_P2	PTE3	VDD	VDD	VDD	VDD	PTB17	PTB16	PTB11	PTB10	E
F	PTE10	PTE9	PTE8	PTE7	VDD	VSS	VSS	VDD	PTB9	PTB8	PTB7	PTB6	F
G	VOUT33	VREGIN	PTE12	PTE11	VREFH	VREFL	VSS	VSS	PTB5	PTB4	PTB3	PTB2	G
H	USB0_DP	USB0_DM	VSS	TAMPER4	VDDA	VSSA	VSS	VSS	PTB1	PTB0/ LLWU_P5	PTA29	PTA28	H
J	PGA2_DP/ ADC2_DP0/ ADC3_DP3/ ADC0_DP1	PGA2_DM/ ADC2_DM0/ ADC0_DM1 ADC3_DM3/	ADC0_SE16/ CMP1_IN2/ ADC0_SE21	TAMPER3	PTA0	PTA1	PTA6	PTA7	PTA13/ LLWU_P4	PTA27	PTA26	PTA25	J
K	PGA3_DP/ ADC3_DP0/ ADC2_DP3/ ADC1_DP1	PGA3_DM/ ADC3_DM0/ ADC2_DM3/ ADC1_DM1	ADC1_SE16/ CMP2_IN2/ ADC0_SE22	TAMPER2	TAMPER1	PTA2	PTA3	PTA8	PTA12	PTA16	PTA17	PTA24	K
L	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23	TAMPER0/ RTC_ WAKEUP_B	VBAT	PTA4/ LLWU_P3	PTA9	PTA11	PTA14	PTA15	RESET_b	L
M	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	TAMPER5	NC	EXTAL32	XTAL32	PTA5	PTA10	VSS	PTA19	PTA18	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 42. K61 144 MAPBGA Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Table 59. Revision History

Rev. No.	Date	Substantial Changes
3	3/2012	Initial public release

Table continues on the next page...