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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

| | |
|-------------------------|---|
| Product Status | Discontinued at Digi-Key |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 160K Logic Elements |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 672-BBGA, FCBGA |
| Supplier Device Package | 672-FBGA, FC (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10as016e3f27e1sg |



Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices

| Market | Applications |
|-----------------------|---|
| Wireless | <ul style="list-style-type: none"> • Channel and switch cards in remote radio heads • Mobile backhaul |
| Wireline | <ul style="list-style-type: none"> • 40G/100G muxponders and transponders • 100G line cards • Bridging • Aggregation |
| Broadcast | <ul style="list-style-type: none"> • Studio switches • Servers and transport • Videoconferencing • Professional audio and video |
| Computing and Storage | <ul style="list-style-type: none"> • Flash cache • Cloud computing servers • Server acceleration |
| Medical | <ul style="list-style-type: none"> • Diagnostic scanners • Diagnostic imaging |
| Military | <ul style="list-style-type: none"> • Missile guidance and control • Radar • Electronic warfare • Secure communications |

Related Information

Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



Key Advantages of Intel Arria 10 Devices

Table 2. Key Advantages of the Intel Arria 10 Device Family

| Advantage | Supporting Feature |
|--|---|
| Enhanced core architecture | <ul style="list-style-type: none">Built on TSMC's 20 nm process technology60% higher performance than the previous generation of mid-range FPGAs15% higher performance than the fastest previous-generation FPGA |
| High-bandwidth integrated transceivers | <ul style="list-style-type: none">Short-reach rates up to 25.8 Gigabits per second (Gbps)Backplane capability up to 12.5 GbpsIntegrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC) |
| Improved logic integration and hard IP blocks | <ul style="list-style-type: none">8-input adaptive logic module (ALM)Up to 65.6 megabits (Mb) of embedded memoryVariable-precision digital signal processing (DSP) blocksFractional synthesis phase-locked loops (PLLs)Hard PCI Express Gen3 IP blocksHard memory controllers and PHY up to 2,400 Megabits per second (Mbps) |
| Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor | <ul style="list-style-type: none">Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric |
| Advanced power savings | <ul style="list-style-type: none">Comprehensive set of advanced power saving featuresPower-optimized MultiTrack routing and core architectureUp to 40% lower power compared to previous generation of mid-range FPGAsUp to 60% lower power compared to previous generation of high-end FPGAs |

Summary of Intel Arria 10 Features

Table 3. Summary of Features for Intel Arria 10 Devices

| Feature | Description |
|------------------------------|---|
| Technology | <ul style="list-style-type: none">TSMC's 20-nm SoC process technologyAllows operation at a lower V_{CC} level of 0.82 V instead of the 0.9 V standard V_{CC} core voltage |
| Packaging | <ul style="list-style-type: none">1.0 mm ball-pitch FINELINE BGA packaging0.8 mm ball-pitch Ultra FINELINE BGA packagingMultiple devices with identical package footprints for seamless migration between different FPGA densitiesDevices with compatible package footprints allow migration to next generation high-end Stratix® 10 devicesRoHS, leaded⁽¹⁾, and lead-free (Pb-free) options |
| High-performance FPGA fabric | <ul style="list-style-type: none">Enhanced 8-input ALM with four registersImproved multi-track routing architecture to reduce congestion and improve compilation timeHierarchical core clocking architectureFine-grained partial reconfiguration |
| Internal memory blocks | <ul style="list-style-type: none">M20K—20-Kb memory blocks with hard error correction code (ECC)Memory logic array block (MLAB)—640-bit memory |
| continued... | |

(1) Contact Intel for availability.



| Feature | Description | |
|-----------------------------------|--|---|
| Embedded Hard IP blocks | Variable-precision DSP | <ul style="list-style-type: none">Native support for signal processing precision levels from 18 x 19 to 54 x 54Native support for 27 x 27 multiplier mode64-bit accumulator and cascade for systolic finite impulse responses (FIRs)Internal coefficient memory banksPadder/subtractor for improved efficiencyAdditional pipeline register to increase performance and reduce powerSupports floating point arithmetic:<ul style="list-style-type: none">Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.Dynamic accumulator reset control.Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks. |
| | Memory controller | DDR4, DDR3, and DDR3L |
| | PCI Express* | PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port |
| | Transceiver I/O | <ul style="list-style-type: none">10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)PCS hard IPs that support:<ul style="list-style-type: none">10-Gbps Ethernet (10GbE)PCIe PIPE interfaceInterlakenGbps Ethernet (GbE)Common Public Radio Interface (CPRI) with deterministic latency supportGigabit-capable passive optical network (GPON) with fast lock-time support13.5G JESD204b8B/10B, 64B/66B, 64B/67B encoders and decodersCustom mode support for proprietary protocols |
| Core clock networks | <ul style="list-style-type: none">Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none">667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface800 MHz LVDS interface clocking with 1,600 Mbps LVDS interfaceGlobal, regional, and peripheral clock networksClock networks that are not used can be gated to reduce dynamic power | |
| Phase-locked loops (PLLs) | <ul style="list-style-type: none">High-resolution fractional synthesis PLLs:<ul style="list-style-type: none">Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)Support integer mode and fractional modeFractional mode support with third-order delta-sigma modulationInteger PLLs:<ul style="list-style-type: none">Adjacent to general purpose I/OsSupport external memory and LVDS interfaces | |
| FPGA General-purpose I/Os (GPIOs) | <ul style="list-style-type: none">1.6 Gbps LVDS—every pair can be configured as receiver or transmitterOn-chip termination (OCT)1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing | |
| External Memory Interface | <ul style="list-style-type: none">Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none">DDR4—speeds up to 1,200 MHz/2,400 MbpsDDR3—speeds up to 1,067 MHz/2,133 MbpsSoft memory controller—provides support for RLDRAM 3⁽²⁾, QDR IV⁽²⁾, and QDR II+ | |
| continued... | | |



| Feature | Description |
|--------------------|---|
| | <ul style="list-style-type: none">Dynamic reconfiguration of the transceivers and PLLsFine-grained partial reconfiguration of the core fabricActive Serial x4 Interface |
| Power management | <ul style="list-style-type: none">SmartVIDLow static power device optionsProgrammable Power TechnologyIntel Quartus Prime integrated power analysis |
| Software and tools | <ul style="list-style-type: none">Intel Quartus Prime design suiteTransceiver toolkitPlatform Designer system integration toolDSP Builder for Intel FPGAsOpenCL™ supportIntel SoC FPGA Embedded Design Suite (EDS) |

Related Information

[Intel Arria 10 Transceiver PHY Overview](#)

Provides details on Intel Arria 10 transceivers.

Intel Arria 10 Device Variants and Packages

Table 4. Device Variants for the Intel Arria 10 Device Family

| Variant | Description |
|-------------------|---|
| Intel Arria 10 GX | FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |
| Intel Arria 10 GT | FPGA featuring: <ul style="list-style-type: none">17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules. |
| Intel Arria 10 SX | SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |

Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



Maximum Resources

Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

| Resource | | Product Line | | | | |
|------------------------------|----------------------|--------------|---------|---------|---------|---------|
| | | GX 160 | GX 220 | GX 270 | GX 320 | GX 480 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 |
| | I/O | 6 | 6 | 8 | 8 | 12 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 |
| GPIO ⁽³⁾ | | 288 | 288 | 384 | 384 | 492 |
| LVDS Pair ⁽⁴⁾ | | 120 | 120 | 168 | 168 | 222 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 |

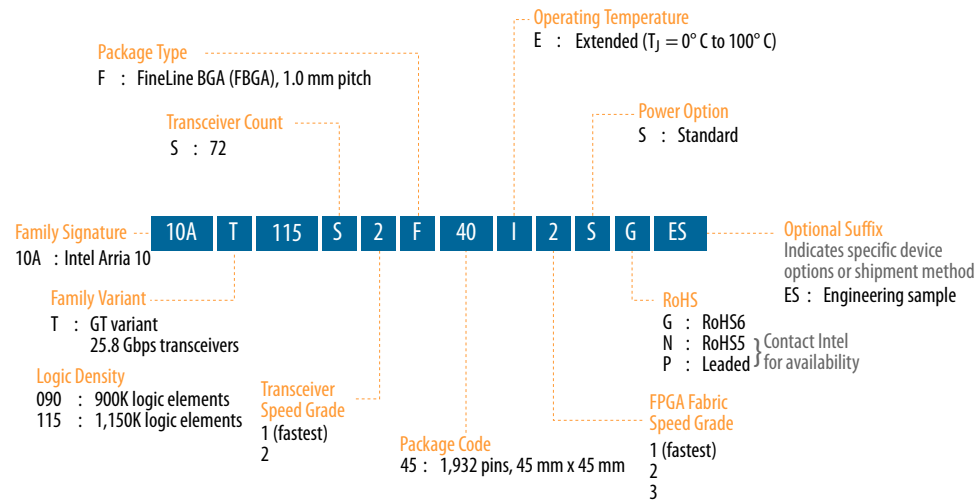
⁽³⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁴⁾ Each LVDS I/O pair can be used as differential input or output.



Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





Maximum Resources

Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices

| Resource | | Product Line | |
|------------------------------|----------------------|-------------------|-------------------|
| | | GT 900 | GT 1150 |
| Logic Elements (LE) (K) | | 900 | 1,150 |
| ALM | | 339,620 | 427,200 |
| Register | | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 48,460 | 54,260 |
| | MLAB | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 32 | 32 |
| | I/O | 16 | 16 |
| Transceiver | 17.4 Gbps | 72 ⁽⁵⁾ | 72 ⁽⁵⁾ |
| | 25.8 Gbps | 6 | 6 |
| GPIO ⁽⁶⁾ | | 624 | 624 |
| LVDS Pair ⁽⁷⁾ | | 312 | 312 |
| PCIe Hard IP Block | | 4 | 4 |
| Hard Memory Controller | | 16 | 16 |

Related Information

Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

Package Plan

Table 11. Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | SF45 (45 mm x 45 mm, 1932-pin FBGA) | | |
|--------------|--|----------|------|
| | 3 V I/O | LVDS I/O | XCVR |
| GT 900 | — | 624 | 72 |
| GT 1150 | — | 624 | 72 |

⁽⁵⁾ If all 6 GT channels are in use, 12 of the GX channels are not usable.

⁽⁶⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁷⁾ Each LVDS I/O pair can be used as differential input or output.



Maximum Resources

Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices

| Resource | | Product Line | | | | | | |
|--------------------------------|----------------------|--------------|---------|---------|---------|---------|---------|-----------|
| | | SX 160 | SX 220 | SX 270 | SX 320 | SX 480 | SX 570 | SX 660 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 | 570 | 660 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 | 217,080 | 251,680 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 | 868,320 | 1,006,720 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 | 36,000 | 42,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 | 5,096 | 5,788 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 | 1,523 | 1,687 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 | 3,046 | 3,374 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| | I/O | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 | 48 | 48 |
| GPIO ⁽⁸⁾ | | 288 | 288 | 384 | 384 | 492 | 696 | 696 |
| LVDS Pair ⁽⁹⁾ | | 120 | 120 | 168 | 168 | 174 | 324 | 324 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| ARM Cortex-A9 MPCore Processor | | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

Package Plan

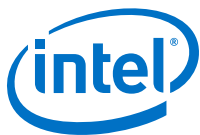
Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | | F34 (35 mm × 35 mm, 1152-pin FBGA) | | |
|--------------|--|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 160 | 48 | 144 | 6 | 48 | 192 | 12 | 48 | 240 | 12 | — | — | — |
| SX 220 | 48 | 144 | 6 | 48 | 192 | 12 | 48 | 240 | 12 | — | — | — |
| SX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 | 48 | 336 | 24 |
| SX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 | 48 | 336 | 24 |
| continued... | | | | | | | | | | | | |

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ Each LVDS I/O pair can be used as differential input or output.



| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | | F34 (35 mm × 35 mm, 1152-pin FBGA) | | |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 480 | — | — | — | — | — | — | 48 | 312 | 12 | 48 | 444 | 24 |
| SX 570 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |
| SX 660 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |

Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|--------------|--|----------|------|---|----------|------|---|----------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 270 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 320 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 480 | 48 | 348 | 36 | — | — | — | — | — | — |
| SX 570 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| SX 660 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |

Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.



I/O Vertical Migration for Intel Arria 10 Devices

Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.

| Variant | Product Line | Package | | | | | | | | | | |
|---------------------|--------------|---------|-----|-----|-----|-----|------|------|------|------|------|------|
| | | U19 | F27 | F29 | F34 | F35 | KF40 | NF40 | RF40 | NF45 | SF45 | UF45 |
| Intel® Arria® 10 GX | GX 160 | ↑ | ↑ | ↑ | | | | | | | | |
| | GX 220 | ↓ | ↓ | ↓ | | | | | | | | |
| | GX 270 | | ↓ | ↓ | ↑ | ↑ | | | | | | |
| | GX 320 | | ↓ | ↓ | ↑ | ↑ | | | | | | |
| | GX 480 | | | ↓ | ↑ | ↑ | | | | | | |
| | GX 570 | | | | ↑ | ↑ | ↑ | ↑ | | | | |
| | GX 660 | | | | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ |
| | GX 900 | | | | ↑ | | | ↑ | ↑ | ↑ | ↑ | ↑ |
| | GX 1150 | | | | ↑ | | | ↑ | ↑ | ↑ | ↑ | ↑ |
| | GT 900 | | | | | | | | | | ↑ | ↑ |
| | GT 1150 | | | | | | | | | | ↓ | ↓ |
| Intel Arria 10 SX | SX 160 | ↑ | ↑ | ↑ | | | | | | | | |
| | SX 220 | ↓ | ↓ | ↓ | | | | | | | | |
| | SX 270 | | ↓ | ↓ | ↑ | ↑ | | | | | | |
| | SX 320 | | ↓ | ↓ | ↑ | ↑ | | | | | | |
| | SX 480 | | | ↓ | ↑ | ↑ | | | | | | |
| | SX 570 | | | | ↑ | ↑ | ↑ | ↑ | | | | |
| | SX 660 | | | | ↑ | ↑ | ↑ | ↑ | | | | |

Note: To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
| | | | 18 x 19 Multiplier | 27 x 27 Multiplier | | |
| | SX 320 | 984 | 1,968 | 984 | 984 | 984 |
| | SX 480 | 1,368 | 2,736 | 1,368 | 1,368 | 1,368 |
| | SX 570 | 1,523 | 3,046 | 1,523 | 1,523 | 1,523 |
| | SX 660 | 1,687 | 3,374 | 1,687 | 1,687 | 1,687 |

Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant | Product Line | Variable-precision DSP Block | Single Precision Floating-Point Multiplication Mode | Single-Precision Floating-Point Adder Mode | Single-Precision Floating-Point Multiply Accumulate Mode | Peak Giga Floating-Point Operations per Second (GFLOPs) |
|-------------------|--------------|------------------------------|---|--|--|---|
| Intel Arria 10 GX | GX 160 | 156 | 156 | 156 | 156 | 140 |
| | GX 220 | 192 | 192 | 192 | 192 | 173 |
| | GX 270 | 830 | 830 | 830 | 830 | 747 |
| | GX 320 | 984 | 984 | 984 | 984 | 886 |
| | GX 480 | 1,369 | 1,368 | 1,368 | 1,368 | 1,231 |
| | GX 570 | 1,523 | 1,523 | 1,523 | 1,523 | 1,371 |
| | GX 660 | 1,687 | 1,687 | 1,687 | 1,687 | 1,518 |
| | GX 900 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| | GX 1150 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| Intel Arria 10 GT | GT 900 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| | GT 1150 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| Intel Arria 10 SX | SX 160 | 156 | 156 | 156 | 156 | 140 |
| | SX 220 | 192 | 192 | 192 | 192 | 173 |
| | SX 270 | 830 | 830 | 830 | 830 | 747 |
| | SX 320 | 984 | 984 | 984 | 984 | 886 |
| | SX 480 | 1,369 | 1,368 | 1,368 | 1,368 | 1,231 |
| | SX 570 | 1,523 | 1,523 | 1,523 | 1,523 | 1,371 |
| | SX 660 | 1,687 | 1,687 | 1,687 | 1,687 | 1,518 |

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

**Table 20. Memory Standards Supported by the Hard Memory Controller**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

| Memory Standard | Rate Support | Ping Pong PHY Support | Maximum Frequency (MHz) |
|-----------------|--------------|-----------------------|-------------------------|
| DDR4 SDRAM | Quarter rate | Yes | 1,067 |
| | | — | 1,200 |
| DDR3 SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 1,067 |
| | | — | 1,067 |
| DDR3L SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 933 |
| | | — | 933 |
| LPDDR3 SDRAM | Half rate | — | 533 |
| | Quarter rate | — | 800 |

Table 21. Memory Standards Supported by the Soft Memory Controller

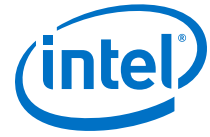
| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|-----------------------------|--------------|-------------------------|
| RLDRAM 3 ⁽¹¹⁾ | Quarter rate | 1,200 |
| QDR IV SRAM ⁽¹¹⁾ | Quarter rate | 1,067 |
| QDR II SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ Xtreme SRAM | Full rate | 333 |
| | Half rate | 633 |

Table 22. Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|-----------------|--------------|-------------------------|
| DDR4 SDRAM | Half rate | 1,200 |
| DDR3 SDRAM | Half rate | 1,067 |
| DDR3L SDRAM | Half rate | 933 |

⁽¹¹⁾ Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

Related Information

[PCS Features](#) on page 30

Low Power Serial Transceivers

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps
- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization
- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps
- All channels feature continuous data rate support up to the maximum rated speed



Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices

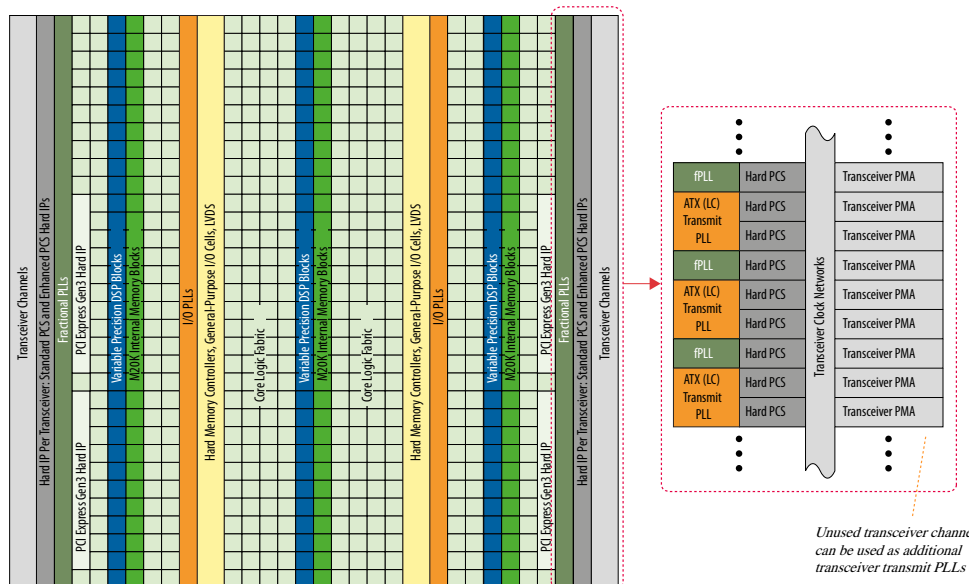
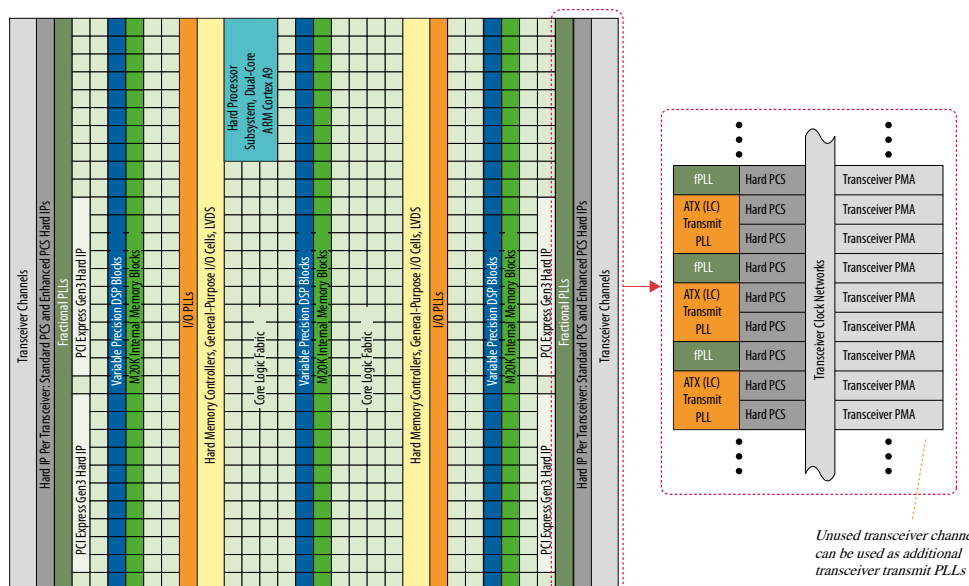


Figure 8. Device Chip Overview for Intel Arria 10 SX Devices



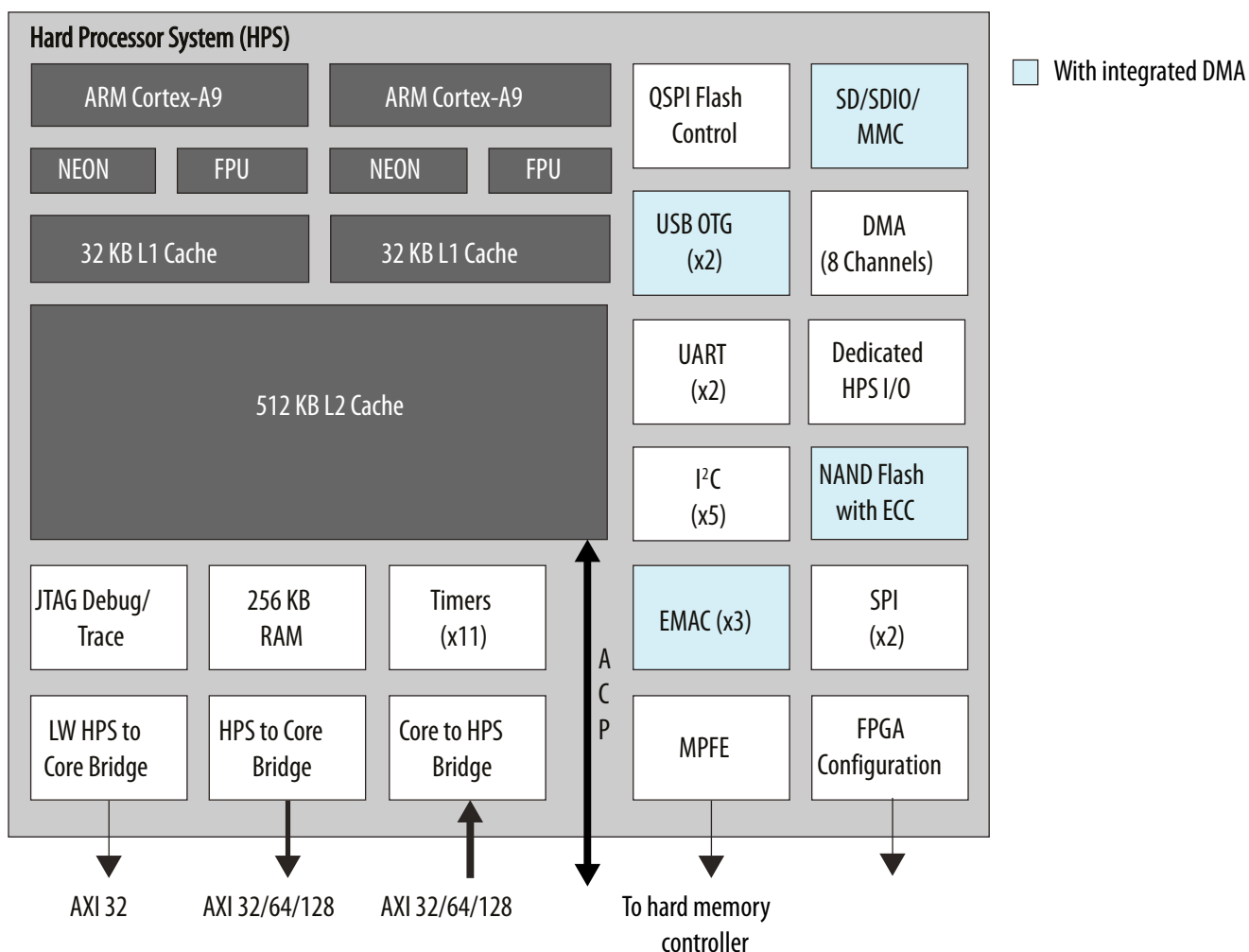
PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.



Figure 9. HPS Block Diagram

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.



Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
 - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
 - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
 - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
 - 32 KB of L1 instruction cache, 32 KB of L1 data cache
 - Single- and double-precision floating-point unit and NEON media engine
 - CoreSight debug and trace technology
 - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I²C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)



| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) ⁽¹³⁾ | Decompression | Design Security ⁽¹⁴⁾ | Partial Reconfiguration ⁽¹⁵⁾ | Remote System Update |
|--|----------------------|----------------------|--------------------------------------|---------------|---------------------------------|---|----------------------|
| Fast passive parallel (FPP) through CPLD or external microcontroller | 8 bits | 100 | 3200 | Yes | Yes | Yes ⁽¹⁷⁾ | PFL IP core |
| | 16 bits | | | Yes | Yes | | |
| | 32 bits | | | Yes | Yes | | |
| Configuration via HPS | 16 bits | 100 | 3200 | Yes | Yes | Yes ⁽¹⁷⁾ | — |
| | 32 bits | | | Yes | Yes | | |
| Configuration via Protocol [CvP (PCIe*)] | x1, x2, x4, x8 lanes | — | 8000 | Yes | Yes | Yes ⁽¹⁶⁾ | — |

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

Power Management

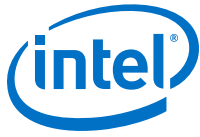
Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

⁽¹³⁾ Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

⁽¹⁴⁾ Encryption and compression cannot be used simultaneously.

⁽¹⁵⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

⁽¹⁷⁾ Supported at a maximum clock rate of 100 MHz.



The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

Document Revision History for Intel Arria 10 Device Overview

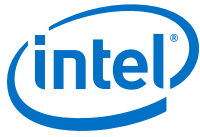
| Document Version | Changes |
|------------------|--|
| 2018.04.09 | Updated the lowest V_{CC} from 0.83 V to 0.82 V in the topic listing a summary of the device features. |

| Date | Version | Changes |
|--------------|------------|---|
| January 2018 | 2018.01.17 | <ul style="list-style-type: none">• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.• Updated maximum frequency supported for half rate QDR II and QDR II + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft Memory Controller</i> table.• Updated transceiver backplane capability to 12.5 Gbps.• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure. |
| continued... | | |



| Date | Version | Changes |
|----------------|------------|--|
| | | <ul style="list-style-type: none"> Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure. Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps. Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table. |
| September 2017 | 2017.09.20 | Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps. |
| July 2017 | 2017.07.13 | Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C". |
| July 2017 | 2017.07.06 | Added automotive temperature option to Intel Arria 10 GX device family. |
| May 2017 | 2017.05.08 | <ul style="list-style-type: none"> Corrected protocol names with "1588" to "IEEE 1588v2". Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants. Removed all "Preliminary" marks. |
| March 2017 | 2017.03.15 | <ul style="list-style-type: none"> Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices. Rebranded as Intel. |
| October 2016 | 2016.10.31 | <ul style="list-style-type: none"> Removed package F36 from Intel Arria 10 GX devices. Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers. |
| May 2016 | 2016.05.02 | <ul style="list-style-type: none"> Updated the FPGA Configuration and HPS Booting topic. Remove V_{CC} PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices. Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA. Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices. |
| February 2016 | 2016.02.11 | <ul style="list-style-type: none"> Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally. Revised the state for Core clock networks in the Summary of Features topic. Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table. Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table. Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table. Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure. Changed transceiver parameters in the "Low Power Serial Transceivers" section. Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table. Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure. Changed the datarates for GT devices in the "PMA Features" section. Changed the datarates for GT devices in the "PCS Features" section. |

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| Date | Version | Changes |
|----------------|------------|---|
| December 2015 | 2015.12.14 | <ul style="list-style-type: none"> Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb. Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources. |
| November 2015 | 2015.11.02 | <ul style="list-style-type: none"> Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660. Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in Number of Multipliers in Intel Arria 10 Devices table. Updated the available options for Arria 10 GX, GT, and SX. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>. |
| June 2015 | 2015.06.15 | Corrected label for Intel Arria 10 GT product lines in the vertical migration figure. |
| May 2015 | 2015.05.15 | Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller. |
| May 2015 | 2015.05.04 | <ul style="list-style-type: none"> Added support for 13.5G JESD204b in the Summary of Features table. Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic. Added a note to the table, Maximum Resource Counts for Arria 10 GT devices. Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic. |
| January 2015 | 2015.01.23 | <ul style="list-style-type: none"> Added floating point arithmetic features in the Summary of Features table. Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb. Updated the table that lists the memory standards supported by Intel Arria 10 devices. Removed support for DDR3U, LPDDR3 SDRAM, RLD RAM 2, and DDR2. Moved RLD RAM 3 support from hard memory controller to soft memory controller. RLD RAM 3 support uses hard PHY with soft memory controller. Added soft memory controller support for QDR IV. Updated the maximum resource count table to include the number of hard memory controllers available in each device variant. Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps. Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz. Added a feature for fractional synthesis PLLs: PLL cascading. Updated the HPS programmable general-purpose I/Os from 54 to 62. |
| September 2014 | 2014.09.30 | <ul style="list-style-type: none"> Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX. Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660. Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150. |
| continued... | | |