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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

|                         |   |
|-------------------------|---|
| Product Status          | Active  |
| Architecture            | MCU, FPGA   |
| Core Processor          | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™  |
| Flash Size              | -   |
| RAM Size                | 256KB   |
| Peripherals             | DMA, POR, WDT   |
| Connectivity            | EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG  |
| Speed                   | 1.5GHz  |
| Primary Attributes      | FPGA - 220K Logic Elements  |
| Operating Temperature   | -40°C ~ 100°C (TJ)  |
| Package / Case          | 780-BBGA, FCBGA   |
| Supplier Device Package | 780-FBGA, FC (29x29)  |
| Purchase URL            | <a href="https://www.e-xfl.com/product-detail/intel/10as022e3f29i2lg">https://www.e-xfl.com/product-detail/intel/10as022e3f29i2lg</a> |



| Feature                                 | Description   |  |
|---|---|--|
| Low-power serial transceivers           | <ul style="list-style-type: none"><li>Continuous operating range:<ul style="list-style-type: none"><li>Intel Arria 10 GX—1 Gbps to 17.4 Gbps</li><li>Intel Arria 10 GT—1 Gbps to 25.8 Gbps</li></ul></li><li>Backplane support:<ul style="list-style-type: none"><li>Intel Arria 10 GX—up to 12.5</li><li>Intel Arria 10 GT—up to 12.5</li></ul></li><li>Extended range down to 125 Mbps with oversampling</li><li>ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module</li><li>Adaptive linear and decision feedback equalization</li><li>Transmitter pre-emphasis and de-emphasis</li><li>Dynamic partial reconfiguration of individual transceiver channels</li></ul> |  |
| HPS<br>(Intel Arria 10 SX devices only) | Processor and system  | <ul style="list-style-type: none"><li>Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability</li><li>256 KB on-chip RAM and 64 KB on-chip ROM</li><li>System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li><li>Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)</li><li>ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage</li></ul>   |
|   | External interfaces   | <ul style="list-style-type: none"><li>Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller</li><li>Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I<sup>2</sup>C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)</li></ul>   |
|   | Interconnects to core   | <ul style="list-style-type: none"><li>High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write</li><li>HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li><li>Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port</li><li>FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller</li></ul> |
| Configuration                           | <ul style="list-style-type: none"><li>Tamper protection—comprehensive design protection to protect your valuable IP investments</li><li>Enhanced 256-bit advanced encryption standard (AES) design security with authentication</li><li>Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3</li></ul>   |  |
| continued...                            |   |  |

(2) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



| Feature            | Description   |
|--------------------|---|
|                    | <ul style="list-style-type: none"><li>Dynamic reconfiguration of the transceivers and PLLs</li><li>Fine-grained partial reconfiguration of the core fabric</li><li>Active Serial x4 Interface</li></ul>   |
| Power management   | <ul style="list-style-type: none"><li>SmartVID</li><li>Low static power device options</li><li>Programmable Power Technology</li><li>Intel Quartus Prime integrated power analysis</li></ul>  |
| Software and tools | <ul style="list-style-type: none"><li>Intel Quartus Prime design suite</li><li>Transceiver toolkit</li><li>Platform Designer system integration tool</li><li>DSP Builder for Intel FPGAs</li><li>OpenCL™ support</li><li>Intel SoC FPGA Embedded Design Suite (EDS)</li></ul> |

### Related Information

#### [Intel Arria 10 Transceiver PHY Overview](#)

Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

**Table 4. Device Variants for the Intel Arria 10 Device Family**

| Variant           | Description   |
|-------------------|---|
| Intel Arria 10 GX | FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.  |
| Intel Arria 10 GT | FPGA featuring: <ul style="list-style-type: none"><li>17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.</li><li>25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules.</li></ul> |
| Intel Arria 10 SX | SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.  |

### Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

#### [Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



## Maximum Resources

**Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)**

| Resource                     |                      | Product Line |         |         |         |         |
|------------------------------|----------------------|--------------|---------|---------|---------|---------|
|                              |                      | GX 160       | GX 220  | GX 270  | GX 320  | GX 480  |
| Logic Elements (LE) (K)      |                      | 160          | 220     | 270     | 320     | 480     |
| ALM                          |                      | 61,510       | 80,330  | 101,620 | 119,900 | 183,590 |
| Register                     |                      | 246,040      | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb)                  | M20K                 | 8,800        | 11,740  | 15,000  | 17,820  | 28,620  |
|                              | MLAB                 | 1,050        | 1,690   | 2,452   | 2,727   | 4,164   |
| Variable-precision DSP Block |                      | 156          | 192     | 830     | 985     | 1,368   |
| 18 x 19 Multiplier           |                      | 312          | 384     | 1,660   | 1,970   | 2,736   |
| PLL                          | Fractional Synthesis | 6            | 6       | 8       | 8       | 12      |
|                              | I/O                  | 6            | 6       | 8       | 8       | 12      |
| 17.4 Gbps Transceiver        |                      | 12           | 12      | 24      | 24      | 36      |
| GPIO <sup>(3)</sup>          |                      | 288          | 288     | 384     | 384     | 492     |
| LVDS Pair <sup>(4)</sup>     |                      | 120          | 120     | 168     | 168     | 222     |
| PCIe Hard IP Block           |                      | 1            | 1       | 2       | 2       | 2       |
| Hard Memory Controller       |                      | 6            | 6       | 8       | 8       | 12      |

<sup>(3)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(4)</sup> Each LVDS I/O pair can be used as differential input or output.



## Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

## Available Options

**Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices**



### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



## Maximum Resources

**Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices**

| Resource                       |                      | Product Line |         |         |         |         |         |           |
|--------------------------------|----------------------|--------------|---------|---------|---------|---------|---------|-----------|
|                                |                      | SX 160       | SX 220  | SX 270  | SX 320  | SX 480  | SX 570  | SX 660    |
| Logic Elements (LE) (K)        |                      | 160          | 220     | 270     | 320     | 480     | 570     | 660       |
| ALM                            |                      | 61,510       | 80,330  | 101,620 | 119,900 | 183,590 | 217,080 | 251,680   |
| Register                       |                      | 246,040      | 321,320 | 406,480 | 479,600 | 734,360 | 868,320 | 1,006,720 |
| Memory (Kb)                    | M20K                 | 8,800        | 11,740  | 15,000  | 17,820  | 28,620  | 36,000  | 42,620    |
|                                | MLAB                 | 1,050        | 1,690   | 2,452   | 2,727   | 4,164   | 5,096   | 5,788     |
| Variable-precision DSP Block   |                      | 156          | 192     | 830     | 985     | 1,368   | 1,523   | 1,687     |
| 18 x 19 Multiplier             |                      | 312          | 384     | 1,660   | 1,970   | 2,736   | 3,046   | 3,374     |
| PLL                            | Fractional Synthesis | 6            | 6       | 8       | 8       | 12      | 16      | 16        |
|                                | I/O                  | 6            | 6       | 8       | 8       | 12      | 16      | 16        |
| 17.4 Gbps Transceiver          |                      | 12           | 12      | 24      | 24      | 36      | 48      | 48        |
| GPIO <sup>(8)</sup>            |                      | 288          | 288     | 384     | 384     | 492     | 696     | 696       |
| LVDS Pair <sup>(9)</sup>       |                      | 120          | 120     | 168     | 168     | 174     | 324     | 324       |
| PCIe Hard IP Block             |                      | 1            | 1       | 2       | 2       | 2       | 2       | 2         |
| Hard Memory Controller         |                      | 6            | 6       | 8       | 8       | 12      | 16      | 16        |
| ARM Cortex-A9 MPCore Processor |                      | Yes          | Yes     | Yes     | Yes     | Yes     | Yes     | Yes       |

## Package Plan

**Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGGA) |             |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |             |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |             |      | F34<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      |
|--------------|--|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
|              | 3 V<br>I/O                               | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                               | LVDS<br>I/O | XCVR |
| SX 160       | 48                                       | 144         | 6    | 48                                      | 192         | 12   | 48                                      | 240         | 12   | —  | —           | —    |
| SX 220       | 48                                       | 144         | 6    | 48                                      | 192         | 12   | 48                                      | 240         | 12   | —  | —           | —    |
| SX 270       | —  | —           | —    | 48                                      | 192         | 12   | 48                                      | 312         | 12   | 48                                       | 336         | 24   |
| SX 320       | —  | —           | —    | 48                                      | 192         | 12   | 48                                      | 312         | 12   | 48                                       | 336         | 24   |
| continued... |  |             |      |   |             |      |   |             |      |  |             |      |

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(9)</sup> Each LVDS I/O pair can be used as differential input or output.



| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGA) |             |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |             |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |             |      | F34<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
|              | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                               | LVDS<br>I/O | XCVR |
| SX 480       | —                                       | —           | —    | —                                       | —           | —    | 48                                      | 312         | 12   | 48                                       | 444         | 24   |
| SX 570       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |
| SX 660       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |

**Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35<br>(35 mm × 35 mm,<br>1152-pin FBGA) |          |      | KF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      | NF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      |
|--------------|--|----------|------|---|----------|------|---|----------|------|
|              | 3 V I/O                                  | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR |
| SX 270       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 320       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 480       | 48                                       | 348      | 36   | —   | —        | —    | —   | —        | —    |
| SX 570       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |
| SX 660       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |

#### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.



**Figure 5. ALM for Intel Arria 10 Devices**



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

## Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
|         |              |                              | 18 x 19 Multiplier                                    | 27 x 27 Multiplier |                                   |   |
|         | SX 320       | 984                          | 1,968   | 984                | 984                               | 984   |
|         | SX 480       | 1,368                        | 2,736   | 1,368              | 1,368                             | 1,368   |
|         | SX 570       | 1,523                        | 3,046   | 1,523              | 1,523                             | 1,523   |
|         | SX 660       | 1,687                        | 3,374   | 1,687              | 1,687                             | 1,687   |

**Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant           | Product Line | Variable-precision DSP Block | Single Precision Floating-Point Multiplication Mode | Single-Precision Floating-Point Adder Mode | Single-Precision Floating-Point Multiply Accumulate Mode | Peak Giga Floating-Point Operations per Second (GFLOPs) |
|-------------------|--------------|------------------------------|---|--|--|---|
| Intel Arria 10 GX | GX 160       | 156                          | 156   | 156  | 156  | 140   |
|                   | GX 220       | 192                          | 192   | 192  | 192  | 173   |
|                   | GX 270       | 830                          | 830   | 830  | 830  | 747   |
|                   | GX 320       | 984                          | 984   | 984  | 984  | 886   |
|                   | GX 480       | 1,369                        | 1,368   | 1,368                                      | 1,368  | 1,231   |
|                   | GX 570       | 1,523                        | 1,523   | 1,523                                      | 1,523  | 1,371   |
|                   | GX 660       | 1,687                        | 1,687   | 1,687                                      | 1,687  | 1,518   |
|                   | GX 900       | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
|                   | GX 1150      | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
| Intel Arria 10 GT | GT 900       | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
|                   | GT 1150      | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
| Intel Arria 10 SX | SX 160       | 156                          | 156   | 156  | 156  | 140   |
|                   | SX 220       | 192                          | 192   | 192  | 192  | 173   |
|                   | SX 270       | 830                          | 830   | 830  | 830  | 747   |
|                   | SX 320       | 984                          | 984   | 984  | 984  | 886   |
|                   | SX 480       | 1,369                        | 1,368   | 1,368                                      | 1,368  | 1,231   |
|                   | SX 570       | 1,523                        | 1,523   | 1,523                                      | 1,523  | 1,371   |
|                   | SX 660       | 1,687                        | 1,687   | 1,687                                      | 1,687  | 1,518   |

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

## Embedded Memory Configurations for Single-port Mode

**Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices**

This table lists the maximum configurations supported for single-port RAM and ROM modes.

| Memory Block | Depth (bits)       | Programmable Width |
|--------------|--------------------|--------------------|
| MLAB         | 32                 | x16, x18, or x20   |
|              | 64 <sup>(10)</sup> | x8, x9, x10        |
| M20K         | 512                | x40, x32           |
|              | 1K                 | x20, x16           |
|              | 2K                 | x10, x8            |
|              | 4K                 | x5, x4             |
|              | 8K                 | x2                 |
|              | 16K                | x1                 |

## Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

### Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

### Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

### Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

<sup>(10)</sup> Supported through software emulation and consumes additional MLAB blocks.



### **Related Information**

#### [Intel Arria 10 Device Datasheet](#)

Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

## **PCIe Gen1, Gen2, and Gen3 Hard IP**

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

### **Related Information**

[PCS Features](#) on page 30

## **Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet**

### **Interlaken Support**

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

### **Related Information**

[PCS Features](#) on page 30

### **10 Gbps Ethernet Support**

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

Figure 6. Intel Arria 10 Transceiver Block Architecture



## Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.



Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices



Figure 8. Device Chip Overview for Intel Arria 10 SX Devices

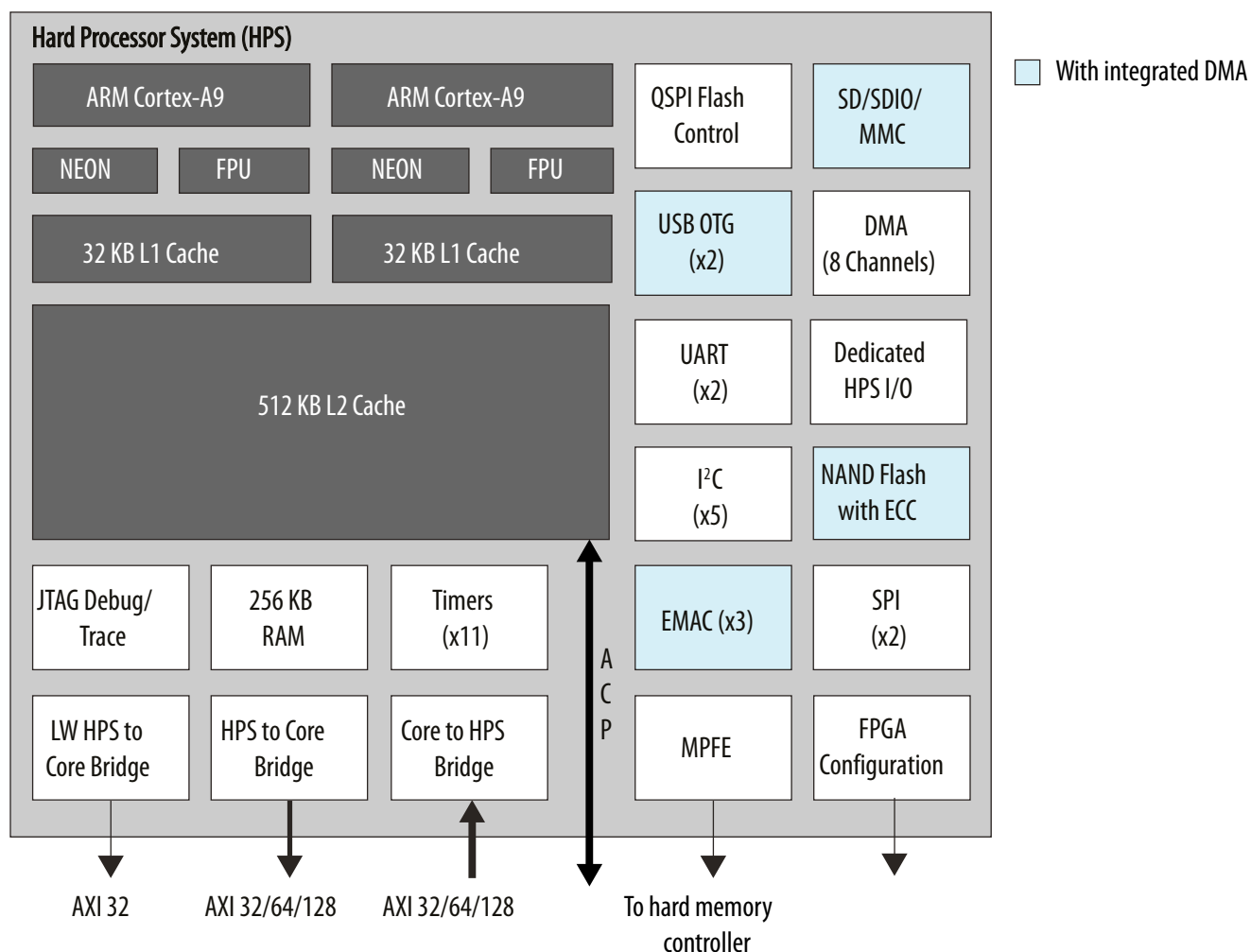


## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.

**Figure 9. HPS Block Diagram**

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



## Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.



**Table 24. Improvements in 20 nm HPS**

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/<br>Improvements                           | Description   |
|---|---|
| Increased performance and overdrive capability        | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.   |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.   |
| Flexible I/O sharing                                  | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none"><li>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.</li><li>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.</li><li>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.</li></ul> |
| EMAC core   | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I <sup>2</sup> C interface.  |
| On-chip memory  | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.  |
| ECC enhancements                                      | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.   |
| HPS to FPGA Interconnect Backbone                     | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.  |
| FPGA configuration and HPS booting                    | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.<br>You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.  |
| Security  | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).   |





## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux\*, VxWorks\*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

### Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

### Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

## Enhanced Configuration and Configuration via Protocol

**Table 25. Configuration Schemes and Features of Intel Arria 10 Devices**

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme   | Data Width    | Max Clock Rate (MHz) | Max Data Rate (Mbps) <sup>(13)</sup> | Decompression | Design Security <sup>(14)</sup> | Partial Reconfiguration <sup>(15)</sup> | Remote System Update                |
|--|---------------|----------------------|--------------------------------------|---------------|---------------------------------|---|-------------------------------------|
| JTAG   | 1 bit         | 33                   | 33                                   | —             | —                               | Yes <sup>(16)</sup>                     | —                                   |
| Active Serial (AS) through the EPCQ-L configuration device   | 1 bit, 4 bits | 100                  | 400                                  | Yes           | Yes                             | Yes <sup>(16)</sup>                     | Yes                                 |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit         | 100                  | 100                                  | Yes           | Yes                             | Yes <sup>(16)</sup>                     | Parallel Flash Loader (PFL) IP core |

*continued...*

<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(16)</sup> Partial configuration can be performed only when it is configured as internal host.



| Scheme   | Data Width           | Max Clock Rate (MHz) | Max Data Rate (Mbps) <sup>(13)</sup> | Decompression | Design Security <sup>(14)</sup> | Partial Reconfiguration <sup>(15)</sup> | Remote System Update |
|--|----------------------|----------------------|--------------------------------------|---------------|---------------------------------|---|----------------------|
| Fast passive parallel (FPP) through CPLD or external microcontroller | 8 bits               | 100                  | 3200                                 | Yes           | Yes                             | Yes <sup>(17)</sup>                     | PFL IP core          |
|  | 16 bits              |                      |                                      | Yes           | Yes                             |   |                      |
|  | 32 bits              |                      |                                      | Yes           | Yes                             |   |                      |
| Configuration via HPS  | 16 bits              | 100                  | 3200                                 | Yes           | Yes                             | Yes <sup>(17)</sup>                     | —                    |
|  | 32 bits              |                      |                                      | Yes           | Yes                             |   |                      |
| Configuration via Protocol [CvP (PCIe*)]                             | x1, x2, x4, x8 lanes | —                    | 8000                                 | Yes           | Yes                             | Yes <sup>(16)</sup>                     | —                    |

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

## SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

## Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(17)</sup> Supported at a maximum clock rate of 100 MHz.



| Date           | Version    | Changes   |
|----------------|------------|---|
| December 2015  | 2015.12.14 | <ul style="list-style-type: none"><li>Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb.</li><li>Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources.</li></ul>  |
| November 2015  | 2015.11.02 | <ul style="list-style-type: none"><li>Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660.</li><li>Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in <b>Number of Multipliers in Intel Arria 10 Devices</b> table.</li><li>Updated the available options for Arria 10 GX, GT, and SX.</li><li>Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li></ul>   |
| June 2015      | 2015.06.15 | Corrected label for Intel Arria 10 GT product lines in the vertical migration figure.   |
| May 2015       | 2015.05.15 | Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller.  |
| May 2015       | 2015.05.04 | <ul style="list-style-type: none"><li>Added support for 13.5G JESD204b in the Summary of Features table.</li><li>Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic.</li><li>Added a note to the table, Maximum Resource Counts for Arria 10 GT devices.</li><li>Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic.</li></ul>  |
| January 2015   | 2015.01.23 | <ul style="list-style-type: none"><li>Added floating point arithmetic features in the Summary of Features table.</li><li>Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb.</li><li>Updated the table that lists the memory standards supported by Intel Arria 10 devices.</li><li>Removed support for DDR3U, LPDDR3 SDRAM, RLD RAM 2, and DDR2.</li><li>Moved RLD RAM 3 support from hard memory controller to soft memory controller. RLD RAM 3 support uses hard PHY with soft memory controller.</li><li>Added soft memory controller support for QDR IV.</li><li>Updated the maximum resource count table to include the number of hard memory controllers available in each device variant.</li><li>Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps.</li><li>Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz.</li><li>Added a feature for fractional synthesis PLLs: PLL cascading.</li><li>Updated the HPS programmable general-purpose I/Os from 54 to 62.</li></ul> |
| September 2014 | 2014.09.30 | <ul style="list-style-type: none"><li>Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX.</li><li>Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660.</li><li>Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150.</li></ul>   |
| continued...   |            |   |



| Date          | Version    | Changes  |
|---------------|------------|--|
| August 2014   | 2014.08.18 | <ul style="list-style-type: none"> <li>Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620.</li> <li>Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table.</li> <li>Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration.</li> <li>Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller.</li> <li>Added variable precision DSP blocks support for floating-point arithmetic.</li> </ul> |
| June 2014     | 2014.06.19 | Updated number of dedicated I/Os in the HPS block to 17.   |
| February 2014 | 2014.02.21 | Updated transceiver speed grade options for GT devices in Figure 2.  |
| February 2014 | 2014.02.06 | Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps.   |
| December 2013 | 2013.12.10 | <ul style="list-style-type: none"> <li>Updated the HPS memory standards support from LPDDR2 to LPDDR3.</li> <li>Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/MMC, DMA, SPI and NAND Flash with ECC blocks .</li> </ul>   |
| December 2013 | 2013.12.02 | Initial release.   |