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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 270K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA, FC (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/10as027h2f34i2lg">https://www.e-xfl.com/product-detail/intel/10as027h2f34i2lg</a>



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Feature	Description	
Embedded Hard IP blocks	Variable-precision DSP	<ul style="list-style-type: none"><li>Native support for signal processing precision levels from 18 x 19 to 54 x 54</li><li>Native support for 27 x 27 multiplier mode</li><li>64-bit accumulator and cascade for systolic finite impulse responses (FIRs)</li><li>Internal coefficient memory banks</li><li>Padder/subtractor for improved efficiency</li><li>Additional pipeline register to increase performance and reduce power</li><li>Supports floating point arithmetic:<ul style="list-style-type: none"><li>Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.</li><li>Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.</li><li>Dynamic accumulator reset control.</li><li>Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.</li></ul></li></ul>
	Memory controller	DDR4, DDR3, and DDR3L
	PCI Express*	PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port
	Transceiver I/O	<ul style="list-style-type: none"><li>10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)</li><li>PCS hard IPs that support:<ul style="list-style-type: none"><li>10-Gbps Ethernet (10GbE)</li><li>PCIe PIPE interface</li><li>Interlaken</li><li>Gbps Ethernet (GbE)</li><li>Common Public Radio Interface (CPRI) with deterministic latency support</li><li>Gigabit-capable passive optical network (GPON) with fast lock-time support</li></ul></li><li>13.5G JESD204b</li><li>8B/10B, 64B/66B, 64B/67B encoders and decoders</li><li>Custom mode support for proprietary protocols</li></ul>
Core clock networks	<ul style="list-style-type: none"><li>Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none"><li>667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface</li><li>800 MHz LVDS interface clocking with 1,600 Mbps LVDS interface</li></ul></li><li>Global, regional, and peripheral clock networks</li><li>Clock networks that are not used can be gated to reduce dynamic power</li></ul>	
Phase-locked loops (PLLs)	<ul style="list-style-type: none"><li>High-resolution fractional synthesis PLLs:<ul style="list-style-type: none"><li>Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)</li><li>Support integer mode and fractional mode</li><li>Fractional mode support with third-order delta-sigma modulation</li></ul></li><li>Integer PLLs:<ul style="list-style-type: none"><li>Adjacent to general purpose I/Os</li><li>Support external memory and LVDS interfaces</li></ul></li></ul>	
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"><li>1.6 Gbps LVDS—every pair can be configured as receiver or transmitter</li><li>On-chip termination (OCT)</li><li>1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing</li></ul>	
External Memory Interface	<ul style="list-style-type: none"><li>Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none"><li>DDR4—speeds up to 1,200 MHz/2,400 Mbps</li><li>DDR3—speeds up to 1,067 MHz/2,133 Mbps</li></ul></li><li>Soft memory controller—provides support for RLDRAM 3<sup>(2)</sup>, QDR IV<sup>(2)</sup>, and QDR II+</li></ul>	
continued...		



Feature	Description	
Low-power serial transceivers	<ul style="list-style-type: none"><li>Continuous operating range:<ul style="list-style-type: none"><li>Intel Arria 10 GX—1 Gbps to 17.4 Gbps</li><li>Intel Arria 10 GT—1 Gbps to 25.8 Gbps</li></ul></li><li>Backplane support:<ul style="list-style-type: none"><li>Intel Arria 10 GX—up to 12.5</li><li>Intel Arria 10 GT—up to 12.5</li></ul></li><li>Extended range down to 125 Mbps with oversampling</li><li>ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module</li><li>Adaptive linear and decision feedback equalization</li><li>Transmitter pre-emphasis and de-emphasis</li><li>Dynamic partial reconfiguration of individual transceiver channels</li></ul>	
HPS (Intel Arria 10 SX devices only)	Processor and system	<ul style="list-style-type: none"><li>Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability</li><li>256 KB on-chip RAM and 64 KB on-chip ROM</li><li>System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li><li>Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)</li><li>ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage</li></ul>
	External interfaces	<ul style="list-style-type: none"><li>Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller</li><li>Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I<sup>2</sup>C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)</li></ul>
	Interconnects to core	<ul style="list-style-type: none"><li>High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write</li><li>HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li><li>Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port</li><li>FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller</li></ul>
Configuration	<ul style="list-style-type: none"><li>Tamper protection—comprehensive design protection to protect your valuable IP investments</li><li>Enhanced 256-bit advanced encryption standard (AES) design security with authentication</li><li>Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3</li></ul>	
continued...		

<sup>(2)</sup> Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Feature	Description
	<ul style="list-style-type: none"><li>Dynamic reconfiguration of the transceivers and PLLs</li><li>Fine-grained partial reconfiguration of the core fabric</li><li>Active Serial x4 Interface</li></ul>
Power management	<ul style="list-style-type: none"><li>SmartVID</li><li>Low static power device options</li><li>Programmable Power Technology</li><li>Intel Quartus Prime integrated power analysis</li></ul>
Software and tools	<ul style="list-style-type: none"><li>Intel Quartus Prime design suite</li><li>Transceiver toolkit</li><li>Platform Designer system integration tool</li><li>DSP Builder for Intel FPGAs</li><li>OpenCL™ support</li><li>Intel SoC FPGA Embedded Design Suite (EDS)</li></ul>

### Related Information

#### [Intel Arria 10 Transceiver PHY Overview](#)

Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

**Table 4. Device Variants for the Intel Arria 10 Device Family**

Variant	Description
Intel Arria 10 GX	FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.
Intel Arria 10 GT	FPGA featuring: <ul style="list-style-type: none"><li>17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.</li><li>25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules.</li></ul>
Intel Arria 10 SX	SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.

## Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

#### [Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



## Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



## Related Information

### Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



## Maximum Resources

**Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)**

Resource		Product Line				
		GX 160	GX 220	GX 270	GX 320	GX 480
Logic Elements (LE) (K)		160	220	270	320	480
ALM		61,510	80,330	101,620	119,900	183,590
Register		246,040	321,320	406,480	479,600	734,360
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620
	MLAB	1,050	1,690	2,452	2,727	4,164
Variable-precision DSP Block		156	192	830	985	1,368
18 x 19 Multiplier		312	384	1,660	1,970	2,736
PLL	Fractional Synthesis	6	6	8	8	12
	I/O	6	6	8	8	12
17.4 Gbps Transceiver		12	12	24	24	36
GPIO <sup>(3)</sup>		288	288	384	384	492
LVDS Pair <sup>(4)</sup>		120	120	168	168	222
PCIe Hard IP Block		1	1	2	2	2
Hard Memory Controller		6	6	8	8	12

<sup>(3)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(4)</sup> Each LVDS I/O pair can be used as differential input or output.

**Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F34 (35 mm × 35 mm, 1152-pin FBGA)			F35 (35 mm × 35 mm, 1152-pin FBGA)			KF40 (40 mm × 40 mm, 1517-pin FBGA)			NF40 (40 mm × 40 mm, 1517-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 270	48	336	24	48	336	24	—	—	—	—	—	—
GX 320	48	336	24	48	336	24	—	—	—	—	—	—
GX 480	48	444	24	48	348	36	—	—	—	—	—	—
GX 570	48	444	24	48	348	36	96	600	36	48	540	48
GX 660	48	444	24	48	348	36	96	600	36	48	540	48
GX 900	—	504	24	—	—	—	—	—	—	—	600	48
GX 1150	—	504	24	—	—	—	—	—	—	—	600	48

**Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	RF40 (40 mm × 40 mm, 1517-pin FBGA)			NF45 (45 mm × 45 mm) 1932-pin FBGA)			SF45 (45 mm × 45 mm) 1932-pin FBGA)			UF45 (45 mm × 45 mm) 1932-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 900	—	342	66	—	768	48	—	624	72	—	480	96
GX 1150	—	342	66	—	768	48	—	624	72	—	480	96

### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

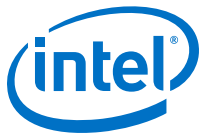
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

[Intel FPGA Product Selector](#)

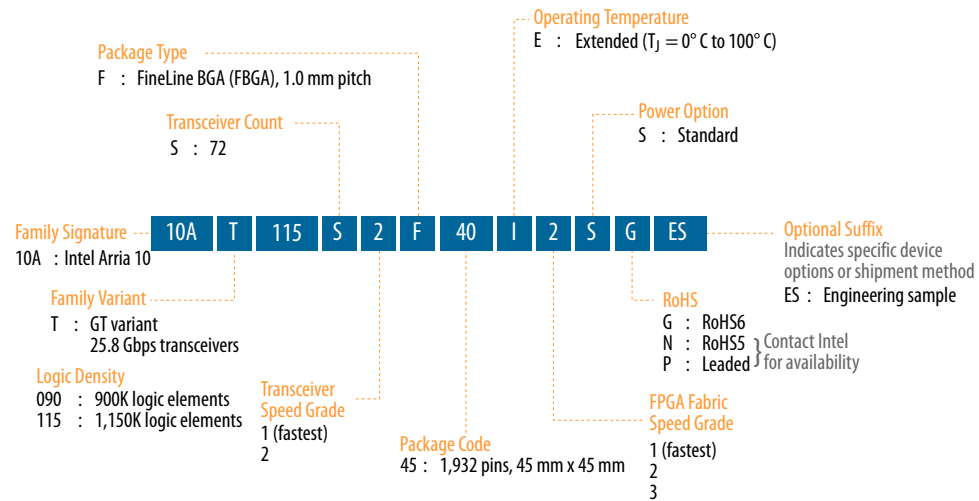
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## Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

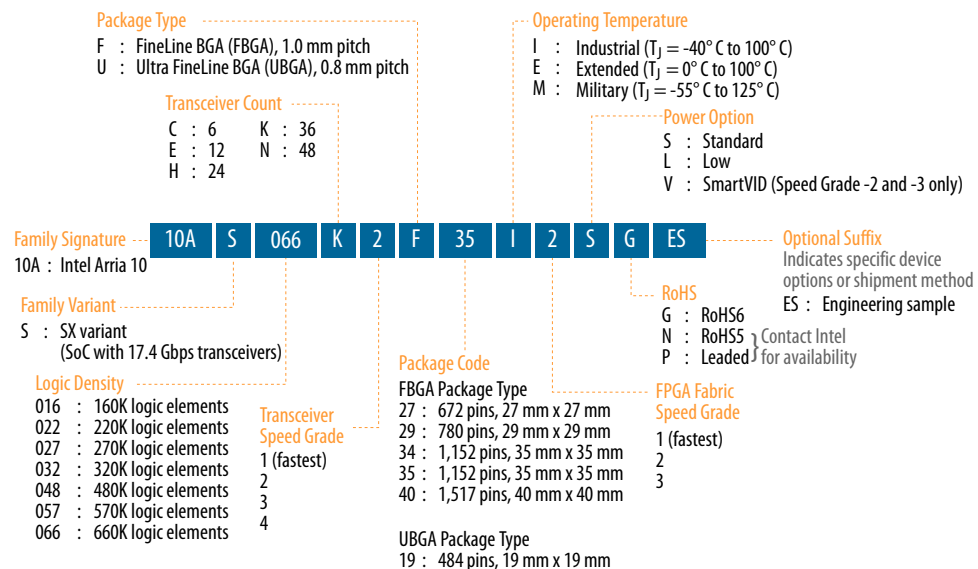
### Related Information

Intel FPGA Product Selector

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## Available Options

**Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices**



### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



## I/O Vertical Migration for Intel Arria 10 Devices

**Figure 4. Migration Capability Across Intel Arria 10 Product Lines**

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.

Variant	Product Line	Package										
		U19	F27	F29	F34	F35	KF40	NF40	RF40	NF45	SF45	UF45
Intel® Arria® 10 GX	GX 160	↑	↑	↑								
	GX 220	↓	↓	↓								
	GX 270		↓	↓	↑	↑						
	GX 320		↓	↓	↑	↑						
	GX 480			↓	↑	↑						
	GX 570				↑	↑	↑	↑				
	GX 660				↑	↑	↑	↑	↑	↑	↑	↑
	GX 900				↑			↑	↑	↑	↑	↑
	GX 1150				↑			↑	↑	↑	↑	↑
	GT 900										↑	↑
	GT 1150										↑	↑
Intel Arria 10 GT	GT 900										↑	↑
	GT 1150										↑	↑
	SX 160	↑	↑	↑								
	SX 220	↓	↓	↓								
	SX 270		↓	↓	↑	↑						
	SX 320		↓	↓	↑	↑						
	SX 480			↓	↑	↑						
	SX 570				↑	↑	↑	↑				
Intel Arria 10 SX	SX 660				↑	↑	↑	↑				

**Note:** To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

## Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
	SX 320	984	1,968	984	984	984
	SX 480	1,368	2,736	1,368	1,368	1,368
	SX 570	1,523	3,046	1,523	1,523	1,523
	SX 660	1,687	3,374	1,687	1,687	1,687

**Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Single Precision Floating-Point Multiplication Mode	Single-Precision Floating-Point Adder Mode	Single-Precision Floating-Point Multiply Accumulate Mode	Peak Giga Floating-Point Operations per Second (GFLOPs)
Intel Arria 10 GX	GX 160	156	156	156	156	140
	GX 220	192	192	192	192	173
	GX 270	830	830	830	830	747
	GX 320	984	984	984	984	886
	GX 480	1,369	1,368	1,368	1,368	1,231
	GX 570	1,523	1,523	1,523	1,523	1,371
	GX 660	1,687	1,687	1,687	1,687	1,518
	GX 900	1,518	1,518	1,518	1,518	1,366
	GX 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 GT	GT 900	1,518	1,518	1,518	1,518	1,366
	GT 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 SX	SX 160	156	156	156	156	140
	SX 220	192	192	192	192	173
	SX 270	830	830	830	830	747
	SX 320	984	984	984	984	886
	SX 480	1,369	1,368	1,368	1,368	1,231
	SX 570	1,523	1,523	1,523	1,523	1,371
	SX 660	1,687	1,687	1,687	1,687	1,518

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.



### **Related Information**

#### [Intel Arria 10 Device Datasheet](#)

Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

## **PCIe Gen1, Gen2, and Gen3 Hard IP**

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

### **Related Information**

[PCS Features](#) on page 30

## **Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet**

### **Interlaken Support**

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

### **Related Information**

[PCS Features](#) on page 30

### **10 Gbps Ethernet Support**

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.



## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I<sup>2</sup>C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.





## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux\*, VxWorks\*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

### Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

### Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

## Enhanced Configuration and Configuration via Protocol

**Table 25. Configuration Schemes and Features of Intel Arria 10 Devices**

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

Scheme	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) <sup>(13)</sup>	Decompression	Design Security <sup>(14)</sup>	Partial Reconfiguration <sup>(15)</sup>	Remote System Update
JTAG	1 bit	33	33	—	—	Yes <sup>(16)</sup>	—
Active Serial (AS) through the EPCQ-L configuration device	1 bit, 4 bits	100	400	Yes	Yes	Yes <sup>(16)</sup>	Yes
Passive serial (PS) through CPLD or external microcontroller	1 bit	100	100	Yes	Yes	Yes <sup>(16)</sup>	Parallel Flash Loader (PFL) IP core

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<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(16)</sup> Partial configuration can be performed only when it is configured as internal host.



Date	Version	Changes
		<ul style="list-style-type: none"> <li>Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure.</li> <li>Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps.</li> <li>Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table.</li> </ul>
September 2017	2017.09.20	Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps.
July 2017	2017.07.13	Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C".
July 2017	2017.07.06	Added automotive temperature option to Intel Arria 10 GX device family.
May 2017	2017.05.08	<ul style="list-style-type: none"> <li>Corrected protocol names with "1588" to "IEEE 1588v2".</li> <li>Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants.</li> <li>Removed all "Preliminary" marks.</li> </ul>
March 2017	2017.03.15	<ul style="list-style-type: none"> <li>Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices.</li> <li>Rebranded as Intel.</li> </ul>
October 2016	2016.10.31	<ul style="list-style-type: none"> <li>Removed package F36 from Intel Arria 10 GX devices.</li> <li>Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers.</li> </ul>
May 2016	2016.05.02	<ul style="list-style-type: none"> <li>Updated the FPGA Configuration and HPS Booting topic.</li> <li>Remove V<sub>CC</sub> PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices.</li> <li>Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA.</li> <li>Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices.</li> </ul>
February 2016	2016.02.11	<ul style="list-style-type: none"> <li>Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally.</li> <li>Revised the state for Core clock networks in the Summary of Features topic.</li> <li>Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table.</li> <li>Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table.</li> <li>Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table.</li> <li>Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure.</li> <li>Changed transceiver parameters in the "Low Power Serial Transceivers" section.</li> <li>Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table.</li> <li>Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure.</li> <li>Changed the datarates for GT devices in the "PMA Features" section.</li> <li>Changed the datarates for GT devices in the "PCS Features" section.</li> </ul>

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Date	Version	Changes
December 2015	2015.12.14	<ul style="list-style-type: none"> <li>Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb.</li> <li>Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources.</li> </ul>
November 2015	2015.11.02	<ul style="list-style-type: none"> <li>Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660.</li> <li>Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in <b>Number of Multipliers in Intel Arria 10 Devices</b> table.</li> <li>Updated the available options for Arria 10 GX, GT, and SX.</li> <li>Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li> </ul>
June 2015	2015.06.15	Corrected label for Intel Arria 10 GT product lines in the vertical migration figure.
May 2015	2015.05.15	Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller.
May 2015	2015.05.04	<ul style="list-style-type: none"> <li>Added support for 13.5G JESD204b in the Summary of Features table.</li> <li>Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic.</li> <li>Added a note to the table, Maximum Resource Counts for Arria 10 GT devices.</li> <li>Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic.</li> </ul>
January 2015	2015.01.23	<ul style="list-style-type: none"> <li>Added floating point arithmetic features in the Summary of Features table.</li> <li>Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb.</li> <li>Updated the table that lists the memory standards supported by Intel Arria 10 devices.</li> <li>Removed support for DDR3U, LPDDR3 SDRAM, RLD RAM 2, and DDR2.</li> <li>Moved RLD RAM 3 support from hard memory controller to soft memory controller. RLD RAM 3 support uses hard PHY with soft memory controller.</li> <li>Added soft memory controller support for QDR IV.</li> <li>Updated the maximum resource count table to include the number of hard memory controllers available in each device variant.</li> <li>Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps.</li> <li>Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz.</li> <li>Added a feature for fractional synthesis PLLs: PLL cascading.</li> <li>Updated the HPS programmable general-purpose I/Os from 54 to 62.</li> </ul>
September 2014	2014.09.30	<ul style="list-style-type: none"> <li>Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX.</li> <li>Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660.</li> <li>Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150.</li> </ul>
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Date	Version	Changes
August 2014	2014.08.18	<ul style="list-style-type: none"> <li>Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620.</li> <li>Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table.</li> <li>Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration.</li> <li>Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller.</li> <li>Added variable precision DSP blocks support for floating-point arithmetic.</li> </ul>
June 2014	2014.06.19	Updated number of dedicated I/Os in the HPS block to 17.
February 2014	2014.02.21	Updated transceiver speed grade options for GT devices in Figure 2.
February 2014	2014.02.06	Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps.
December 2013	2013.12.10	<ul style="list-style-type: none"> <li>Updated the HPS memory standards support from LPDDR2 to LPDDR3.</li> <li>Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/MMC, DMA, SPI and NAND Flash with ECC blocks .</li> </ul>
December 2013	2013.12.02	Initial release.