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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 320K Logic Elements
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA, FC (29x29)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/10as032e2f29e2sg">https://www.e-xfl.com/product-detail/intel/10as032e2f29e2sg</a>



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## Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

Market	Applications
Wireless	<ul style="list-style-type: none"> <li>• Channel and switch cards in remote radio heads</li> <li>• Mobile backhaul</li> </ul>
Wireline	<ul style="list-style-type: none"> <li>• 40G/100G muxponders and transponders</li> <li>• 100G line cards</li> <li>• Bridging</li> <li>• Aggregation</li> </ul>
Broadcast	<ul style="list-style-type: none"> <li>• Studio switches</li> <li>• Servers and transport</li> <li>• Videoconferencing</li> <li>• Professional audio and video</li> </ul>
Computing and Storage	<ul style="list-style-type: none"> <li>• Flash cache</li> <li>• Cloud computing servers</li> <li>• Server acceleration</li> </ul>
Medical	<ul style="list-style-type: none"> <li>• Diagnostic scanners</li> <li>• Diagnostic imaging</li> </ul>
Military	<ul style="list-style-type: none"> <li>• Missile guidance and control</li> <li>• Radar</li> <li>• Electronic warfare</li> <li>• Secure communications</li> </ul>

### Related Information

#### Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



Feature	Description	
Embedded Hard IP blocks	Variable-precision DSP	<ul style="list-style-type: none"><li>Native support for signal processing precision levels from 18 x 19 to 54 x 54</li><li>Native support for 27 x 27 multiplier mode</li><li>64-bit accumulator and cascade for systolic finite impulse responses (FIRs)</li><li>Internal coefficient memory banks</li><li>Preadder/subtractor for improved efficiency</li><li>Additional pipeline register to increase performance and reduce power</li><li>Supports floating point arithmetic:<ul style="list-style-type: none"><li>Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.</li><li>Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.</li><li>Dynamic accumulator reset control.</li><li>Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.</li></ul></li></ul>
	Memory controller	DDR4, DDR3, and DDR3L
	PCI Express*	PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port
	Transceiver I/O	<ul style="list-style-type: none"><li>10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)</li><li>PCS hard IPs that support:<ul style="list-style-type: none"><li>10-Gbps Ethernet (10GbE)</li><li>PCIe PIPE interface</li><li>Interlaken</li><li>Gbps Ethernet (GbE)</li><li>Common Public Radio Interface (CPRI) with deterministic latency support</li><li>Gigabit-capable passive optical network (GPON) with fast lock-time support</li></ul></li><li>13.5G JESD204b</li><li>8B/10B, 64B/66B, 64B/67B encoders and decoders</li><li>Custom mode support for proprietary protocols</li></ul>
Core clock networks	<ul style="list-style-type: none"><li>Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none"><li>667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface</li><li>800 MHz LVDS interface clocking with 1,600 Mbps LVDS interface</li></ul></li><li>Global, regional, and peripheral clock networks</li><li>Clock networks that are not used can be gated to reduce dynamic power</li></ul>	
Phase-locked loops (PLLs)	<ul style="list-style-type: none"><li>High-resolution fractional synthesis PLLs:<ul style="list-style-type: none"><li>Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)</li><li>Support integer mode and fractional mode</li><li>Fractional mode support with third-order delta-sigma modulation</li></ul></li><li>Integer PLLs:<ul style="list-style-type: none"><li>Adjacent to general purpose I/Os</li><li>Support external memory and LVDS interfaces</li></ul></li></ul>	
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none"><li>1.6 Gbps LVDS—every pair can be configured as receiver or transmitter</li><li>On-chip termination (OCT)</li><li>1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing</li></ul>	
External Memory Interface	<ul style="list-style-type: none"><li>Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none"><li>DDR4—speeds up to 1,200 MHz/2,400 Mbps</li><li>DDR3—speeds up to 1,067 MHz/2,133 Mbps</li></ul></li><li>Soft memory controller—provides support for RLDRAM 3<sup>(2)</sup>, QDR IV<sup>(2)</sup>, and QDR II+</li></ul>	
continued...		



## Maximum Resources

**Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)**

Resource		Product Line				
		GX 160	GX 220	GX 270	GX 320	GX 480
Logic Elements (LE) (K)		160	220	270	320	480
ALM		61,510	80,330	101,620	119,900	183,590
Register		246,040	321,320	406,480	479,600	734,360
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620
	MLAB	1,050	1,690	2,452	2,727	4,164
Variable-precision DSP Block		156	192	830	985	1,368
18 x 19 Multiplier		312	384	1,660	1,970	2,736
PLL	Fractional Synthesis	6	6	8	8	12
	I/O	6	6	8	8	12
17.4 Gbps Transceiver		12	12	24	24	36
GPIO <sup>(3)</sup>		288	288	384	384	492
LVDS Pair <sup>(4)</sup>		120	120	168	168	222
PCIe Hard IP Block		1	1	2	2	2
Hard Memory Controller		6	6	8	8	12

<sup>(3)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(4)</sup> Each LVDS I/O pair can be used as differential input or output.



## Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





## Maximum Resources

**Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices**

Resource		Product Line	
		GT 900	GT 1150
Logic Elements (LE) (K)		900	1,150
ALM		339,620	427,200
Register		1,358,480	1,708,800
Memory (Kb)	M20K	48,460	54,260
	MLAB	9,386	12,984
Variable-precision DSP Block		1,518	1,518
18 x 19 Multiplier		3,036	3,036
PLL	Fractional Synthesis	32	32
	I/O	16	16
Transceiver	17.4 Gbps	72 <sup>(5)</sup>	72 <sup>(5)</sup>
	25.8 Gbps	6	6
GPIO <sup>(6)</sup>		624	624
LVDS Pair <sup>(7)</sup>		312	312
PCIe Hard IP Block		4	4
Hard Memory Controller		16	16

### Related Information

#### Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

## Package Plan

**Table 11. Package Plan for Intel Arria 10 GT Devices**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	SF45 (45 mm x 45 mm, 1932-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR
GT 900	—	624	72
GT 1150	—	624	72

<sup>(5)</sup> If all 6 GT channels are in use, 12 of the GX channels are not usable.

<sup>(6)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(7)</sup> Each LVDS I/O pair can be used as differential input or output.



## Maximum Resources

**Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices**

Resource		Product Line						
		SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Logic Elements (LE) (K)		160	220	270	320	480	570	660
ALM		61,510	80,330	101,620	119,900	183,590	217,080	251,680
Register		246,040	321,320	406,480	479,600	734,360	868,320	1,006,720
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620	36,000	42,620
	MLAB	1,050	1,690	2,452	2,727	4,164	5,096	5,788
Variable-precision DSP Block		156	192	830	985	1,368	1,523	1,687
18 x 19 Multiplier		312	384	1,660	1,970	2,736	3,046	3,374
PLL	Fractional Synthesis	6	6	8	8	12	16	16
	I/O	6	6	8	8	12	16	16
17.4 Gbps Transceiver		12	12	24	24	36	48	48
GPIO <sup>(8)</sup>		288	288	384	384	492	696	696
LVDS Pair <sup>(9)</sup>		120	120	168	168	174	324	324
PCIe Hard IP Block		1	1	2	2	2	2	2
Hard Memory Controller		6	6	8	8	12	16	16
ARM Cortex-A9 MPCore Processor		Yes	Yes	Yes	Yes	Yes	Yes	Yes

## Package Plan

**Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 160	48	144	6	48	192	12	48	240	12	—	—	—
SX 220	48	144	6	48	192	12	48	240	12	—	—	—
SX 270	—	—	—	48	192	12	48	312	12	48	336	24
SX 320	—	—	—	48	192	12	48	312	12	48	336	24
continued...												

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(9)</sup> Each LVDS I/O pair can be used as differential input or output.





Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 480	—	—	—	—	—	—	48	312	12	48	444	24
SX 570	—	—	—	—	—	—	—	—	—	48	444	24
SX 660	—	—	—	—	—	—	—	—	—	48	444	24

**Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F35 (35 mm × 35 mm, 1152-pin FBGA)			KF40 (40 mm × 40 mm, 1517-pin FBGA)			NF40 (40 mm × 40 mm, 1517-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 270	48	336	24	—	—	—	—	—	—
SX 320	48	336	24	—	—	—	—	—	—
SX 480	48	348	36	—	—	—	—	—	—
SX 570	48	348	36	96	600	36	48	540	48
SX 660	48	348	36	96	600	36	48	540	48

#### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

**Figure 5. ALM for Intel Arria 10 Devices**



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

## Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
	SX 320	984	1,968	984	984	984
	SX 480	1,368	2,736	1,368	1,368	1,368
	SX 570	1,523	3,046	1,523	1,523	1,523
	SX 660	1,687	3,374	1,687	1,687	1,687

**Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Single Precision Floating-Point Multiplication Mode	Single-Precision Floating-Point Adder Mode	Single-Precision Floating-Point Multiply Accumulate Mode	Peak Giga Floating-Point Operations per Second (GFLOPs)
Intel Arria 10 GX	GX 160	156	156	156	156	140
	GX 220	192	192	192	192	173
	GX 270	830	830	830	830	747
	GX 320	984	984	984	984	886
	GX 480	1,369	1,368	1,368	1,368	1,231
	GX 570	1,523	1,523	1,523	1,523	1,371
	GX 660	1,687	1,687	1,687	1,687	1,518
	GX 900	1,518	1,518	1,518	1,518	1,366
	GX 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 GT	GT 900	1,518	1,518	1,518	1,518	1,366
	GT 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 SX	SX 160	156	156	156	156	140
	SX 220	192	192	192	192	173
	SX 270	830	830	830	830	747
	SX 320	984	984	984	984	886
	SX 480	1,369	1,368	1,368	1,368	1,231
	SX 570	1,523	1,523	1,523	1,523	1,371
	SX 660	1,687	1,687	1,687	1,687	1,518

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.



## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

**Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices**

Variant	Product Line	M20K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Intel Arria 10 GX	GX 160	440	8,800	1,680	1,050	9,850
	GX 220	587	11,740	2,703	1,690	13,430
	GX 270	750	15,000	3,922	2,452	17,452
	GX 320	891	17,820	4,363	2,727	20,547
	GX 480	1,431	28,620	6,662	4,164	32,784
	GX 570	1,800	36,000	8,153	5,096	41,096
	GX 660	2,131	42,620	9,260	5,788	48,408
	GX 900	2,423	48,460	15,017	9,386	57,846
	GX 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 GT	GT 900	2,423	48,460	15,017	9,386	57,846
	GT 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 SX	SX 160	440	8,800	1,680	1,050	9,850
	SX 220	587	11,740	2,703	1,690	13,430
	SX 270	750	15,000	3,922	2,452	17,452
	SX 320	891	17,820	4,363	2,727	20,547
	SX 480	1,431	28,620	6,662	4,164	32,784
	SX 570	1,800	36,000	8,153	5,096	41,096
	SX 660	2,131	42,620	9,260	5,788	48,408



The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
  - Conventional integer mode equivalent to the general purpose PLL
  - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

## I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

## FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
  - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
  - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis

- Series ( $R_S$ ) and parallel ( $R_T$ ) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

## External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

### Related Information

#### [External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

## Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

**Figure 6. Intel Arria 10 Transceiver Block Architecture**



## Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.



Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices

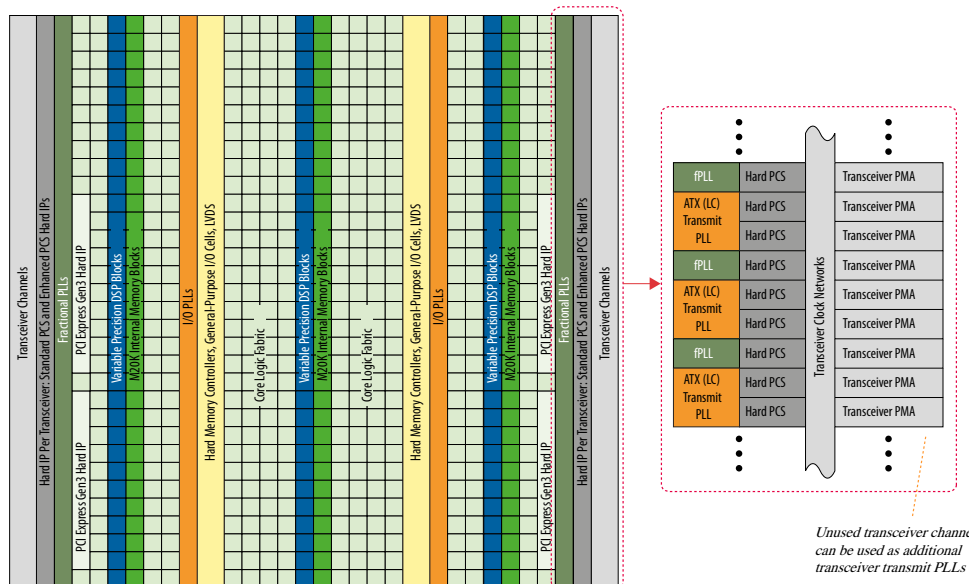


Figure 8. Device Chip Overview for Intel Arria 10 SX Devices



## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.





Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

**Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices**

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices) 1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 12.5 Gbps
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Variable Gain Amplifier	Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
Advanced Transmit (ATX) PLL	Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
Dynamic Partial Reconfiguration	Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

## PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.



Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
CPRI 6.0 (64B/66B)	0.6144 to 10.1376	Native PHY	Enhanced PCS
CPRI 4.2 (8B/10B)	0.6144 to 9.8304	Native PHY	Standard PCS
OBSAI RP3 v4.2	0.6144 to 6.144	Native PHY	Standard PCS
SD-SDI/HD-SDI/3G-SDI	0.143 <sup>(12)</sup> to 2.97	Native PHY	Standard PCS

### Related Information

#### [Intel Arria 10 Transceiver PHY User Guide](#)

Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

## SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

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<sup>(12)</sup> The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.



The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core  $V_{CC}$  while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

Document Version	Changes
2018.04.09	Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features.

Date	Version	Changes
January 2018	2018.01.17	<ul style="list-style-type: none"><li>• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.</li><li>• Updated maximum frequency supported for half rate QDR II and QDR II + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft Memory Controller</i> table.</li><li>• Updated transceiver backplane capability to 12.5 Gbps.</li><li>• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure.</li></ul>
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Date	Version	Changes
		<ul style="list-style-type: none"> <li>Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure.</li> <li>Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps.</li> <li>Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table.</li> </ul>
September 2017	2017.09.20	Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps.
July 2017	2017.07.13	Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C".
July 2017	2017.07.06	Added automotive temperature option to Intel Arria 10 GX device family.
May 2017	2017.05.08	<ul style="list-style-type: none"> <li>Corrected protocol names with "1588" to "IEEE 1588v2".</li> <li>Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants.</li> <li>Removed all "Preliminary" marks.</li> </ul>
March 2017	2017.03.15	<ul style="list-style-type: none"> <li>Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices.</li> <li>Rebranded as Intel.</li> </ul>
October 2016	2016.10.31	<ul style="list-style-type: none"> <li>Removed package F36 from Intel Arria 10 GX devices.</li> <li>Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers.</li> </ul>
May 2016	2016.05.02	<ul style="list-style-type: none"> <li>Updated the FPGA Configuration and HPS Booting topic.</li> <li>Remove V<sub>CC</sub> PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices.</li> <li>Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA.</li> <li>Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices.</li> </ul>
February 2016	2016.02.11	<ul style="list-style-type: none"> <li>Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally.</li> <li>Revised the state for Core clock networks in the Summary of Features topic.</li> <li>Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table.</li> <li>Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table.</li> <li>Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table.</li> <li>Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure.</li> <li>Changed transceiver parameters in the "Low Power Serial Transceivers" section.</li> <li>Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table.</li> <li>Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure.</li> <li>Changed the datarates for GT devices in the "PMA Features" section.</li> <li>Changed the datarates for GT devices in the "PCS Features" section.</li> </ul>

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Date	Version	Changes
December 2015	2015.12.14	<ul style="list-style-type: none"> <li>Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb.</li> <li>Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources.</li> </ul>
November 2015	2015.11.02	<ul style="list-style-type: none"> <li>Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660.</li> <li>Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in <b>Number of Multipliers in Intel Arria 10 Devices</b> table.</li> <li>Updated the available options for Arria 10 GX, GT, and SX.</li> <li>Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li> </ul>
June 2015	2015.06.15	Corrected label for Intel Arria 10 GT product lines in the vertical migration figure.
May 2015	2015.05.15	Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller.
May 2015	2015.05.04	<ul style="list-style-type: none"> <li>Added support for 13.5G JESD204b in the Summary of Features table.</li> <li>Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic.</li> <li>Added a note to the table, Maximum Resource Counts for Arria 10 GT devices.</li> <li>Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic.</li> </ul>
January 2015	2015.01.23	<ul style="list-style-type: none"> <li>Added floating point arithmetic features in the Summary of Features table.</li> <li>Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb.</li> <li>Updated the table that lists the memory standards supported by Intel Arria 10 devices.</li> <li>Removed support for DDR3U, LPDDR3 SDRAM, RLD RAM 2, and DDR2.</li> <li>Moved RLD RAM 3 support from hard memory controller to soft memory controller. RLD RAM 3 support uses hard PHY with soft memory controller.</li> <li>Added soft memory controller support for QDR IV.</li> <li>Updated the maximum resource count table to include the number of hard memory controllers available in each device variant.</li> <li>Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps.</li> <li>Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz.</li> <li>Added a feature for fractional synthesis PLLs: PLL cascading.</li> <li>Updated the HPS programmable general-purpose I/Os from 54 to 62.</li> </ul>
September 2014	2014.09.30	<ul style="list-style-type: none"> <li>Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX.</li> <li>Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660.</li> <li>Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150.</li> </ul>
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